Cooperation on the development and production of state-of-the-art microelectronics.

Ю.А.Мурин, С.Себаллос.

совещания по научно-техническому сотрудничеству с КНР - 2022.10.13

OUTLINE

- Cooperation background
- Current work
- Future collaboration

MPD-ITS Collaboration

CERN supervision

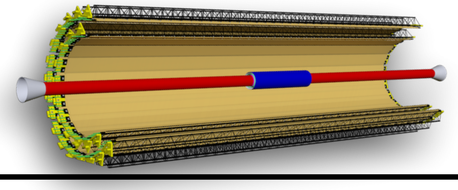
Original plan

JINR		CCNU	
SPbSU	MSU	Ins. Mod. Phys	USTC

- Components distribution

- HIC assembly (33%)	- HIC Assembly (66%)
- Stave assembly (33%)	- Stave assembly (66%)
- Simulations (50%)	- Simulations (50%)
- Integration Mech. & Cooling (100%)	- Read-out electronics Devel. (100%)
- DCS (100%)	- Read-out electronics Prod. (100%)

50%



50%

Layer assembly, detector commissioning and In-beam Tests at JINR

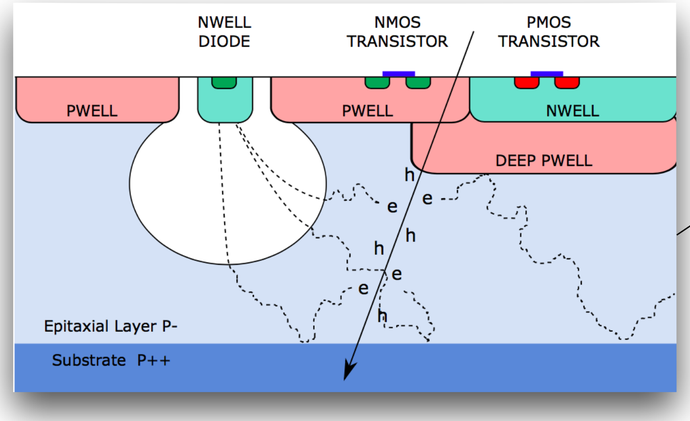
The MAPS chip

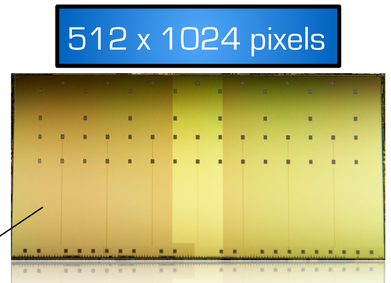
TowerJazz 0.18 µm CMOS pixel sensor

» High-resistivity (> 1kΩ cm) p-type epitaxial layer (20µm - 40µm thick) on p-type substrate.

» Small n-well diode (2-3 µm diameter), ~100 times smaller than pixel => low capacitance.

» Deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area.





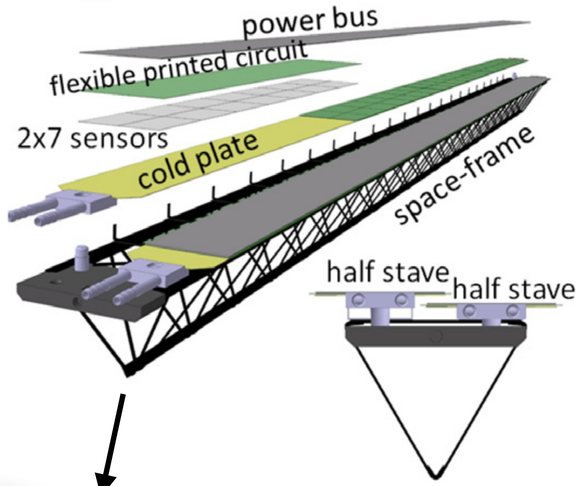
Sensor architecture

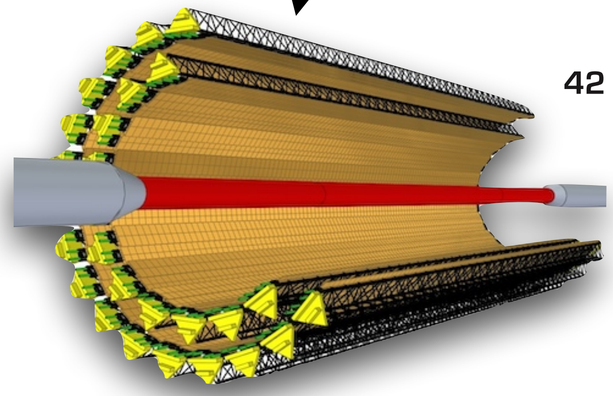
Size: 15mm x 30mm

Pixel pitch: 28µm x 28µm

Power consumption: 39mW/cm^2

Dead area 1.1mm x 30mm

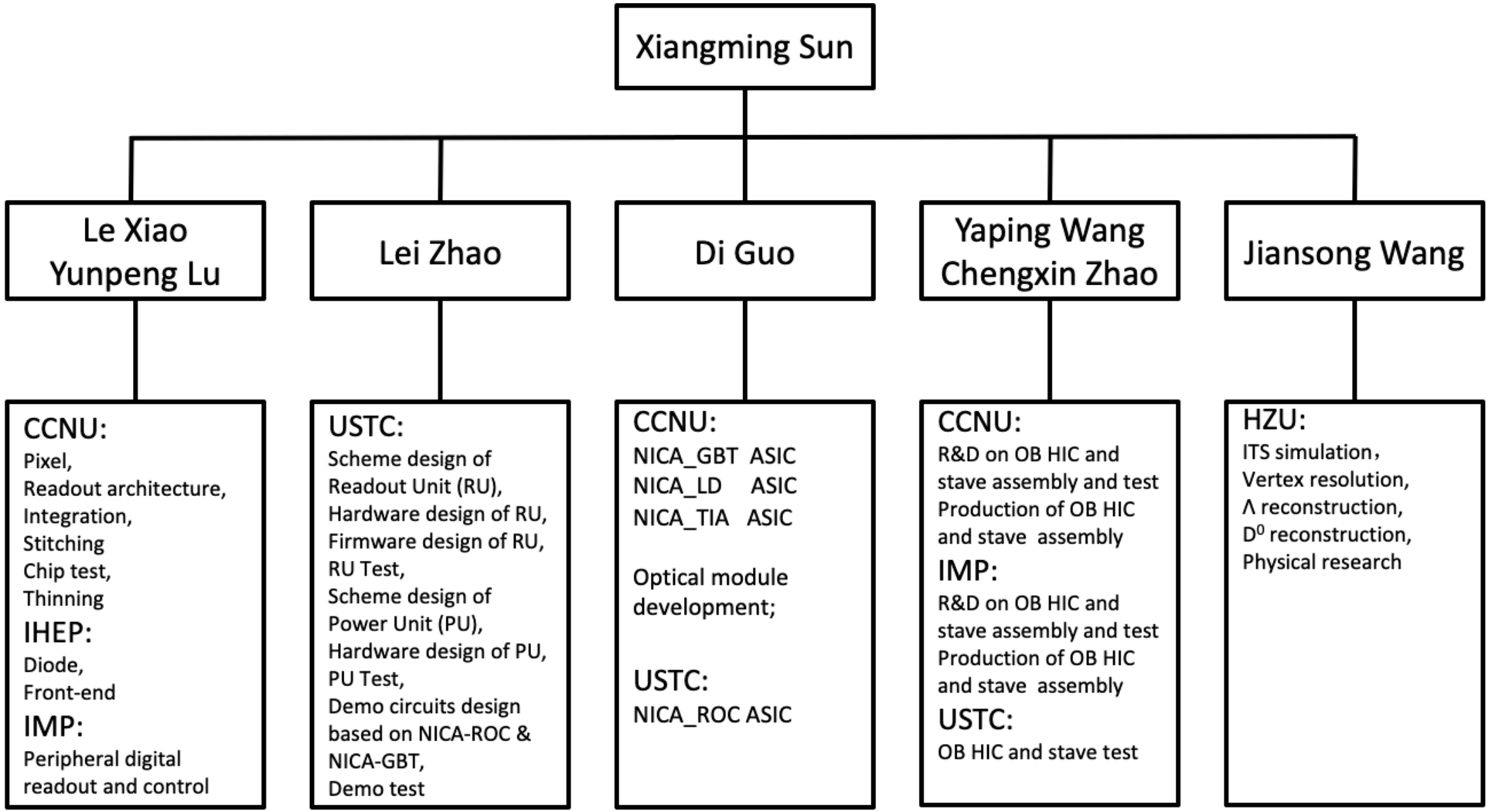




42 Staves

MPD-ITS Collaboration

Chinese Group Members



MPD-ITS collaboration coordination

After a Pandemic-related interruption the collaboration was resumed in Sept. 2020

MPD-ITS meeting for resuming Russia-China collaboration
Friday 25 Sep 2020, 09:00 → 10:05 Europe/Moscow
Webcast (LBNL)

2nd Meeting on China-Russia MPD IT System
16 Oct 2020, 18:00 → 17 Oct 2020, 23:55 Europe/Moscow
Webcast (LBNL)

MPD-ITS General Coordination meeting
Thursday 18 Feb 2021, 18:00 → 20:00 Europe/Moscow
Nu Xu (Central China Normal University(CCNU))

MPD-ITS General Coordination meeting
Thursday 24 Jun 2021, 09:00 → 10:25 Europe/Moscow
Nu Xu (Central China Normal University(CCNU))

MPD-ITS General Coordination meeting
Wednesday 26 Jan 2022, 09:00 → 10:00 Europe/Moscow
Nu Xu (Central China Normal University(CCNU))

MPD-ITS General Coordination meeting
Friday 22 Apr 2022, 09:00 → 10:00 Europe/Moscow
Nu Xu (Central China Normal University(CCNU))

MPD-ITS General Coordination meeting
Thursday 4 Aug 2022, 10:00 → 11:40 Europe/Moscow
Room 120 (JINR-LHEP Build. 216)
Yuri Murin

MPD-ITS General Coordination meeting
Thursday 29 Sep 2022, 10:00 → 11:00 Europe/Moscow
Room 215 - Conference room (JINR-LHEP Build. 215)
Yuri Murin

MPD-ITS Readout electronics coordination meeting
Friday 18 Dec 2020, 12:00 → 14:00 Europe/Moscow
Webcast (JINR)

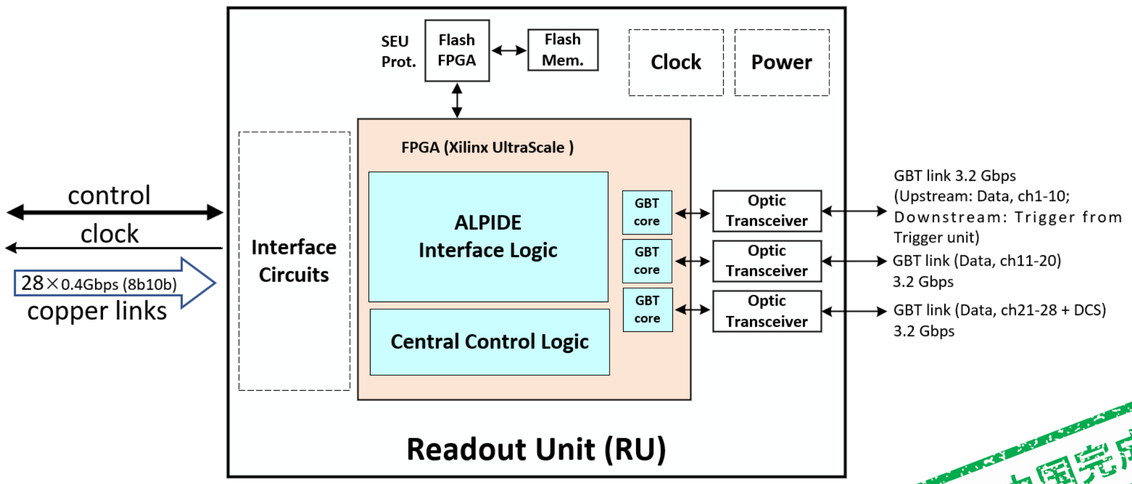
MPD-ITS Readout electronics coordination meeting
Monday 8 Feb 2021, 16:00 → 18:00 Europe/Moscow
Webcast (JINR)

MPD-ITS Workgroup meeting 2021.06.17 - Special Readout Edition
Thursday 17 Jun 2021, 10:00 → 12:00 Europe/Moscow
Bld. 216 (Room 120 & Webcast)
Yuri Murin

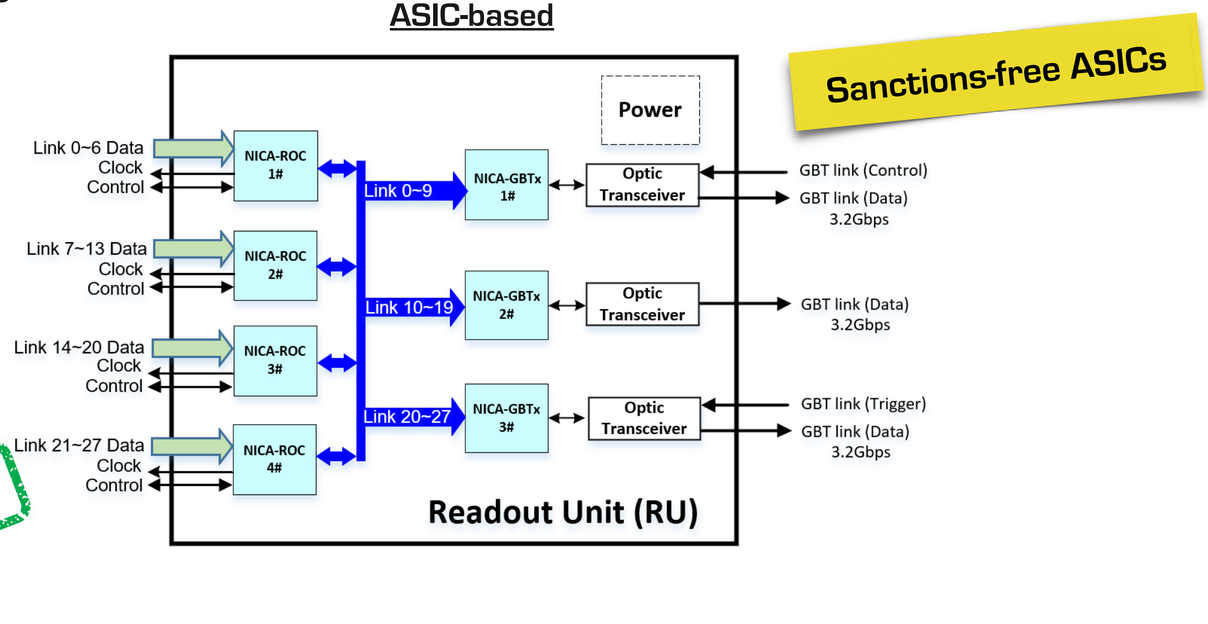
Readout electronics Design/Production

MPD-ITS RU design solutions.

FPGA-based



ASIC-based

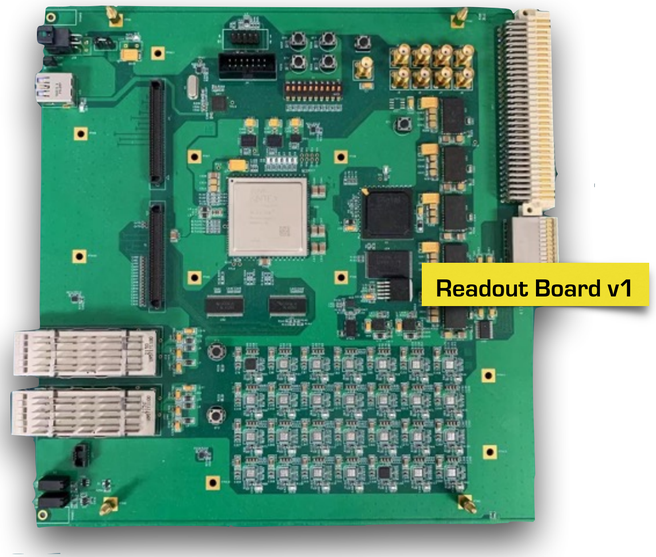


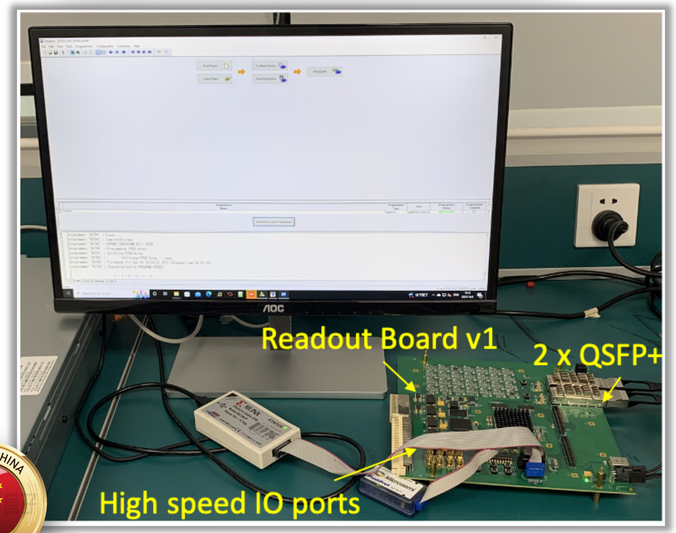
- **NICA_ROC:** Concentrates the output data of front-end MAPS chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to ALPIDE chips.
- **NICA_GBTx:** A high-speed bidirectional data interface ASIC for optical links.
  - It receives multichannel data from the front-end (NICA_ROC), performs scrambling, encoding, frame building and serializing as the main function for the up-link direction.
  - It receives high-speed serial data from the back-end, performs CDR (Clock and Data Recovery), deserializing, decoding and distributing to the front-end as the main function for the down-link direction.
- **NICA_LD (Laser Driver) and NICA_TIA (Transimpedance Amplifier):** Are two analog ASICs that would be integrated together with the laser and PD (Pin Diode) in the customized optical transceiver module.
  - NICA_LD receives the high-speed up-link serial data from NICA_GBTx and amplifies the signal to driver the laser.
  - NICA_TIA receives the down-link serial signal from the pin diode, and amplifies the signal to NICA_GBTx, so that the data can be furthered processed in NICA_GBTx.

Readout electronics Design/Production

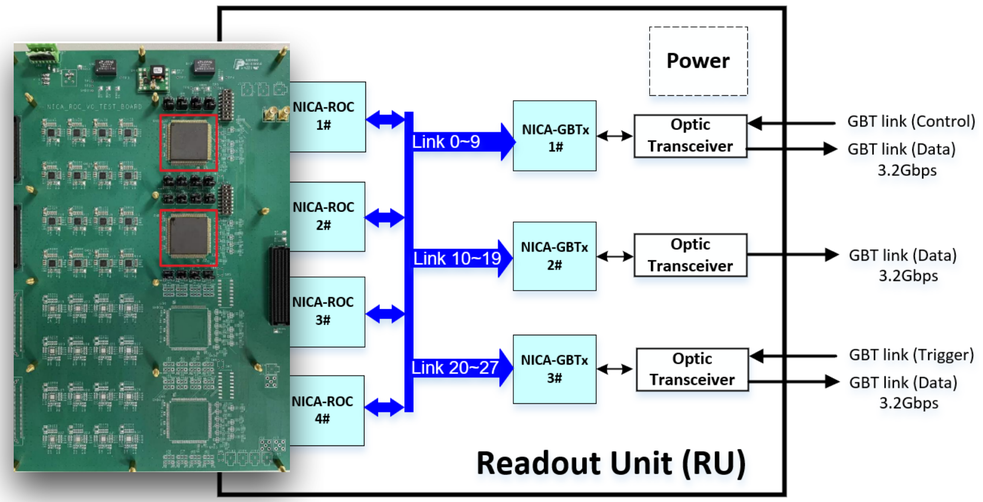
MPD-ITS RU design solutions.

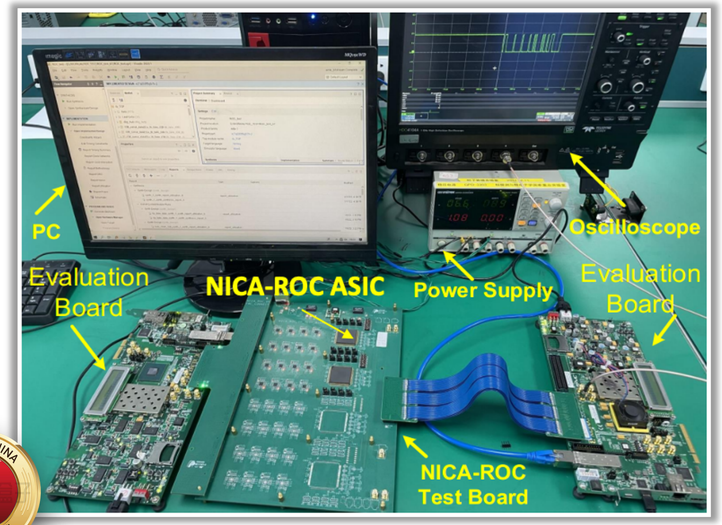
FPGA-based





ASIC-based

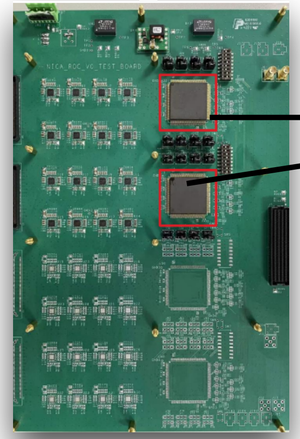




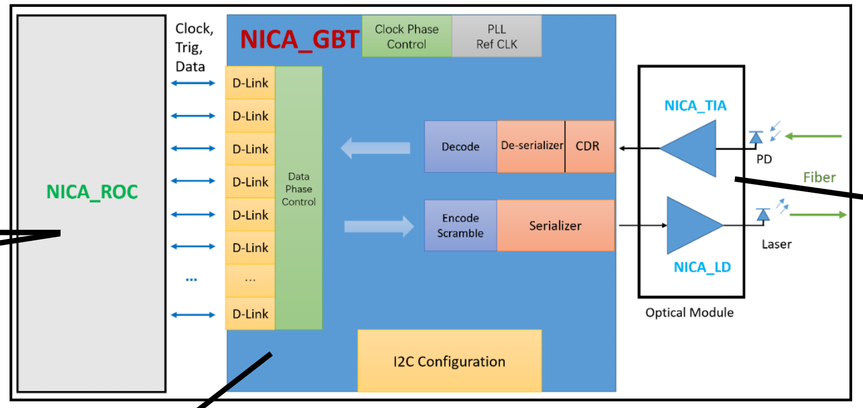
Readout electronics Design/Production - ASIC_based

NICA_GBT, NICA_ROC, NICA_LD/Rx ASIC and customized Optical Module

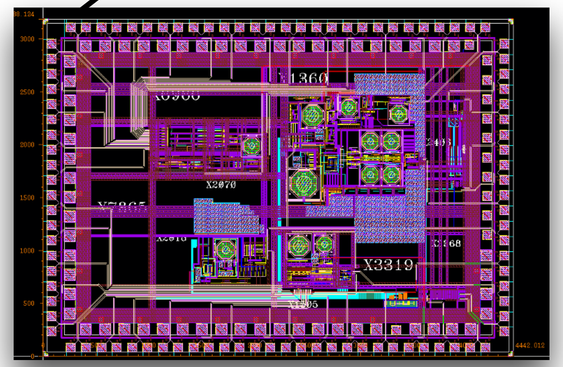
NICA_ROC



First chips already under test

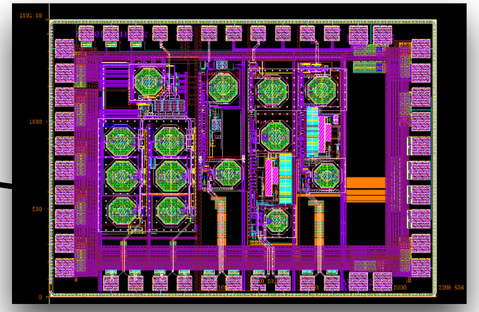


NICA_GBT_v1



Overall layout

NICA_LD & NICA_TIA



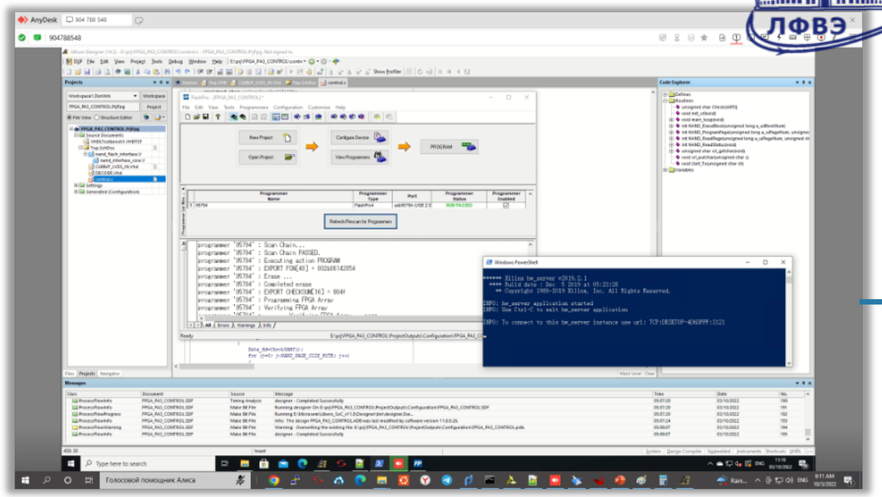
Overall layout

NICA_LD and NICA_TIA designs are combined into one chip for test and verification

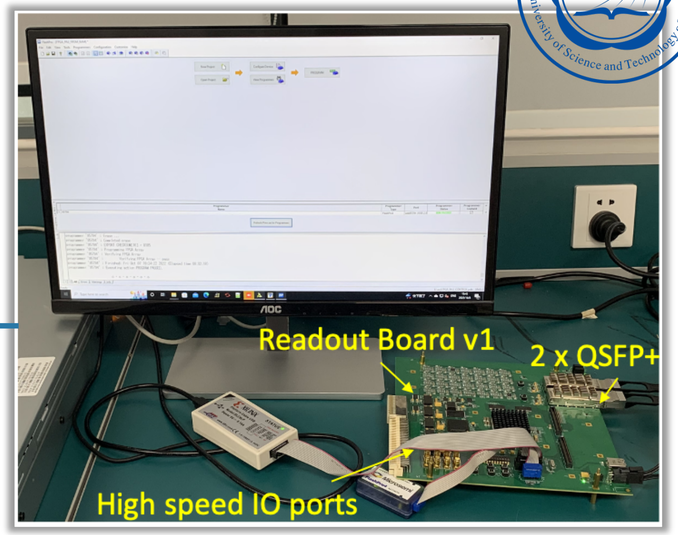
The second MPW run for the NICA_LD and NICA_Rx together with NICA_GBTx is scheduled for October 16th, 2022 based on SMIC 55nm

Readout electronics Design/Production - FPGA_based

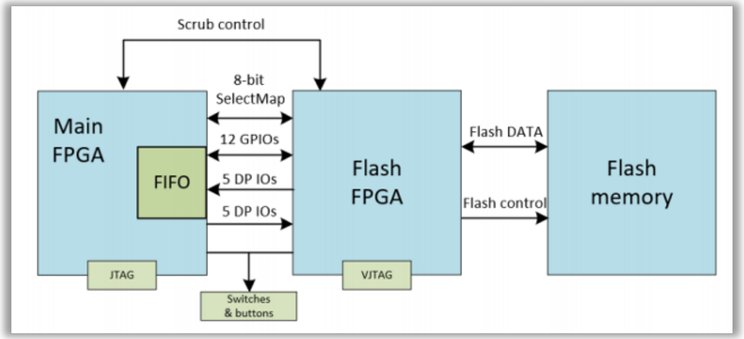
The RU firmware is being jointly developed by T. Yao (USTC) and R. Arteche (JINR)



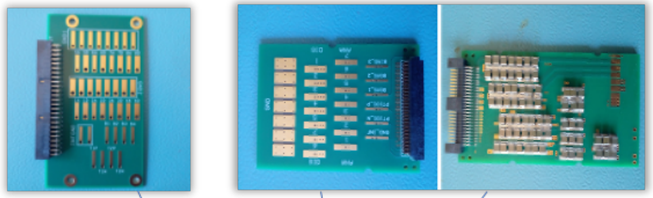
internet

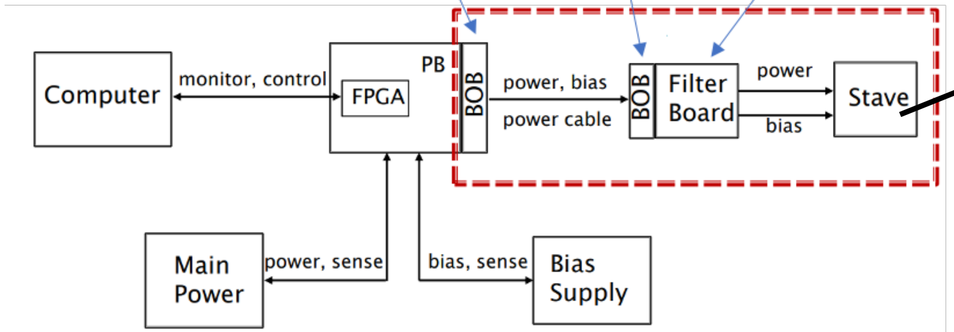


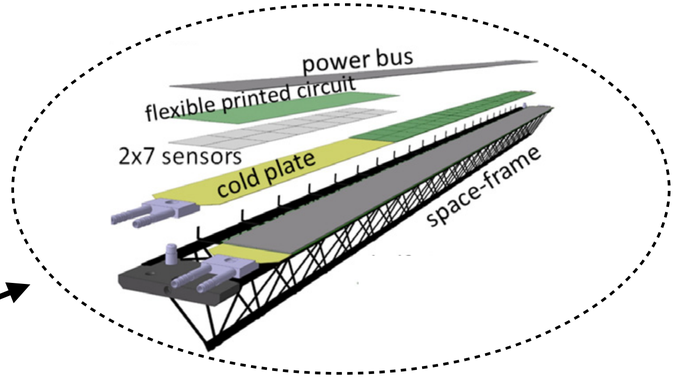
Arteche is remotely testing the firmware of the Auxiliary Flash FPGA that will be responsible of the booting, scrubbing, monitor and control of the main FPGA.



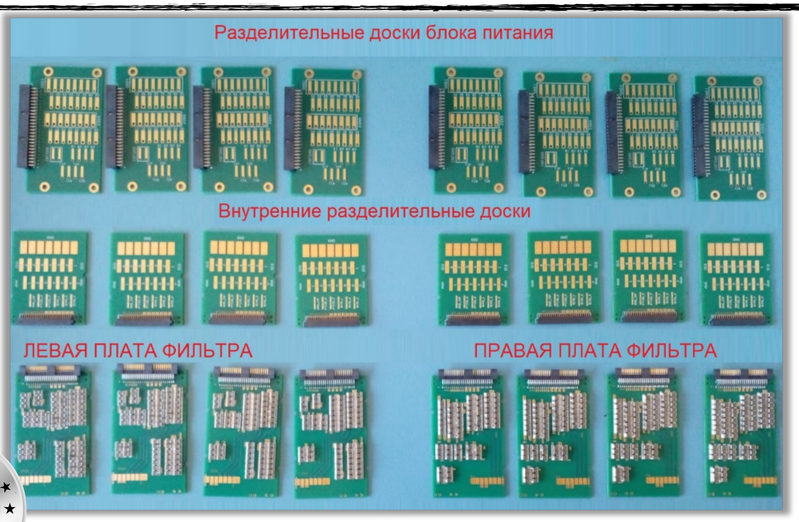
Production of 7 Sets of Breakout and Filters Boards







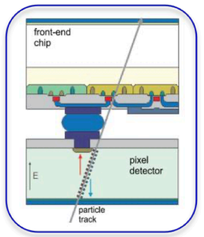
Four Set of Break Out Boards and Filter Boards will be exported to China

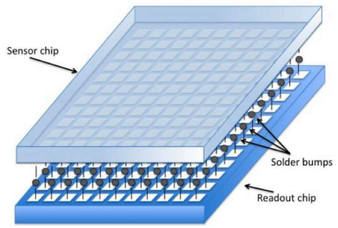


From Russia with Love

The MAPS chip

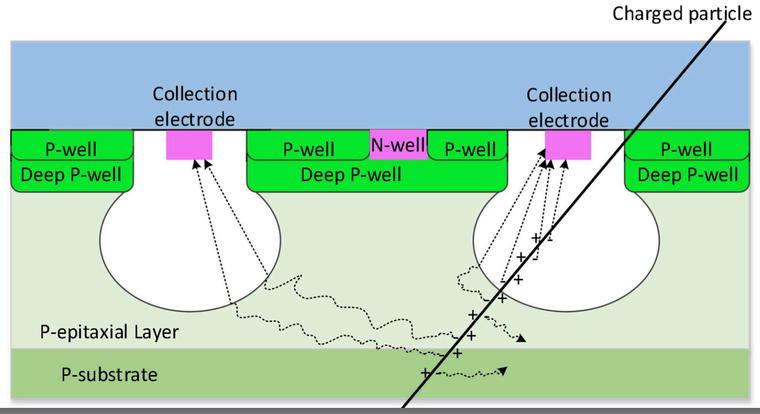
Technique scheme – MAPS VS Hybrid pixel detector





Hybrid pixel detector:

- The sensor and readout electronics are combined by flip chip bonding
- Fast readout rate
- Strong radiation resistance
- Large input capacitance
- High mass
- High cost



MAPS:

- The sensor and readout circuit are integrated on the same silicon chip
- Small input capacitance->Achieve low power consumption
- Low mass
- Low cost

Le Xiao (CCNU)

First-ever full MAPS detector (10 m²)

1. ALICE-ITS (LHC, CERN)
2. sPHENIX-MVTX (RHIC, BNL)
3. MPD-ITS (NICA, JINR)

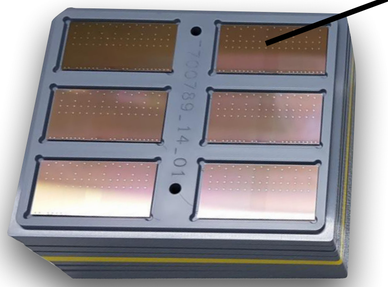
MAPS-based tracker technology is foreseen to become the new standard for fundamental and applied research.

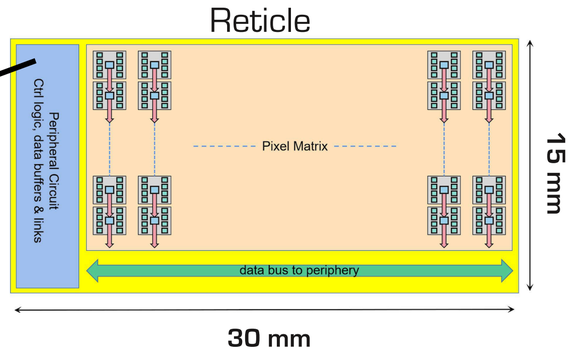
MAPS are currently spinning off, targeting X-ray and synchrotron radiation applications in astrophysics, biomedical imaging, and spectroscopy.

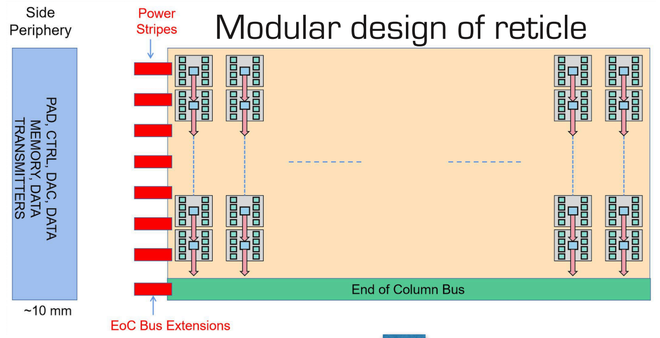
The MAPS chip

Monolithic Active Pixel Sensors

MPD-ITS Outer Barrel

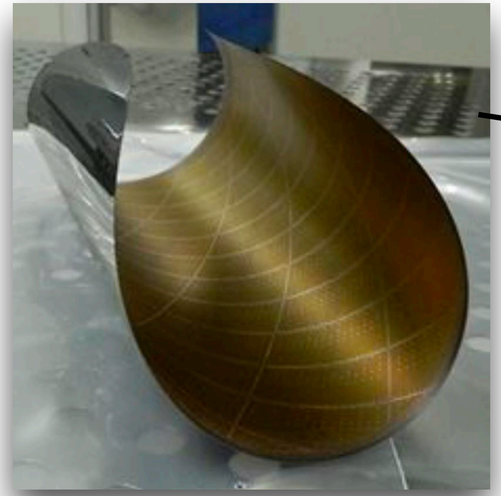


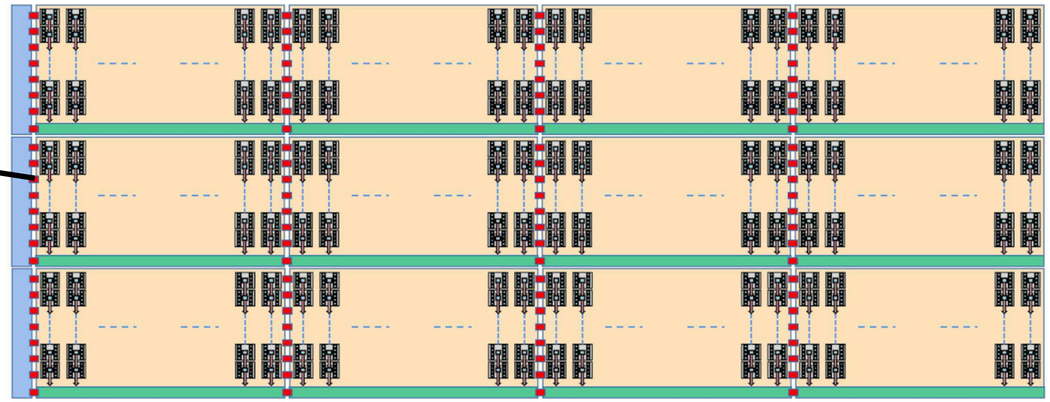




Stitching

MPD-ITS Inner Barrel

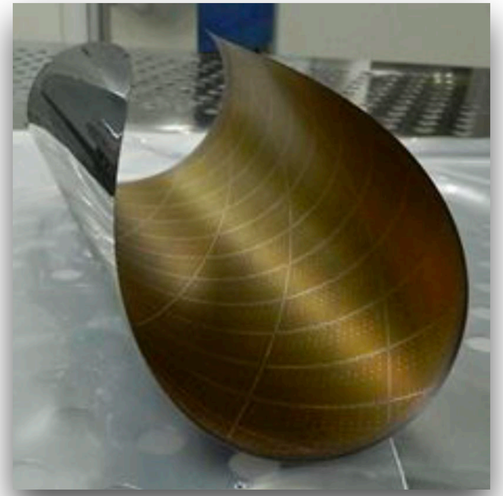




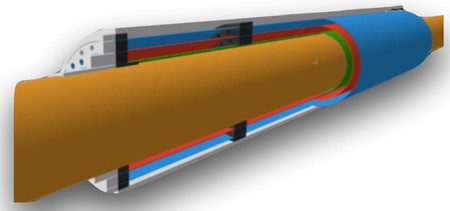
Large-area MAPS (14 cm x 5.6 cm/7.5 cm/9.4 cm)

The Chinese version of MAPS

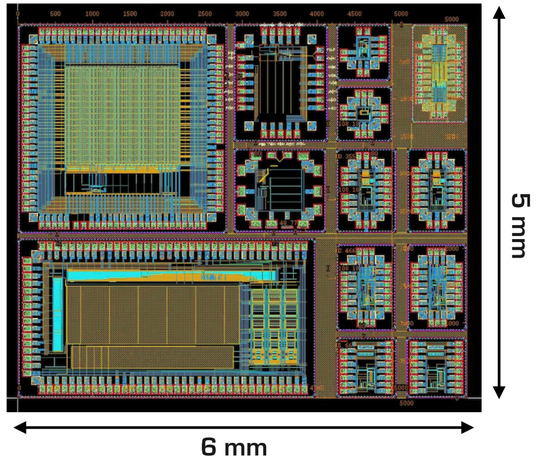
MPD-ITS Inner Barrel



Already undergoing R&D as part of the MPD-ITS project



First MPW on a 55 nm CIS process



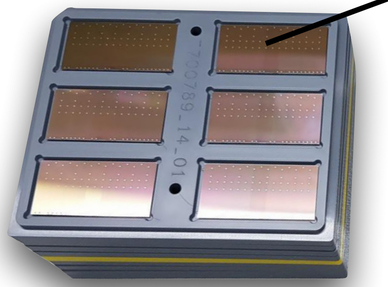
The wafers may be delivered in December 2022.

- CMOS Process: 55 nm CIS, stitching、 4 metal layers , support N-WELL、P-WELL、 Deep N-WELL、 Deep P-WELL.
- Die size: 6mm x 5mm
- Including 10 kinds of chips: readout architecture chip, diode and pixel test chip, PLL, Serilizer, DAC, LDO, ADC, etc..

The Chinese version of MAPS

Monolithic Active Pixel Sensors

MPD-ITS Outer Barrel



19000 chips should arrive from CERN

And that is all!

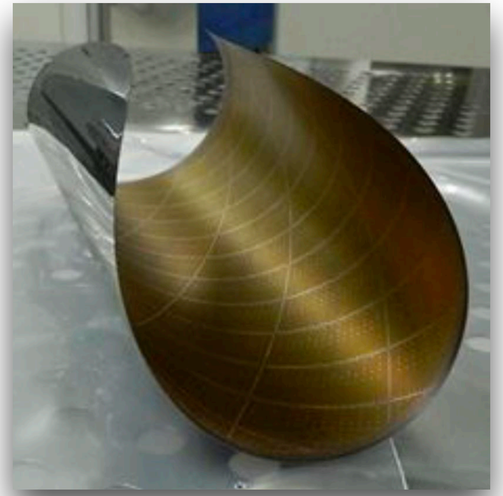
A new project proposal was born!

Chinese ALPIDE-like MAPS version

- Development time ~ 2 years.
- Russian contribution (Initially):
  - Financial support
  - Providing beam test capabilities.

Access to unlimited number!!!

MPD-ITS Inner Barrel



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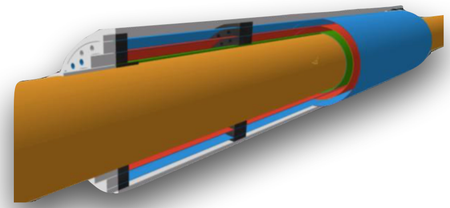
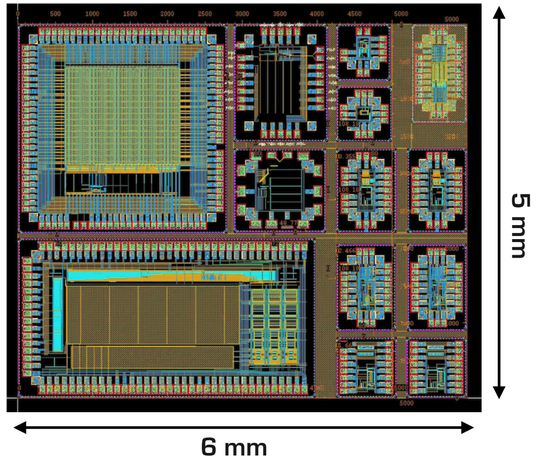


First MPW on a 55 nm CIS process



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- Die size: 6mm x 5mm
- Including 10 kinds of chips: readout architecture chip, diode and pixel test chip, PLL, Serilizer, DAC, LDO, ADC, etc..

Joint Research Proposal

RSF-NSFC Cooperation: Possibility for Joint Russian-Chinese Project Proposals

2023-2025 Joint Project Description Template

A complete proposal in this competition consists of the joint project description (following this document) and the specific documents, necessary for both funding organizations respectively (for Chinese Scientists – following the NSFC rules, for Russian scientists – following the RSF competition documentation).
The proposal must be written in English. There is a strict limit of 20 pages for the joint project description (font size: 11 or 12, line spacing: 1.15). Applicants are obliged to ensure that the project description contains sufficient information for evaluation.

Core data

Title of the Research Project

Title in English: **Fast data processing through real-time AI for NICA/MPD and future EicC detectors**
Title in Russian: **Быстрая система обработки данных на основе ИИ в режиме реального времени для MPD и будущих экспериментов на EicC**
Title in Mandarin: **应用于 NICA/MPD 和未来 EicC 探测器上基于实时人工智能的快速数据处理**

Project Partners
Name and affiliation of the Chinese Principal Investigator
Name (in both English and Mandarin), title: **王亚平, Yaping Wang, Professor**
Host Institution: **Central China Normal University (CCNU)**
Contact telephone number and E-Mail address: **86-13697332703, wangyaping@mail.ccnu.edu.cn**

Name and affiliation of the Russian Principal Investigator
Name (including Patronymic name), title: **César Ceballos Sánchez, Staff Scientist**
Host institution: **Joint Institute for Nuclear Research (JINR)**
Contact telephone number and E-Mail address: **+7 9261486684, ceballos@jinr.ru**

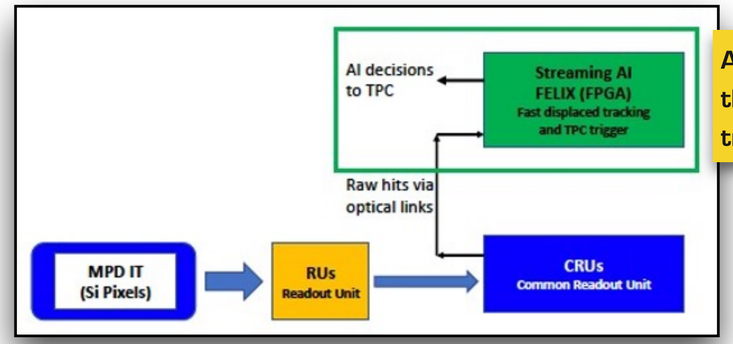
Motivation: Current and future major HEP experiments would face the challenge on how to deal with the large volume of raw data (> Tb/s) generated from sophisticated state-of-the-art detectors in high rate collisions.

Basis: most heavy flavour physics measurements can be performed solely based on tracking.

NICA Example:

- NICA can deliver proton beams at interaction rate around 4 MHz .
- The triggered readout rate of MPD is limited to 5 kHz by TPC readout.
- The MPD is limited to collect less than 1% of the total p+p (and p+Au) rate when using triggered readout

Proposed solution: To develop real-time artificial intelligence (AI) technologies implemented in the detector readout electronics loop that address these challenges (Selective Streaming Readout).



AI-trained FPGA, will identify tracks from heavy quark decays that are pointing away from the nominal beam center to trigger the readout of the much slower TPC detector.

Goal: To design and test a system for the MPD experiment to demonstrate the feasibility and performance, and later apply it to the EicC experiments.

Summary

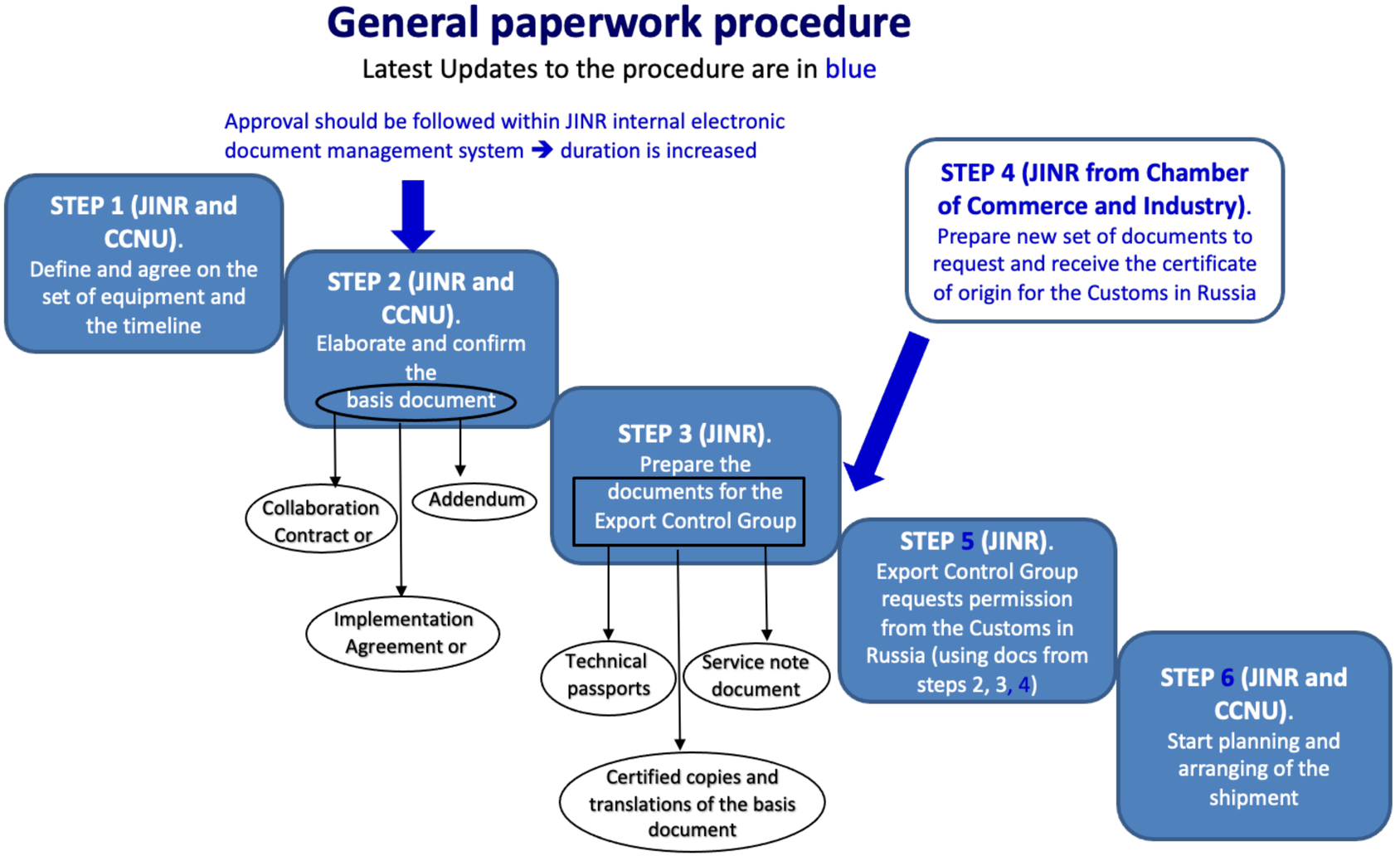
There is a mutual interest on getting access to sanctions-free state-of-the-art microelectronics.

- The MPD-ITS project offers the opportunity to strength the collaboration with Chinese top-level scientific institutions (CCNU, HZU, IHEP, IMP, USTC).
- The current and future collaborations on microelectronics development and production will make available to Russia sanctions-free cutting-edge technologies.
- A special role is played by the joint development and production of Monolithic Active Pixel Sensors (MAPS) to be used on:
  - Current and future HEP experiments.
  - Other possible applications.

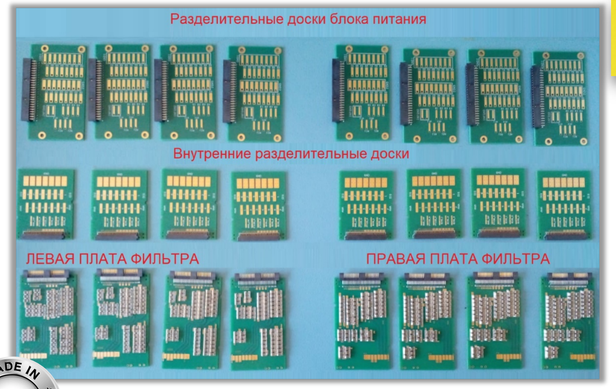
- <u>Current and future enrolments on the collaboration with China:</u>
  - Production of the Inner Tracking System of the MPD (Electronics, Mechanics, Assembly).
  - Developing and production of FPGA-based GBTx emulator readout units.
  - Developing and production of full ASIC-based readout units.
  - Developing and production of ALPIDE-like MAPS and large-area sensors.
  - Developing and production of an AI fast data-processing smart trigger system ITS-TPC.

Remark (!)

It will be very difficult to implement serious and large-scale collaboration with China unless the current trading procedure won't be revised and restructure.



Remark (!)



From Russia with Love…а с большим терпением

Total time = ?
(Estimate 6 months)

#	Task	Status	Timeline
1	Purchasing the components, elaboration of design and production of the set of boards by JINR	completed	Ready by 07.2022
2	Elaboration and approval of the Basis document (Addendum №2 to MoU_NICA_Wuhan) by both parties (JINR and CCNU) within JINR internal electronic document management system	completed	• started on 04.07.2022, • completed on 09.08.2022
3	Elaboration and approval of the set of documents (technical passport, service note documents, certified translation and copies) for the Export control group	completed	• started on 04.07.2022, • completed on 22.07.2022
4	Elaboration of the certificate of origin required by the Customs in Russia comprised of the following: 1.elaboration and approval of the contract between JINR and Chamber of Commerce and Industry – completed, 2.preparation / negotiation on details for the set of documents to apply for certificate based on rules from Chamber of Commerce – in-progress, 3.Signing the documents and getting the certificate of origin from the Chamber of Commerce	in-progress	• contract initiated on 23.08.2022 and completed on 04.10.2022, • the first remarks on documents received on 05.10.2022
5	Requesting the permission for the export from Customs in Russia on behalf of JINR with the set of documents from # 2 – 4	not started	•
6	Plan the flight and send the package to China	not started	•

Remark (!!)

It is necessary to have a permanent political support all the way and it should be coordinated at the level of JINR, if possible.

Special attention should be paid since the very beginning to key issues like **intellectual property** and **export licenses** in order to avoid repeating bad experiences from the recent past.

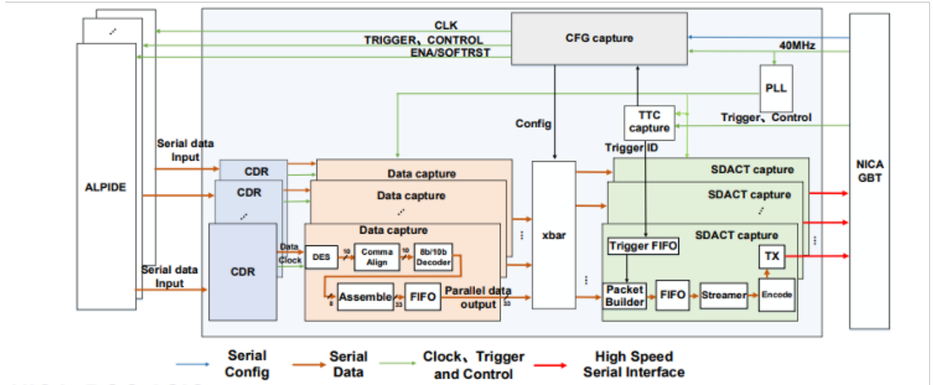
Conclusions

- The STS-Department has established collaborative links with specific Chinese scientific institutions.
- In addition to the current collaboration projects, there are clear proposals for future collaboration on the development and production of state-of-the-art microelectronics with a preliminary identification of our possible contribution to those projects.
- It is necessary to simplify the procedures for import/export from/to China, otherwise not a single serious project will be possible to be implemented in practice
- A strong and permanent political support will be essential to ensure that Russia will receive the expected benefits.

Thank you.

BackUp

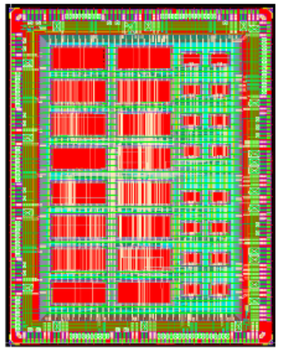
NICA_ROC ASIC Design



NICA_ROC ASIC

- **Design based on the self-defined interface and data format**
- Receives trigger/clock/control from NICA_GBT, and distributes to the front-end
- Receives and merges data from ALPIDE modules, reformats the data and send to NICA_GBT
- Receives trigger to reduce the number of events to transmit

Layout



- Areas：5.7 mm×4.5 mm
- Pins：247
- Package：QFP256

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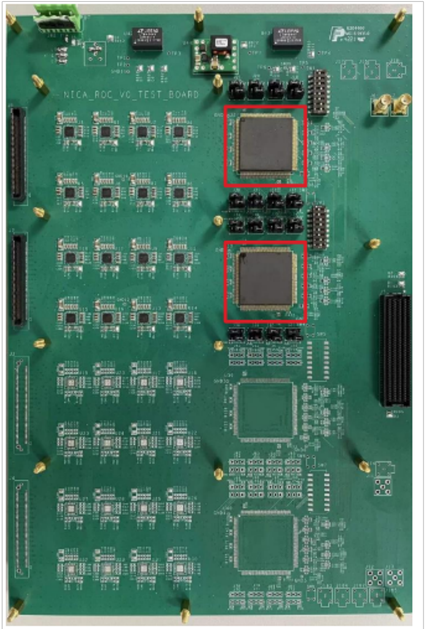
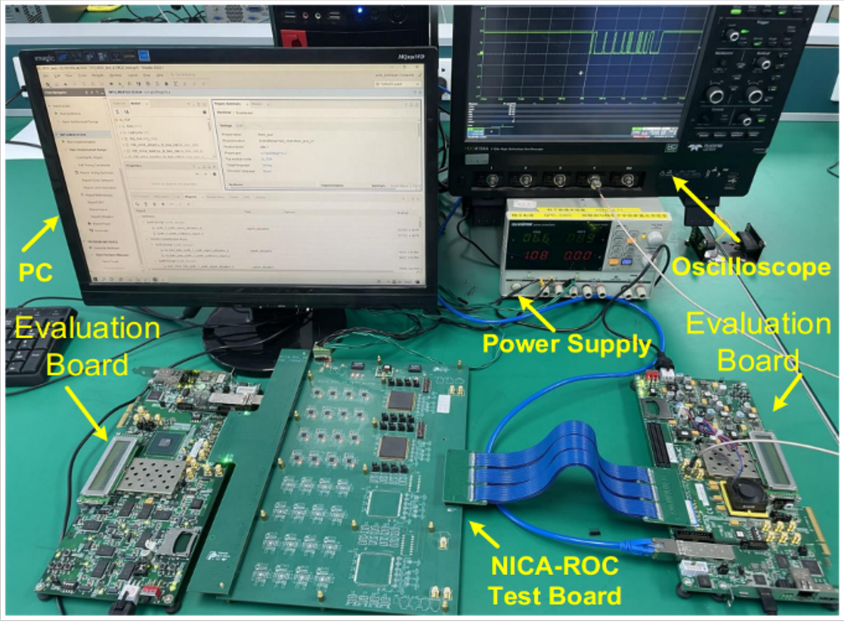
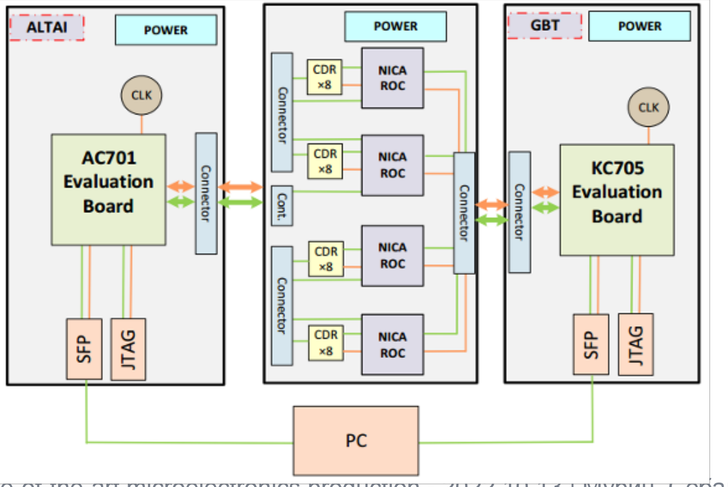


NICA ROC ASIC

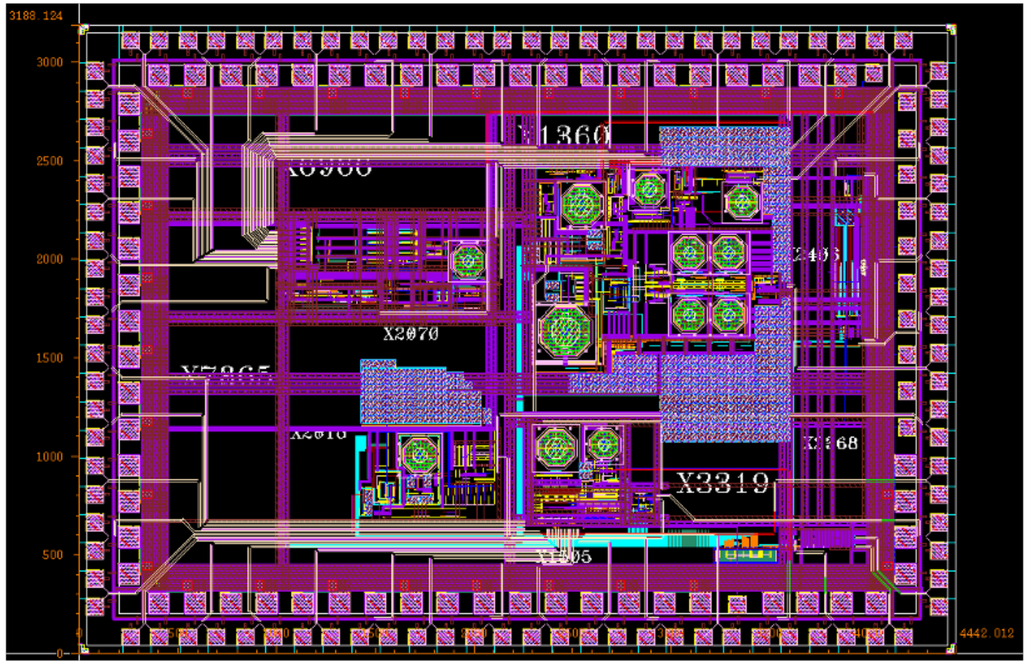
NICA_ROC test.



- The KC705 FPGA evaluation board act as a substitute for GBT ASIC.
- The AC701 evaluation board simulates ALTAI function to generate data.
- The control commands received by the A7 is decoded and sent to PC.
- Data loopback test to verify that the link logic is correct (Tx and Rx).
- Compare and analyze data transferred directly to PC with data in NICA_ROC format



NICA_GBT, NICA_LD and NICA_TIA ASIC



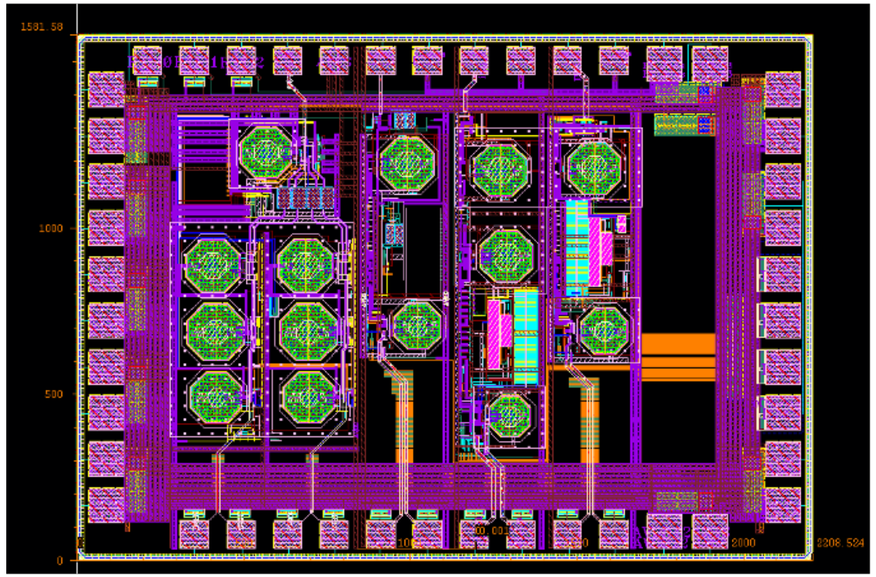
NICA_GBT_v1 overall layout

NICA_GBT_v1 includes the following sub-modules:

- **5.12Gbps/10.24 Gbps 16:1 Serializer**
- **2.56Gbps/10.24 Gbps 1:16 Deserializer**
- **2.56 Gbps/10.24 Gbps CDR**
- **5.12 GHz PLL**
- **Clock manager module**
- **160M/320M/640M/1.28Gbps Phase Aligner**
- **Up to 1.28 Gbps rail-to-rail Receiver(to front-end)**
- **10.24 Gbps three-tap pre-emphasis**

- NICA_GBT_v1: the first prototype version of NICA_GBT with full analog sub-modules.
- Total pins: 166
  Die size: 2880 x 4000 µm
  (Dimensions shown in the picture will shrink to 90%)
- Dual-row wire-bonding pads used in this version for test, and will be replaced by BGA package in the next run.
- Scheduled to be submitted on October 16th 2022, tested in March 2023.
- Digital function is under design and will be included in NICA_GBT_v2.

NICA_GBT, NICA_LD and NICA_TIA ASIC



NICA_LD and NICA_TIA overall layout

- NICA_LD and NICA_TIA designs are combined into one chip for test and verification.
- Die size: 1400 * 2000 µm
- Four independent channels. Two channels are laser driver designs and two channels are TIA designs.
- Different data-rate and power consumption versions.
- Scheduled to be submitted on October 16th 2022, tested in March 2023.

Joint Research Proposal

RSF-NSFC Cooperation: Possibility for Joint Russian-Chinese Project Proposals

2023-2025 Joint Project Description Template

A complete proposal in this competition consists of the joint project description (following this document) and the specific documents, necessary for both funding organizations respectively (for Chinese Scientists – following the NSFC rules, for Russian scientists – following the RSF competition documentation).
The proposal must be written in English. There is a strict limit of 20 pages for the joint project description (font size: 11 or 12, line spacing: 1.15). Applicants are obliged to ensure that the project description contains sufficient information for evaluation.

Core data

Title of the Research Project

Title in English: **Fast data processing through real-time AI for NICA/MPD and future EicC detectors**

Title in Russian: **Быстрая система обработки данных на основе ИИ в режиме реального времени для MPD и будущих экспериментов на EicC**

Title in Mandarin: **应用于 NICA/MPD 和未来 EicC 探测器上基于实时人工智能的快速数据处理**

Project Partners

Name and affiliation of the Chinese Principal Investigator
Name (in both English and Mandarin), title: **王亚平, Yaping Wang, Professor**
Host Institution: **Central China Normal University (CCNU)**
Contact telephone number and E-Mail address: **86-13697332703, wangyaping@mail.ccnu.edu.cn**

Name and affiliation of the Russian Principal Investigator
Name (including Patronymic name), title: **César Ceballos Sánchez, Staff Scientist**
Host institution: **Joint Institute for Nuclear Research (JINR)**
Contact telephone number and E-Mail address: **+7 9261486684, ceballos@jinr.ru**

Tasks

- Task 1 - Physics simulations, tracking and selective streaming system design and algorithm development: (1) Simulated data generation for selected physics; (2) Co-design of physics-aware artificial system to detect selected physics signal.
- Task 2 - AI model development based on Graphic Neural Network (GNN), and the GNNs are adopted for handling sparse detector images and identifying interesting tracks.
- Task 3 - FPGA board development for the Streaming AI Trigger System.
- Task 4 - Integrated selective streaming readout of the MPD/IT detector, the related electronics hardware development and the FPGA implementation of the machine learning algorithm.
- Task 5 – Built a standalone test station comprising the front-end electronics of MPD-ITS detector plus the streaming readout unit.

Partner A's work (China): Task 2, Task 3, Task 4.

Partner B's work (Russia): Task 1, Task 4, Task 5.