The Relevance of ATLAS experience and its relevance to the data acquisition of the BM@N experiment at NICA complex

> Kehinde Tomiwa kehinde.gbenga.tomiwa@cern.ch

On behalf of the HEP group University of the Witwatersrand Johannesburg SQM Conference 2015



OF THE WITH A THRSRAND

10HANNESBURG





Outline

- Introduction
- WITS HEP at ATLAS
- ATLAS TileCal Detector
- TileCal DAQ Architecture
- Towards Upgrade of ATLAS detector
- NICA Project
- BM@N Detector
- Connections between TileCal/BM@N/MPD detectors
- BM@N DAQ system
- BM@N DAQ Trigger overview
- BM@NData Flow
- Summary/Outlook



K.Tomiwa

1

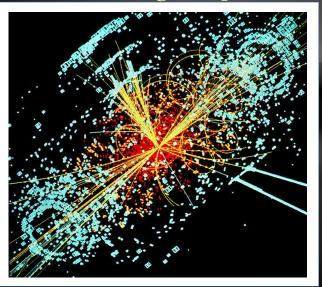
Introduction

Understanding the Universe



High energy Experiments

Collision/fixed target experiments



Experiments at LHC, proposed MPD/BM@N, etc comes with challenges. Big data.

Data processing rate (High frequency of acquisition). Way out. Development of High-throughput Electronics.

For data processing

Data reduction at maximum readout efficiency with no dead time

K.Tomiwa

WITS HEP at ATLAS

Wits HEP group has sustained effort at ATLAS in the following ways. Higgs Physics in Di-Photon Channel.

- Understanding the production of jets in association with the new boson.
- Search Higgs boson in the di-photon decay channel in associated with intermediate missing transverse energy.
- A Di-Higgs search in the yybb decay channel using ATLAS detector
- Search for additional bosons.

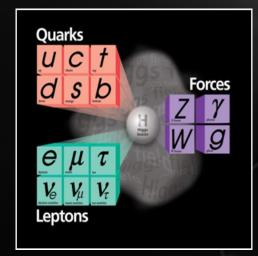
Electronics

Single Event Upset (SEU) and Reliability
Mobile Drawer integration checking (MobiDick) system for Tilecal Detector

•Super Readout Drivers (sROD) for TileCal Detector

The Grid

•Wits operates ATLAS Tier-3 site which comprise of over 100's CPU nodes.



K.Tomiwa

WITS HEP at ATLAS cont.

Computing

Massive affordable computing (MAC project)

- Development of modular ARM board,
- Cheap alternatives for high throughput super computing at high power efficiencies

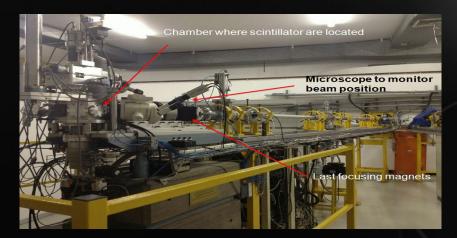
Material

Effects of ionizing radiation on plastic scintillators

Wits HEP group's Publications



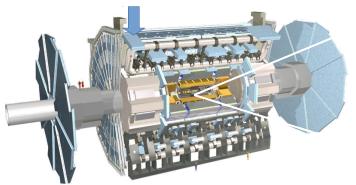
CERN data center

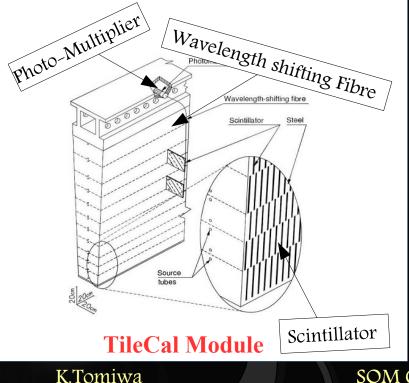


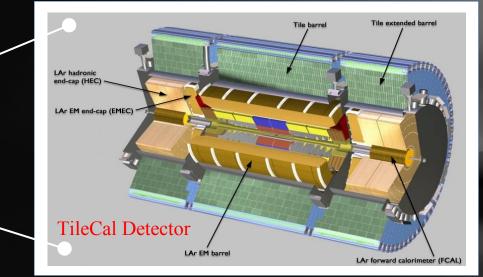
Scintillators study at iThemba Laboratory

ATLAS TileCal Detector

ATLAS Detector



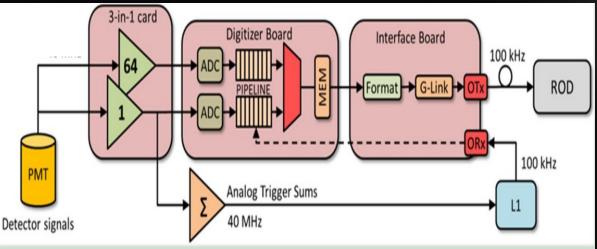




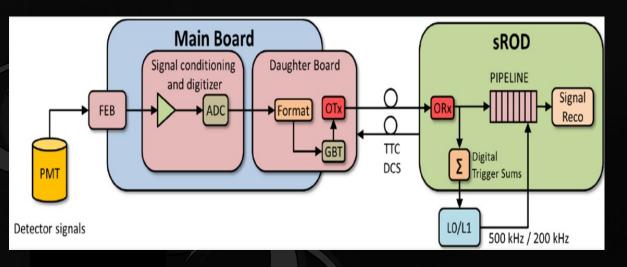
- Measure energy of Hadron and Jet.
- Uses steel absorber and plastic scintillating tiles as active materials
- Wavelength shifting fibres collect light to Photo-multiplier (PMTs).
- More than 10 000 channels.

TileCal DAQ Architecture

Current Architecture



Phase II Upgrade Architecture



-3-in-1: shaping, amplification and integration
-Motherboard: Programming, powering of FEE
Digitizer card: digitization and pipeline
-Interface board: 100KHz to ROD

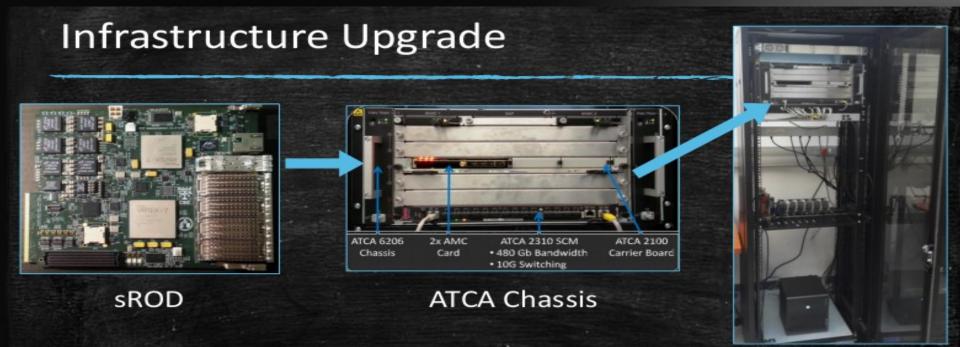
•Main-board.Shaping and digitization

•Daughter board: FPGA based board for formatting and data output to sROD at 40MHz

•SROD: Pipeline, monitors system functions and detector control

K.Tomiwa

Toward Upgrade of ATLAS detector Development ATCA system



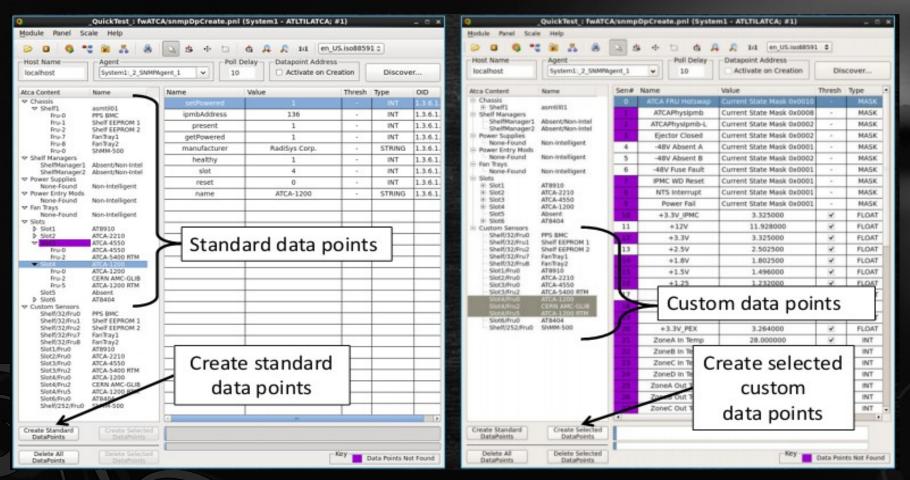
- ATCA replacement for VME Crates
- ATCA will house sROD and interface into the Detector Control System
- No software tools for this integration effort

| | Present | Phase II |
|-----------|-----------|------------------------|
| Total BW | ~165 Gbps | ~40 Tbps (+40 Tbps) |
| N. fibers | 256 | 4096 (+4096) |
| BW/drawer | 640 Mbps | 160 Gbps (+160 Gbps |

TileCal Bandwidth upgrade

Toward Upgrade of ATLAS detector cont.

Development ATCA system



Advantages of ATCA system

High Speed back-plane 10G 40GMonitoring and control

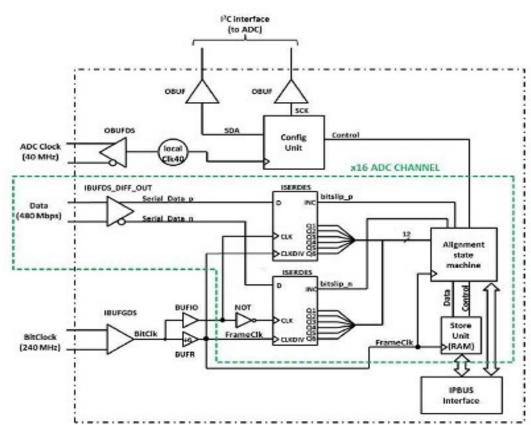
Hot Swapping
 <u>Re</u>dundancy

K.Tomiwa

Toward Upgrade of ATLAS detector cont. Development of ADC trigger board for PROMETOE of ATLAS TileCal

Architecture

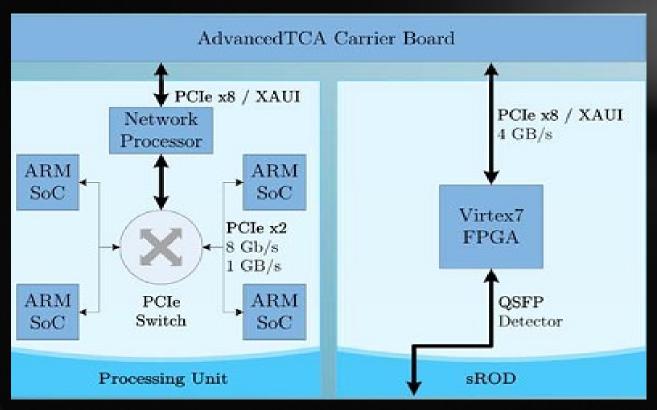
- Modules that are needed:
 - 16 x ADC readout cell
 - configuration unit
 - I2C interface
 - Send 40 MHz Clock (From ADC)
 - ADC and FPGA firmware running in the same clock domain
 - FIFO memories or IPBUS memories
 - State machines
 - Word and Bit Alignment
 - Control and Data Flow



K.Tomiwa

Toward Upgrade of ATLAS detector cont.

General purpose processing unit for the upgrade of TileCale



- PU is an ARM based cluster farm, proposed as co-processor to sROD
- Architecture enables efficient online data processing by ensuring high throughput
- Low latency by ensuring fast access to streaming data.

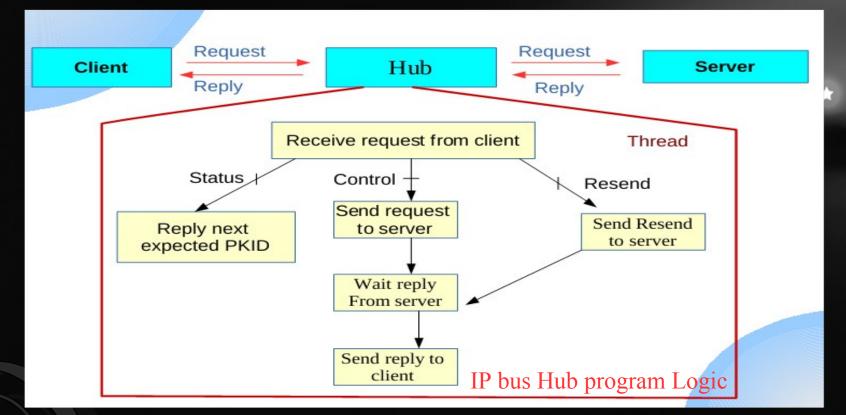
K.Tomiwa

SQM Conference $6^{th} - 11^{th}$ July 2015

1

Toward Upgrade of ATLAS detector cont.

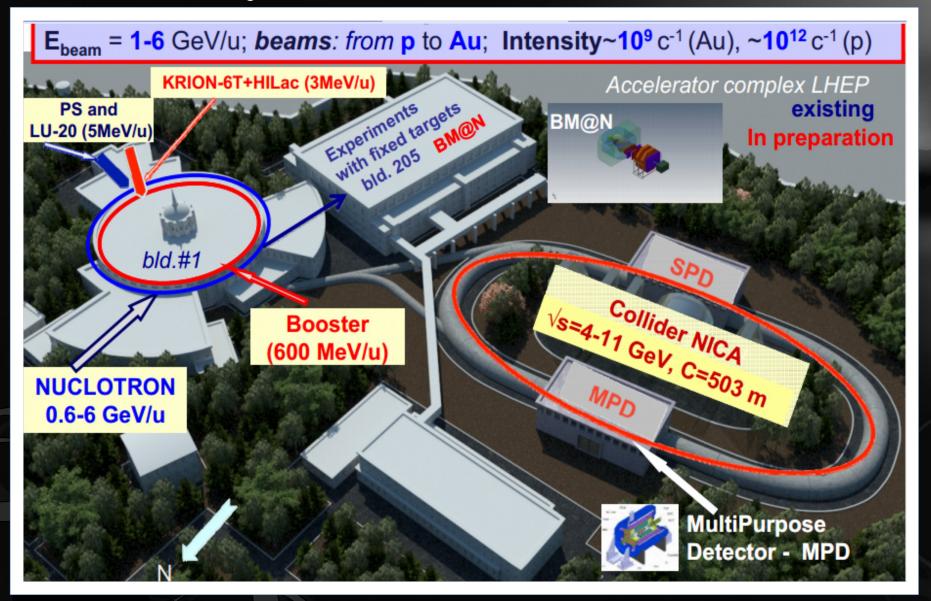
An IP bus protocol for ATLAS TileCal



- IP bus Hub is implemented in C++
- It is a software instance of packet manager

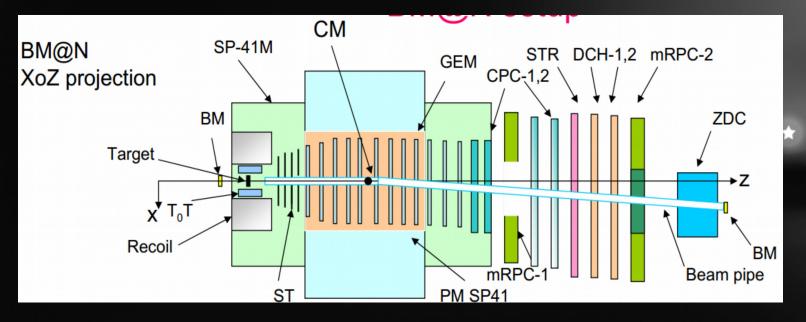
- Acts a mediator between single hardware device and multiple clients
- It allows simultaneous access to one device from one or more client applications

NICA Project



K.Tomiwa

BM@N detector



BM@N Schema

GEM → Gaseous Electron Multipliers

TOF \rightarrow Time of Flight Detector

 $TOT \rightarrow Fast Start Detector$

DCH \rightarrow Drift Chamber

Photo: BM@N project

K.Tomiwa

ZDC \rightarrow Zero Degree Calorimeter

CPC \rightarrow Cathode pad chamber

ECal → Electromagnetic Calorimeter

 $ST \rightarrow Straw$ tubes

Connections between TileCal/BM@N/MPD detectors

Systems were built to detect particles

Particle react with medium in the detector

Transfer energy in some recognized ways (e.g Energy loss in material

is a signature)

Systems were designed to measure particle interaction at high speed..

Systems require Detector readout electronics to shape, amplify and digitize signal produced by detectors medium.

Due to collision rate and volume output data, they rely on High throughput electronics for maximum readout efficiency.

High throughput electronics

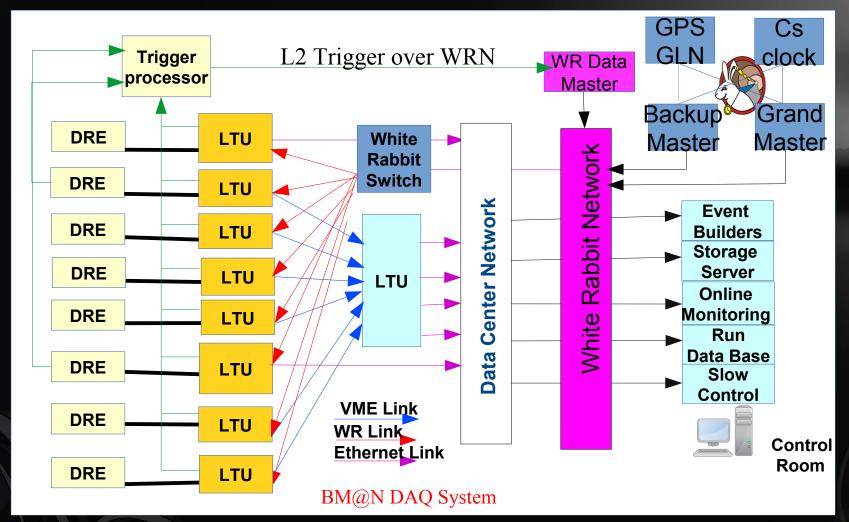
Maximum readout efficiency

No dead time with data selection and compression.

Reduces Large volume of data to scientific data with the help of fast and low latency triggers.

K.Tomiwa

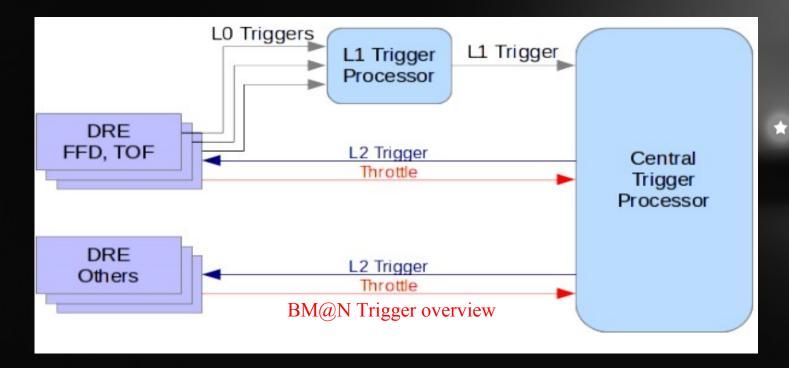
BM@N DAQ System



Detector Readout Electronics(DRE): Time-stamping Time to digital converter(TDC), Amplitude to digital converter (ADC) and TQDC discrete signal counter. **Local Trigger Unit(LTU)**: Trigger signal distributor.

K.Tomiwa

DAQ trigger overview

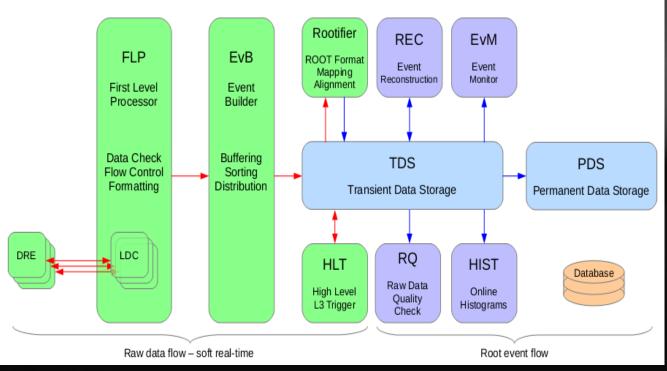


L1TP and CTP are Hardware based trigger

L1TP: Processes logical level 0 trigger signals to produce L1 trigger
CTP: Uses the Level 1 trigger to issue L2 trigger to the DAQ system.
Performs time-stamping of incoming L1 trigger signal.
Time reference by GPS/GLONASS receivers and Cesium clock

K.Tomiwa

Data Flow



BM@N Data flow

First Level Processor: Runs basis data check and reduction algorithm.

Zero Suppression waveform compression.

Wits Proposed A general purpose processing unit used with ATLAS sROD for FLP and EvB. (work in progress)

K.Tomiwa

SQM Conference $6^{\text{th}} - 11^{\text{th}}$ July 2015

. .

Summary/Outlook

Experiments to understand the universe produce big data with high event rate

High data throughput electronics are required.

To cope with event rate

To reduce data size to scientific data

Wits HEP group has sustained involvement in ATLAS Experiment

Detector Software development Physics analysis

Outlook

Development of general purpose ARM-based processing unit for BM@N DAQ system Contribution to physics analysis

Thanks for listening :)