Quality control and analysis of Si-planes FSD in the Xe-run

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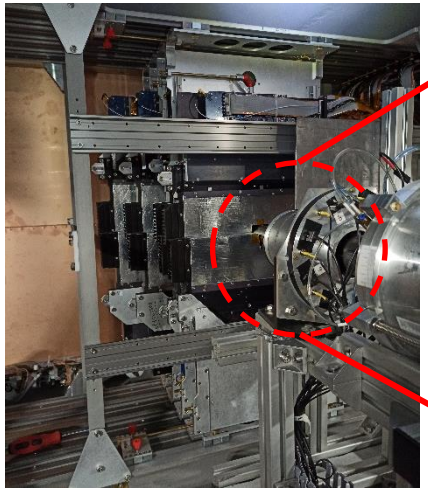
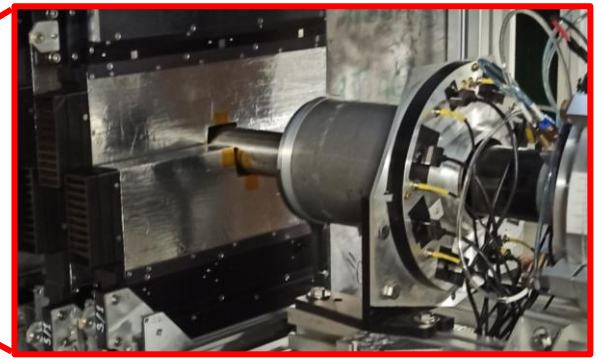
10th Collaboration Meeting
of the BM@N Experiment at the NICA Facility

16 May 2023

Forward Silicon Detectors Configuration (BM@N 2023 – Xe run)

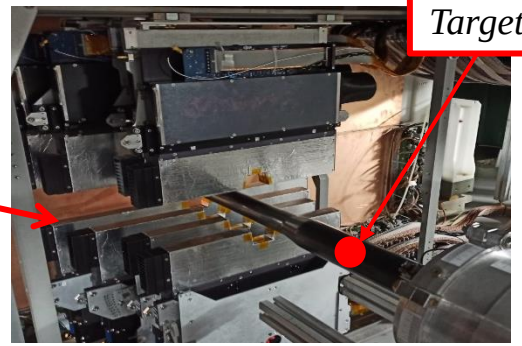




Barrel detector and target node

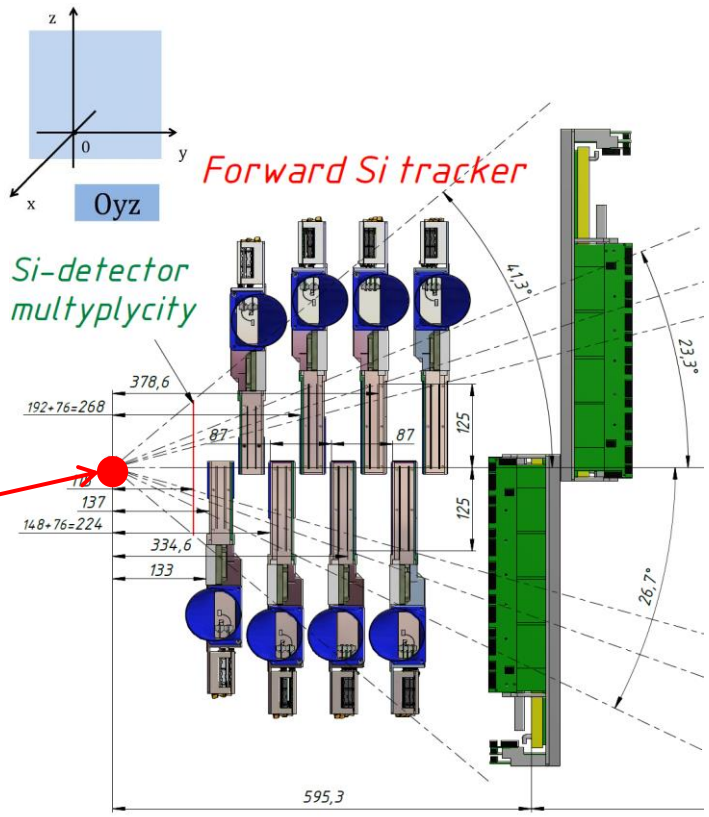
View of the FSD in the magnet SP-41 (working position)

Half plane view #3

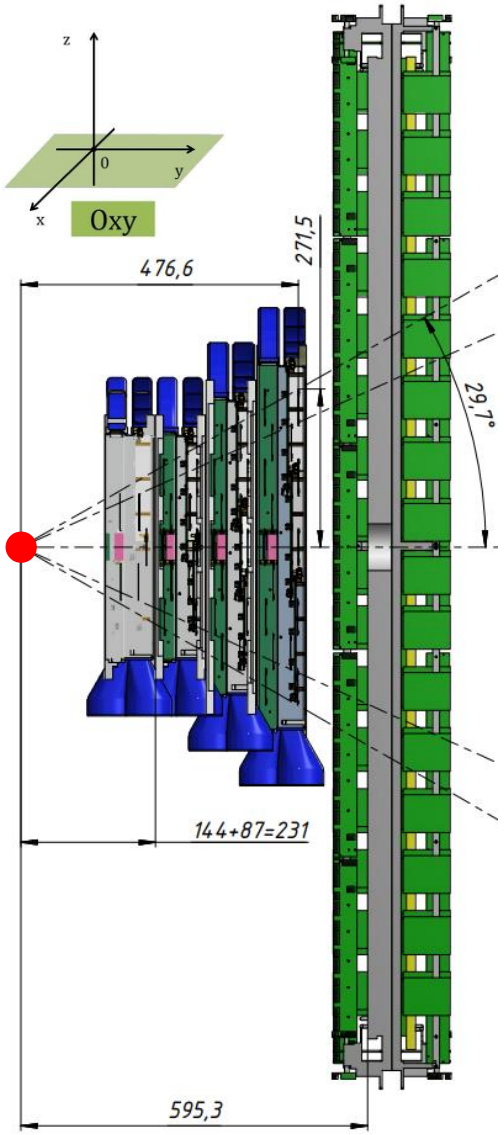


View of the FSD in the magnet SP-41

Target



Location of FSD planes in session 2023 (side OYZ)



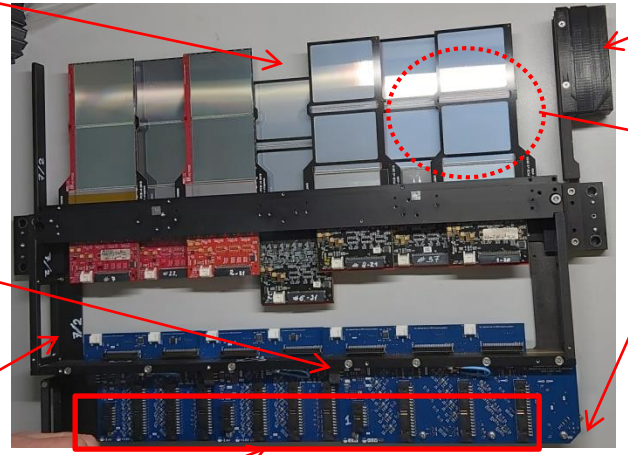
Location of FSD planes in session 2023 (side OXY)

Planes	#0	#1	#2	#3	Total
Modules	6	10	14	18	48
Channels	7680	12800	17920	23040	53760
Area, m^2	0,035	0,073	0,102	0,132	0,307

Silicon Detector Module

Beam pipe hole

Silicon half-plane with FEE



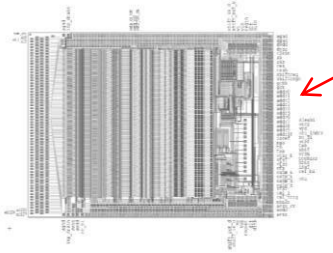
Cooling system output

LV input

Cooling system input

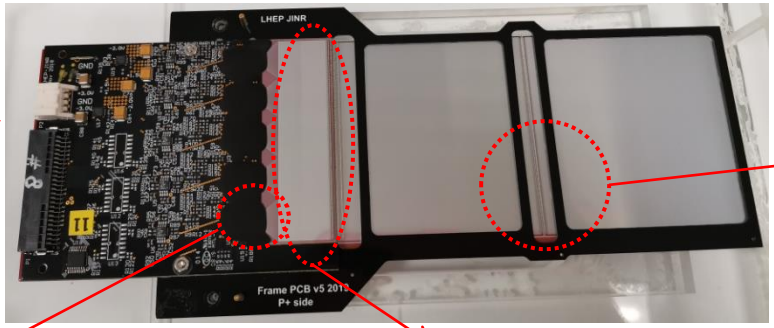
HV input

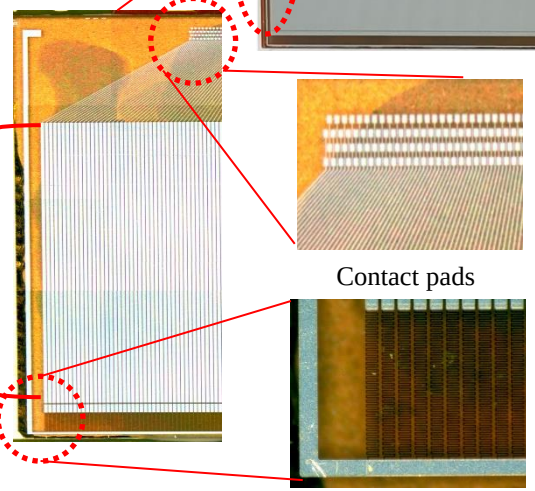
Outputs to DAQ



ASIC VATAGP7.2 (5 chips on each side of module)
Number of CSA: 128 channels
Dynamic range: ±30 fC
Peaking time (slow/fast shaper): 500 ns/ 50ns
Noise (ENC): 70e +12e/pF (typ.)
Voltage supply: +1,5 V, -2,0 V
Gain from input to output buffer: 16,5 μA/fC
Output Serial analog multiplexer clock speed: 3,9 MHz
Power dissipation per channel: 2,2 mW

Silicon Detector module (p+) side





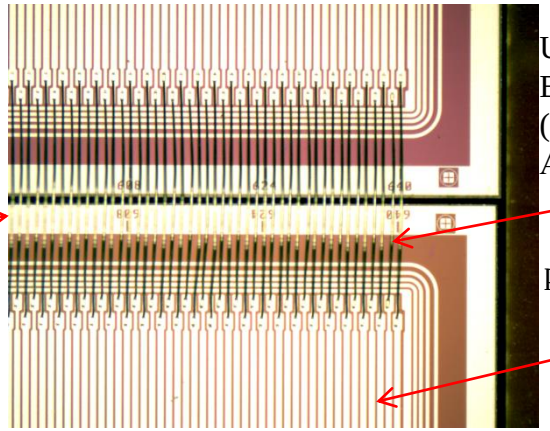
Capacitor

Contact pads

Value of poly-Si resistors

Pitch Adapter (n+) side
Number of channels: 640
Value of poly-Si resistors: ≈ 1 MΩ
Value of integrated capacitors: ≈ 120 pF
Capacitor working voltage: 100 V
Capacitor breakdown voltage: >150 V
Manufactured by ZNTC (Zelenograd)

63000 μm ± 15μm



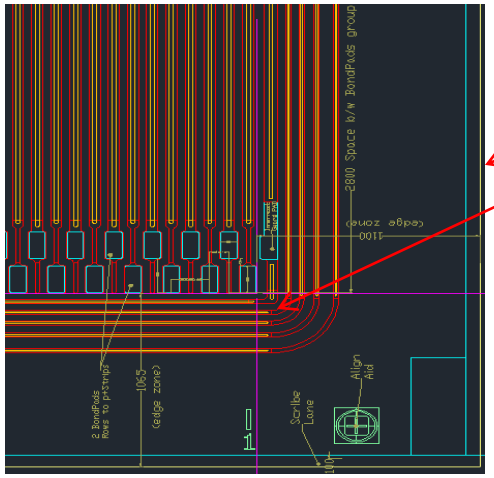
Ultrasonic Bonding (US- Bonding) Al wire Ø 25 μm

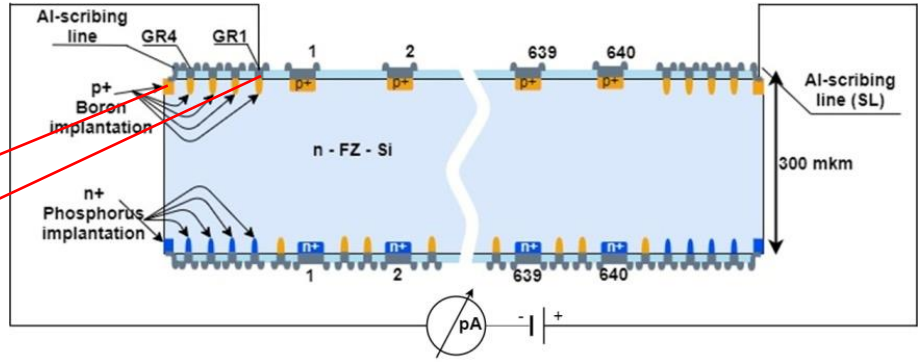
p^+ implantation region

Double sided Silicon detector (p+) side
Size: 63x63x0,3 mm^3 (on 4" – FZ-Si wafers)
Topology: double sided microstrip (DSSD) (DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 103 μm;
Stereo angle between p^+/n^+ strips: $2,5^0$
Number of strips: 640 (p^+)× 640(n^+)
Development by JINR, RIMST (Zelenograd)
Manufactured by RIMST (Zelenograd)

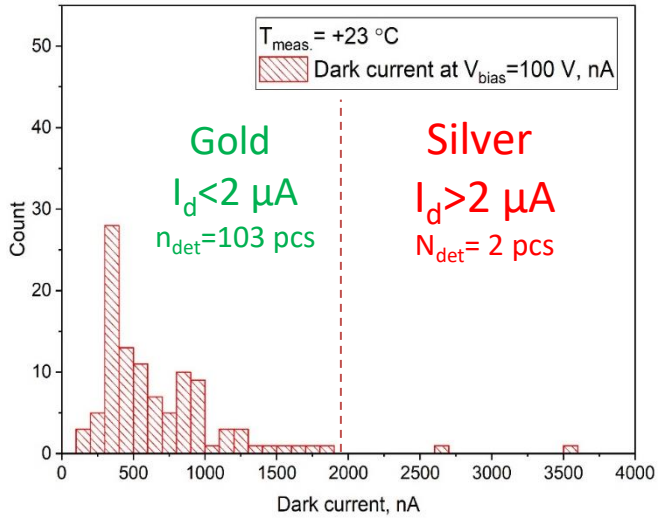
DSSD and Pitch Adapter tests

Basic parameters of DSSD 640×640 for Forward Silicon Tracker

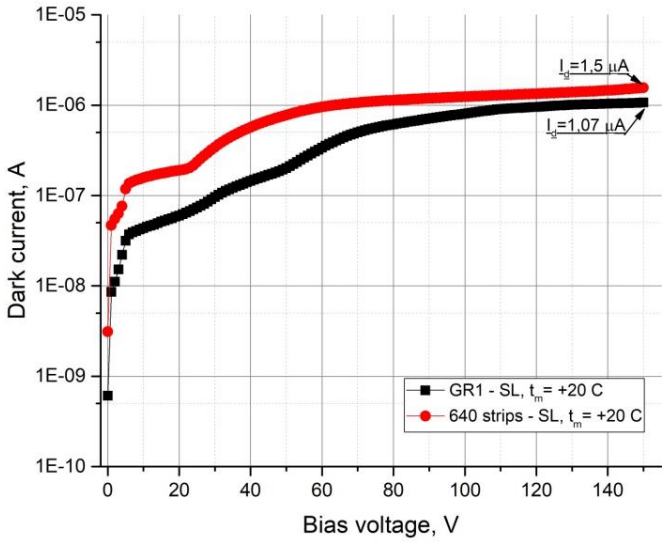




Measurement scheme of summary dark current by using first guard ring and scribing line

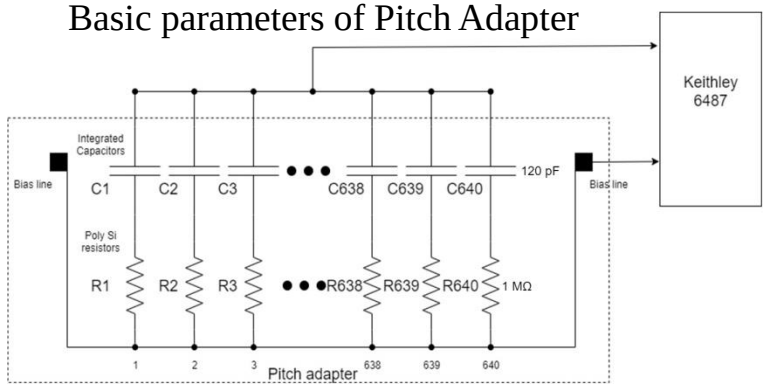


Summary DSSD's Dark Currents at V_{bias} = 100 V and t_m= +23 ºC, RIMST, Zelenograd

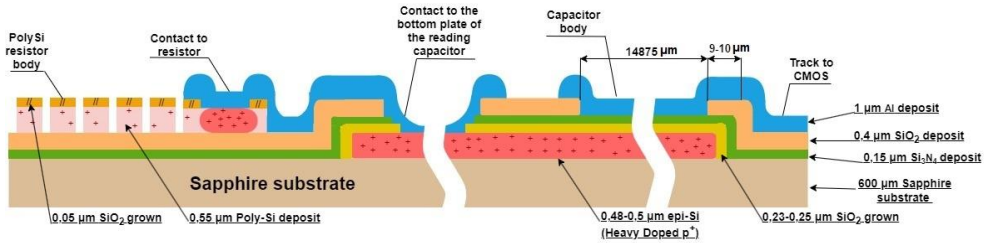


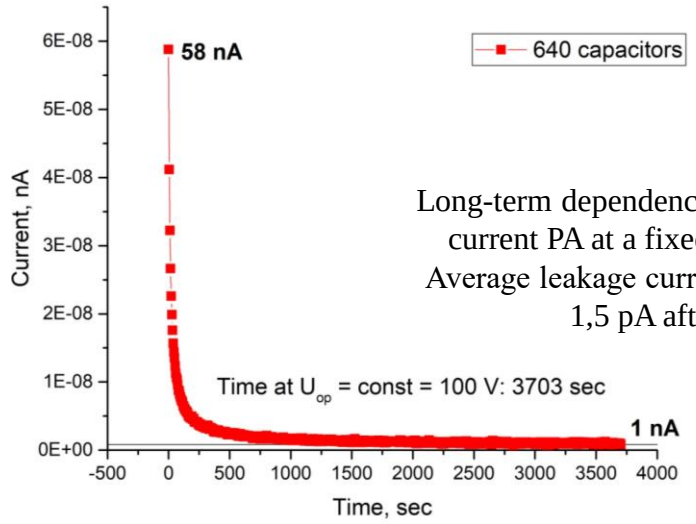
I-Vs for different measurement scheme, t = +20˚

Basic parameters of Pitch Adapter



Measurement scheme of summary leakage current





Long-term dependence of the total leakage current PA at a fixed voltage of 100 V
Average leakage current for 1 capacitor ≈ 1,5 pA after 1 hour

Stages of Assembly and Testing of the Silicon Coordinate Module

Assembly FEE PCBs with PAs

1 Assembly FEE PCBs with ASICs, testing

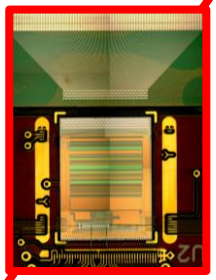
2 Ultrasonic bonding for Pitch Adapter and ASICs

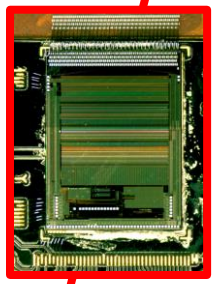
3 Filling ASICs and USB PA with compound

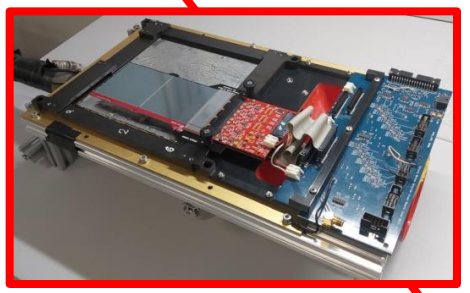
Testing the assembled FEE boards and writing the results to the database

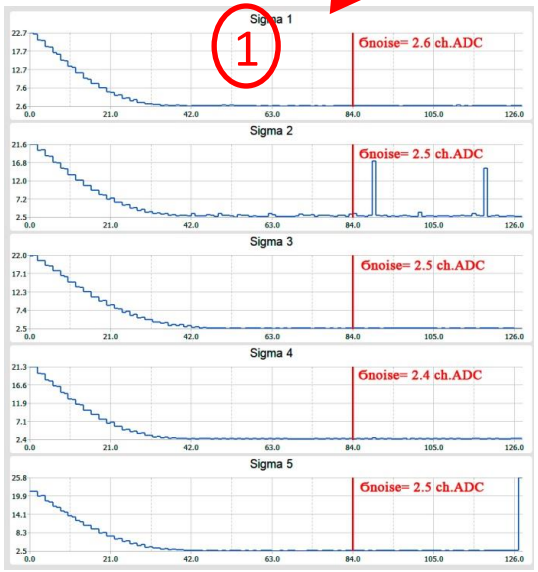
Assembly FEE boards with DSSDs (VBLHEP)

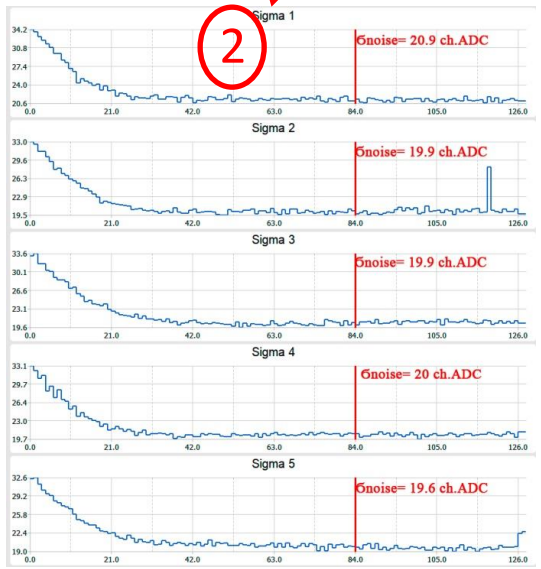
Module testing with β-source and write results to database

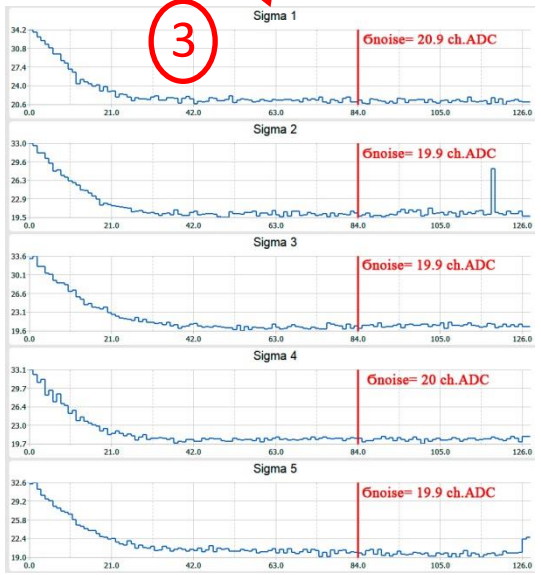


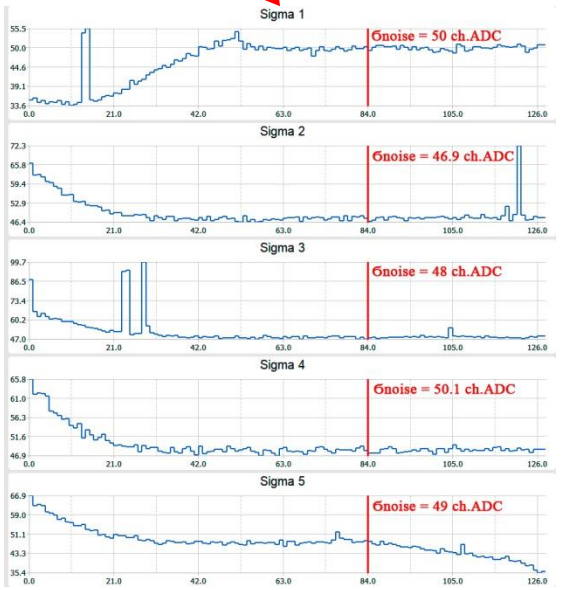












$б_{noise}$: C_{in}= 0 pF, I_{in}= 0 nA

$б_{noise}$: C_{in}= CR_{PA}, I_{in}= I_{PA}

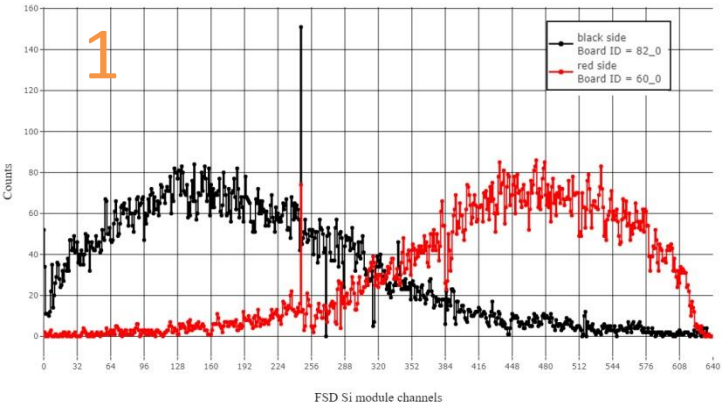
$б_{noise}$: C_{in}= CR_{PA}, I_{in}= I_{PA}+I_{encap}

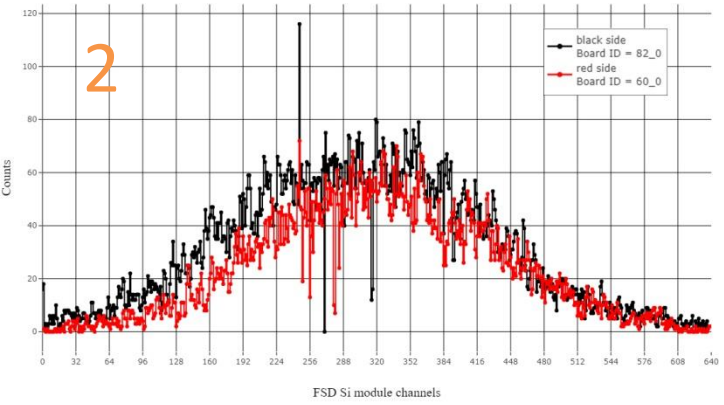
$б_{noise}$: C_{in}= CR_{PA}+ CR_{DSSD}, I_{in}= I_{DSSD} +I_{PA}+I_{encap}

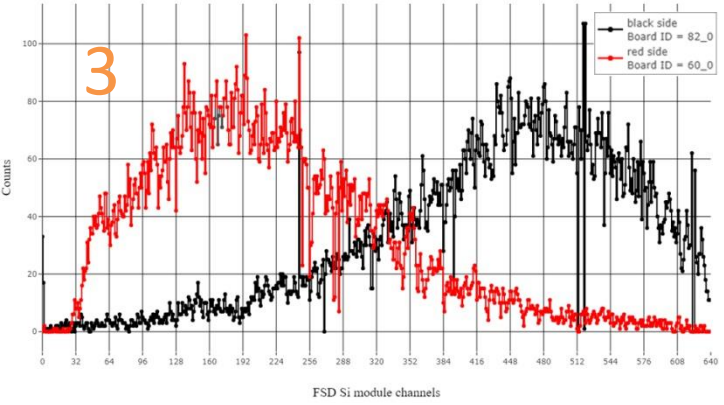
FST Si module test results

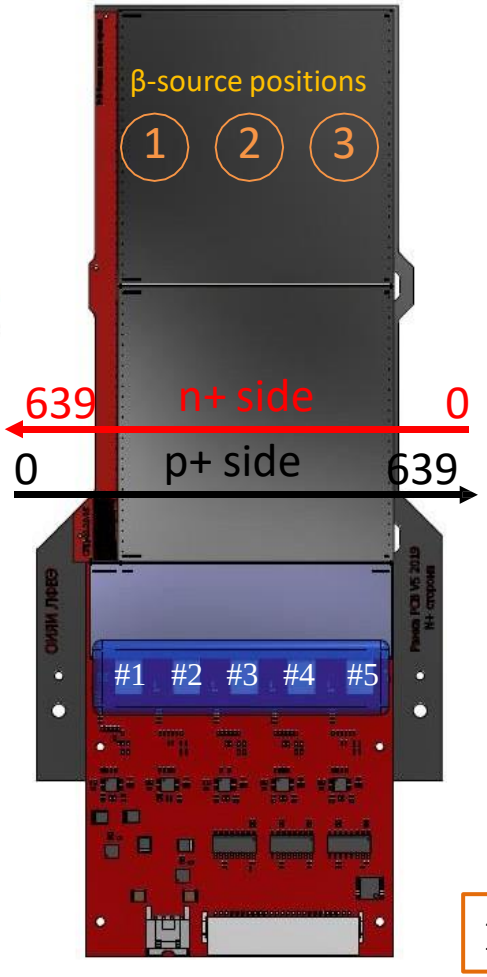
module #42

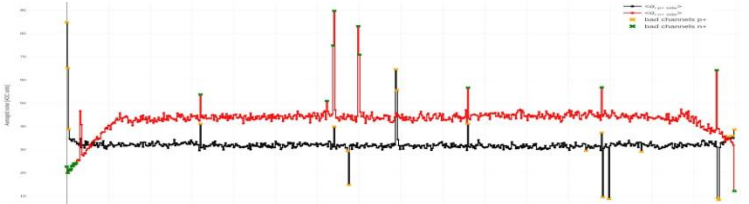
Occupancy distributions in FSD Si module channels after noise suppresion



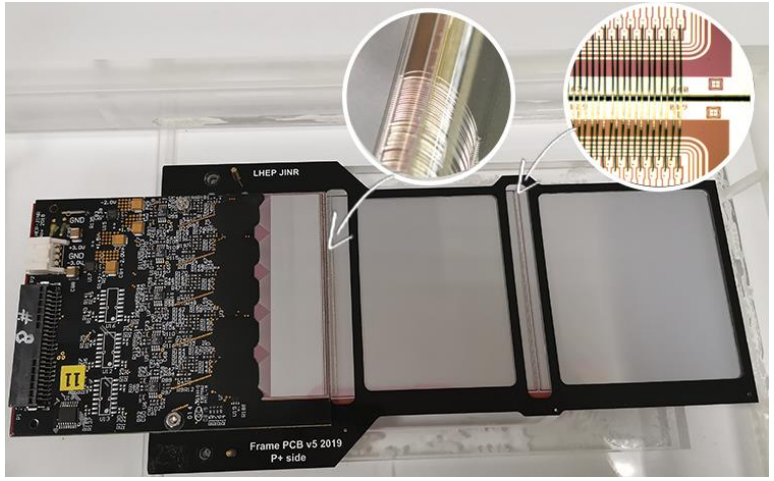






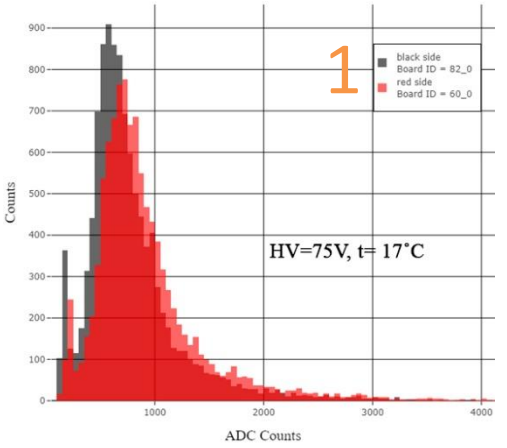


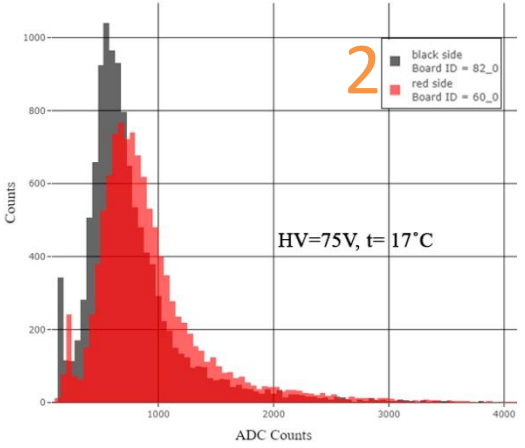
Sigma values of each FSD Si module channels at 75 V

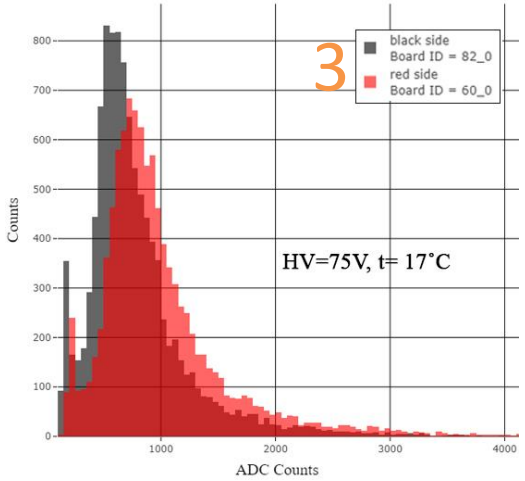


Module view after US- Bonding detectors and PAs, number of US- Bonding – 640, Ø Al wire – 25 μm

1ch. ADC_{p+} = 45 e 1 ch.ADC_{n+}= 42 e







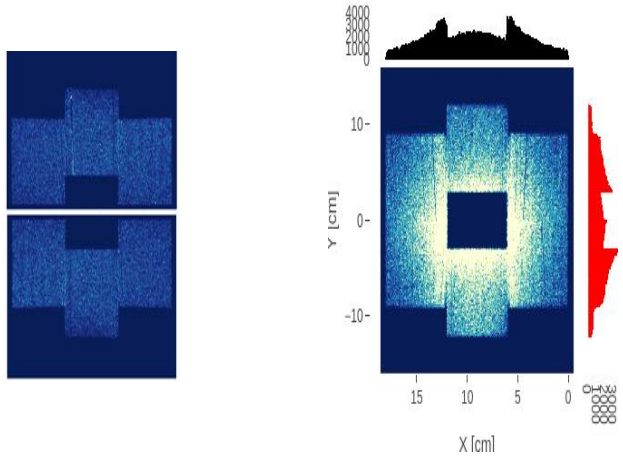
Module ID	Dark current (50V), nA	Mean noise ($^{+}$p), ch.ADC	Mean noise ($^{+}$n), ch.ADC	MPV ($^{+}$p), ch.ADC	MPV ($^{+}$n), ch.ADC	S/N p^{+} side	S/N n^{+} side	Bad channels ratio, %
42_0	3 584,00	36,93	50,76	536,20	578,89	14,09	13,32	0,55

Analysis of the work of Si-planes FSD in Xe-run

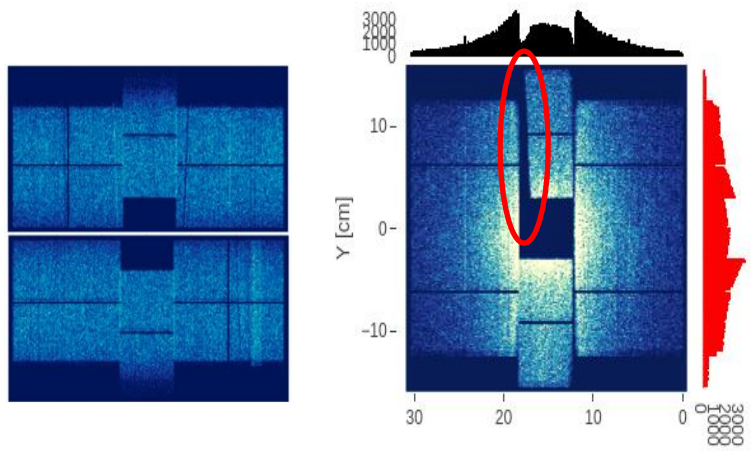
defects before BM@N session — defects after BM@N session

Cosmic tests

Session BM@N 2022 г. – 2023 г.
RUN 7529 (11.01.2023), t_c = 25,2°C
Target №2 CsI (2%)



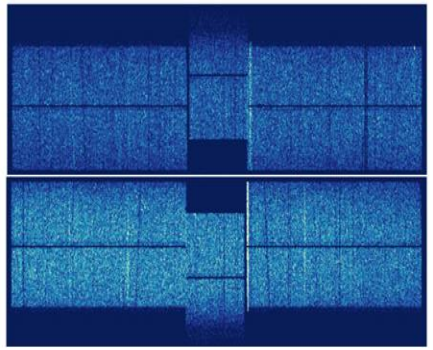
Hits distribution at Station # 0 (6 modules, DSSD 63x93 mm^2,
1 module = 1 DSSD) $I_{start/stop}$ = **8,99 / 8,21 µA (06.12 / 01.02)**

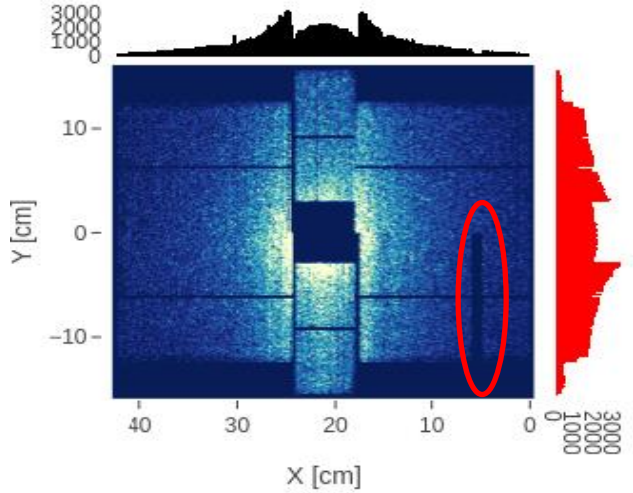


Hits distribution at Station # 1 (10 modules, DSSD 63x63 mm^2
1 module = 2 DSSD) $I_{start/stop}$ = **40,7 / 48,33 µA (06.12 / 01.02)**

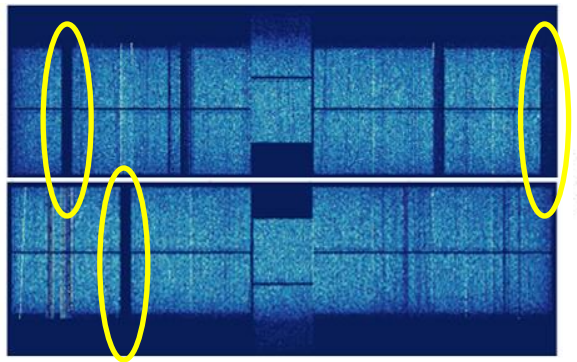
Cosmic tests

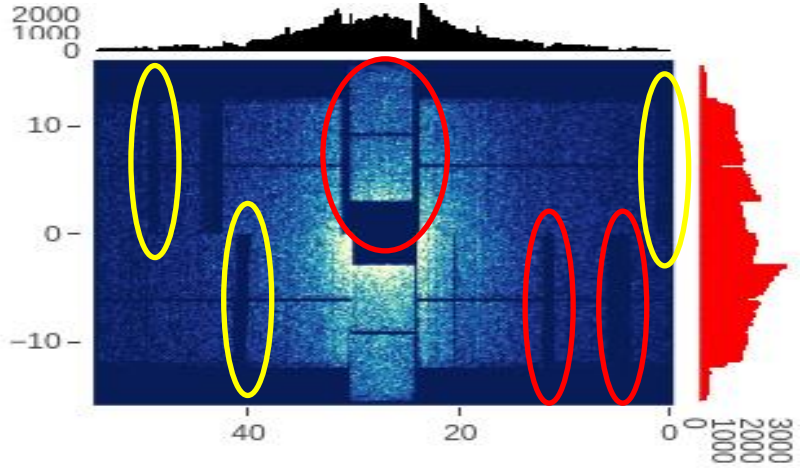
Session BM@N 2022 г. – 2023 г.
RUN 7529 (11.01.2023), t_c = 25,2°C
Target №2 CsI (2%)





Hits distribution at Station # 2 (14 modules, DSSD 63x63 mm^2
1 module = 2 DSSD) , $I_{start/stop}$ = **27,6 / 28,5 µA (06.12 /01.02)**





Hits distribution at Station # 3 (18 modules DSSD 63x63 mm^2
1 module = 2 DSSD) $I_{start/stop}$ = **6,9 / 7,38 µA (06.12 /01.02)**

Conclusion

Eliminate dead zones (sized 128 channels) in coordinate planes

Backup slides

Conclusion

Results

+All FSD planes worked stably in the BM@N-2023 session:

- No thermal breakdown of detectors;
- No electrical breakdown of PAs;
- Stable operation of the reading electronics;

+ According to the analysis of dark currents, the detectors received a minimal amount of radiation damage and can be used in the next session BM@N;

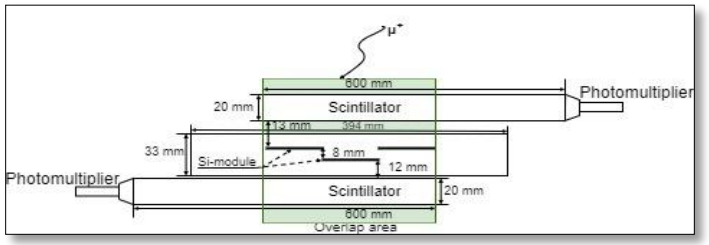
Plans

•Elimination of dead zones:

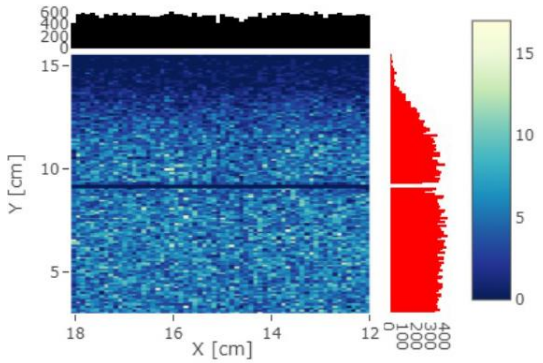
- Re-testing PCBs that did not pass the initial selection for installation in the module;
- Building new modules.

FST Si module test results

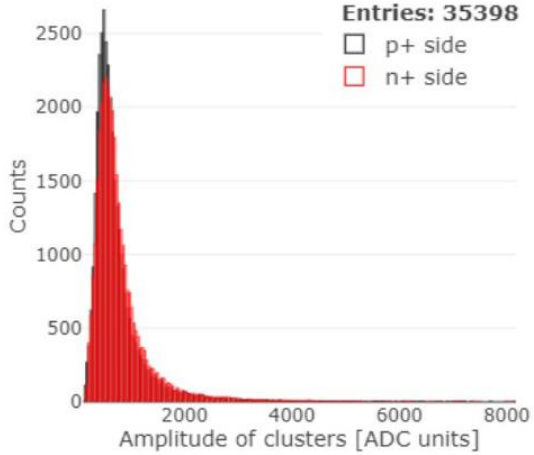
Cosmic test



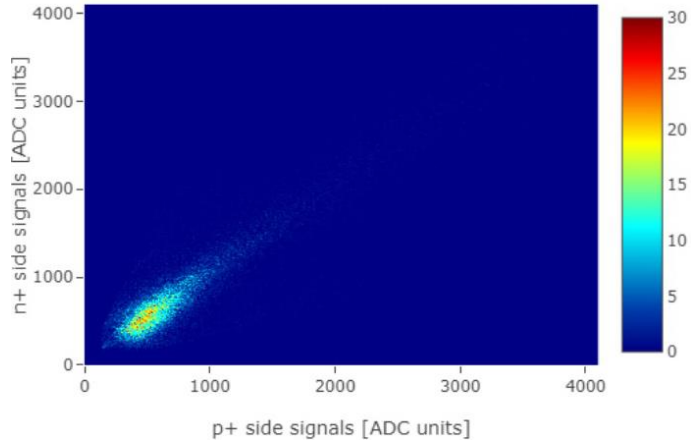
Hits distribution



Amplitude of clusters distributions



Correlation plot



Xe run BM@N, 2023