# Status of the STS project

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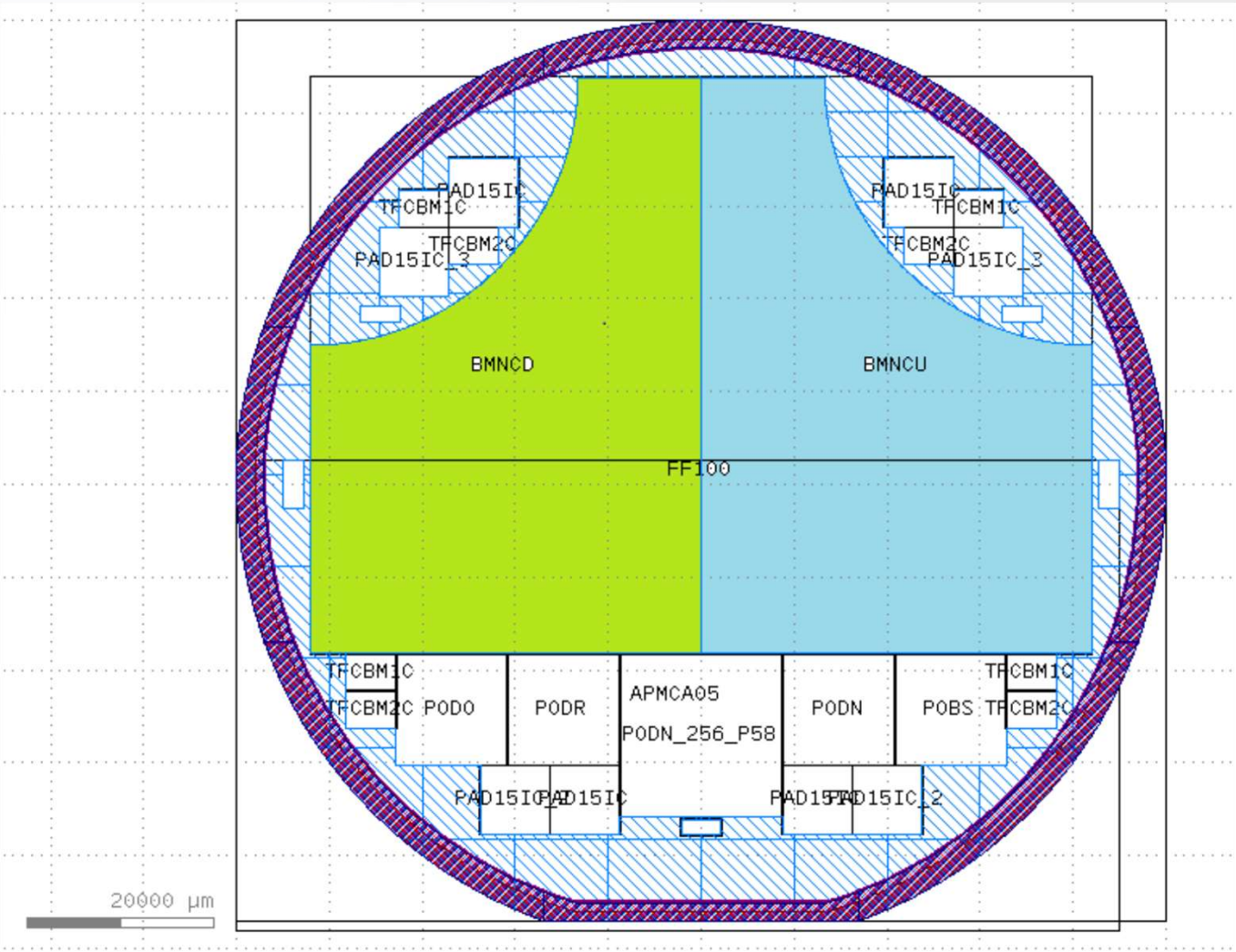
# Status of STS Components

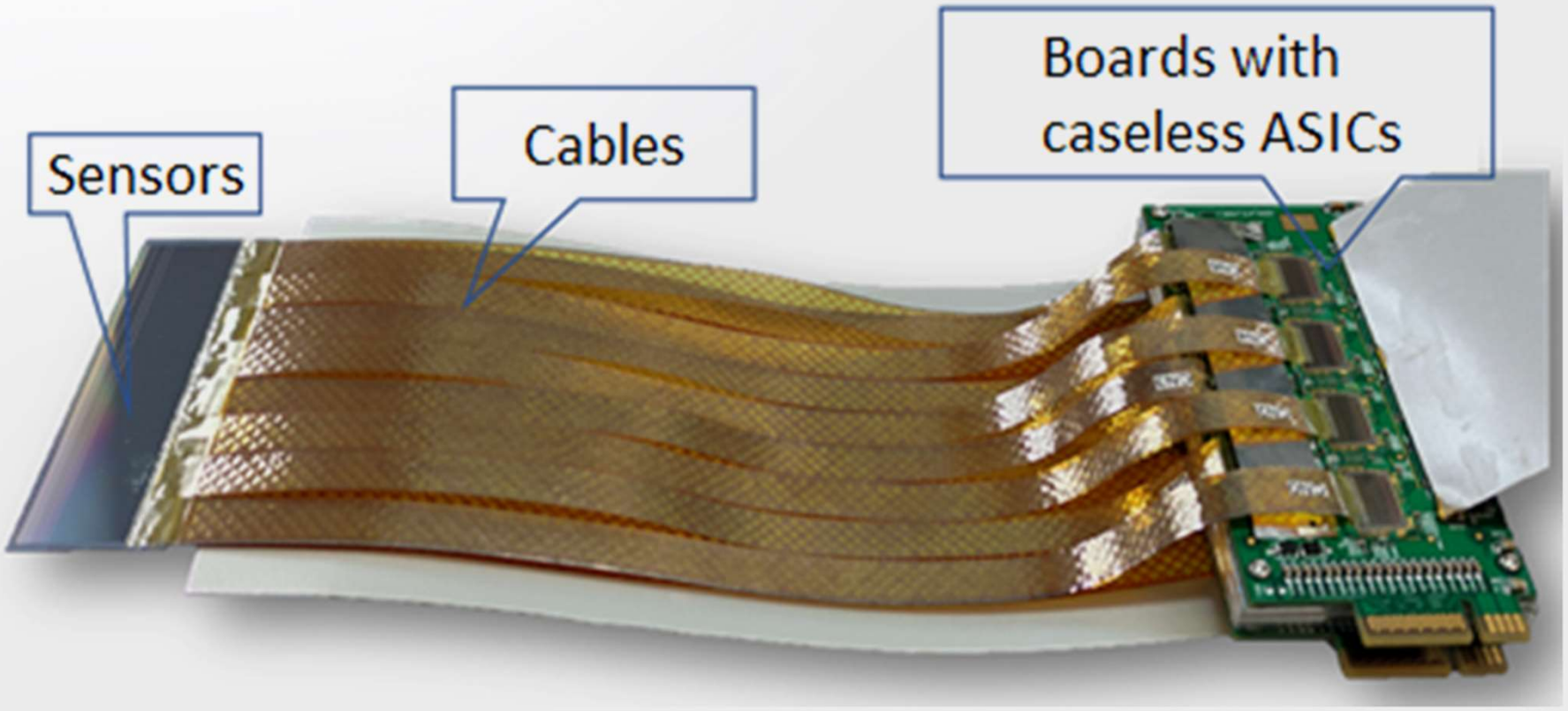
- Sensors
- Low mass cables
- ASICs

# Sensors

Sensors for central part of ladders – totally we need 16 sensors with specific geometry.



# Low mass cables



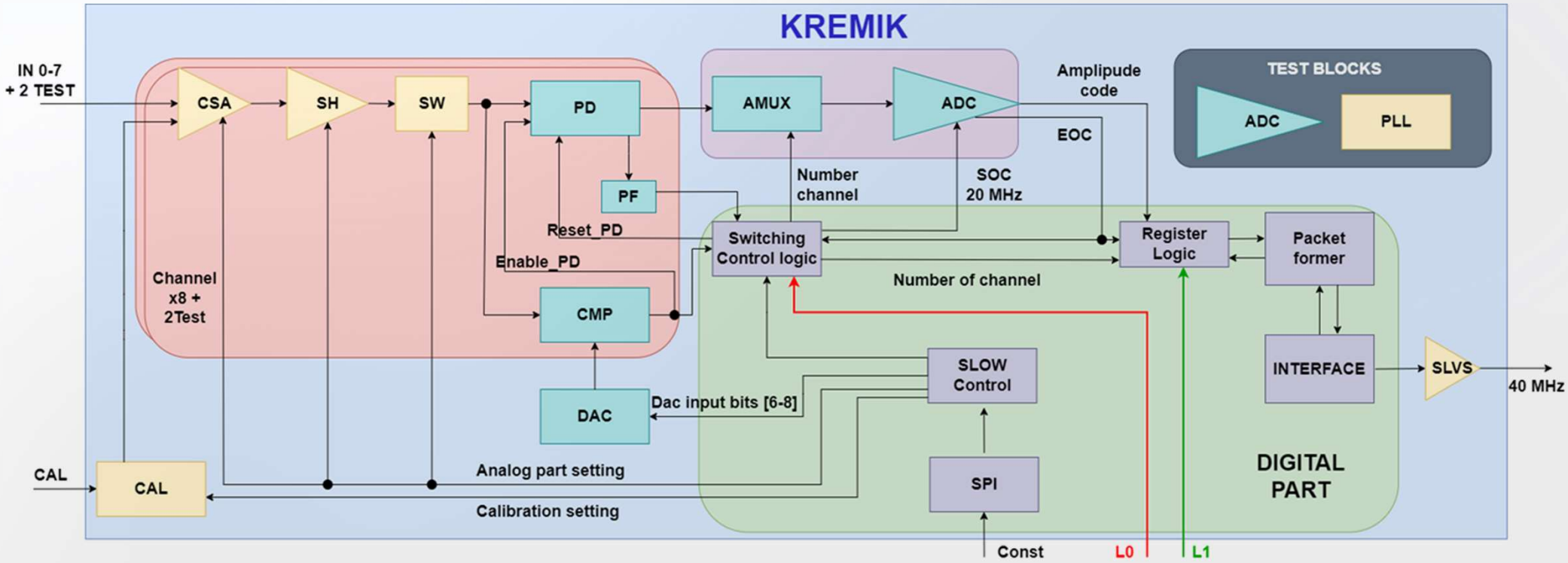
# ASIC

- Specifications
- Block diagram
- Chronograms
- Analog front-end
- Mixed-signal part
- Digital part
- Outcomes

# Chip Specifications

- The prototype version must process signals with a maximum frequency of 100 kHz. It will use 2 triggers: L0 one at a frequency of 100 kHz with a signal arrival delay of up to 500 ns and L1 – at a frequency of 50 kHz having a signal arrival delay of up to 10 μs
- Input signals of both polarities (electrons & holes)
- Dynamic Range up to 30 MIPs (108 fC)
- Typical input amplitude 1 MIP (3.6 fC)
- ENC at detector capacitances ranging 10-30pF < 1500 el
- Channel rate < 1 kHz (> 1 ms per event)
- Programmable shaping time 200, 300 & 500 ns
- Channel peak amplitude detection & 10 bit ADC
- Prototype ASIC size 5 x 5 $mm^2$
- Forecast on power consumption for final chip version (128 chs.) < 600 mW

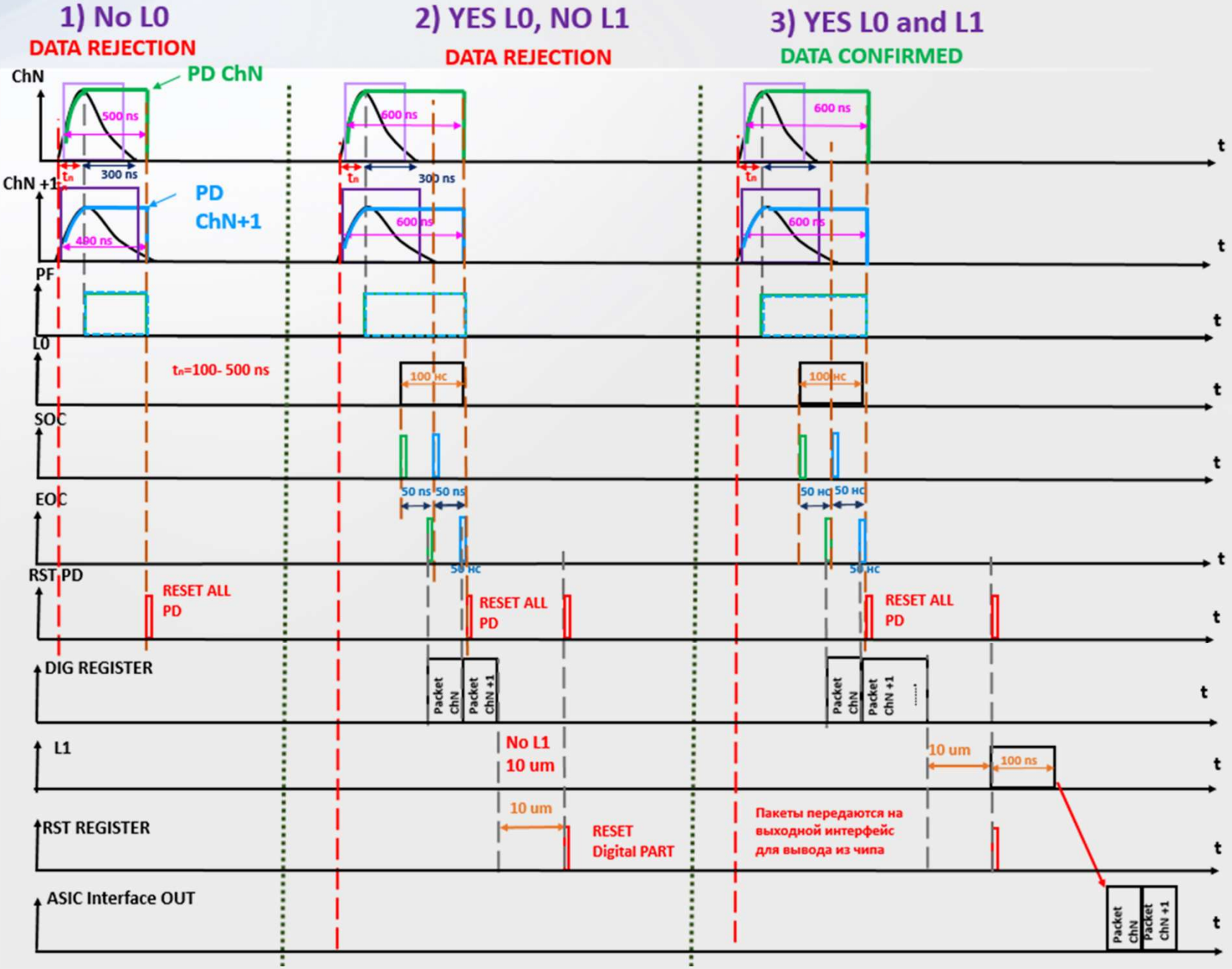
# Block diagram of prototype



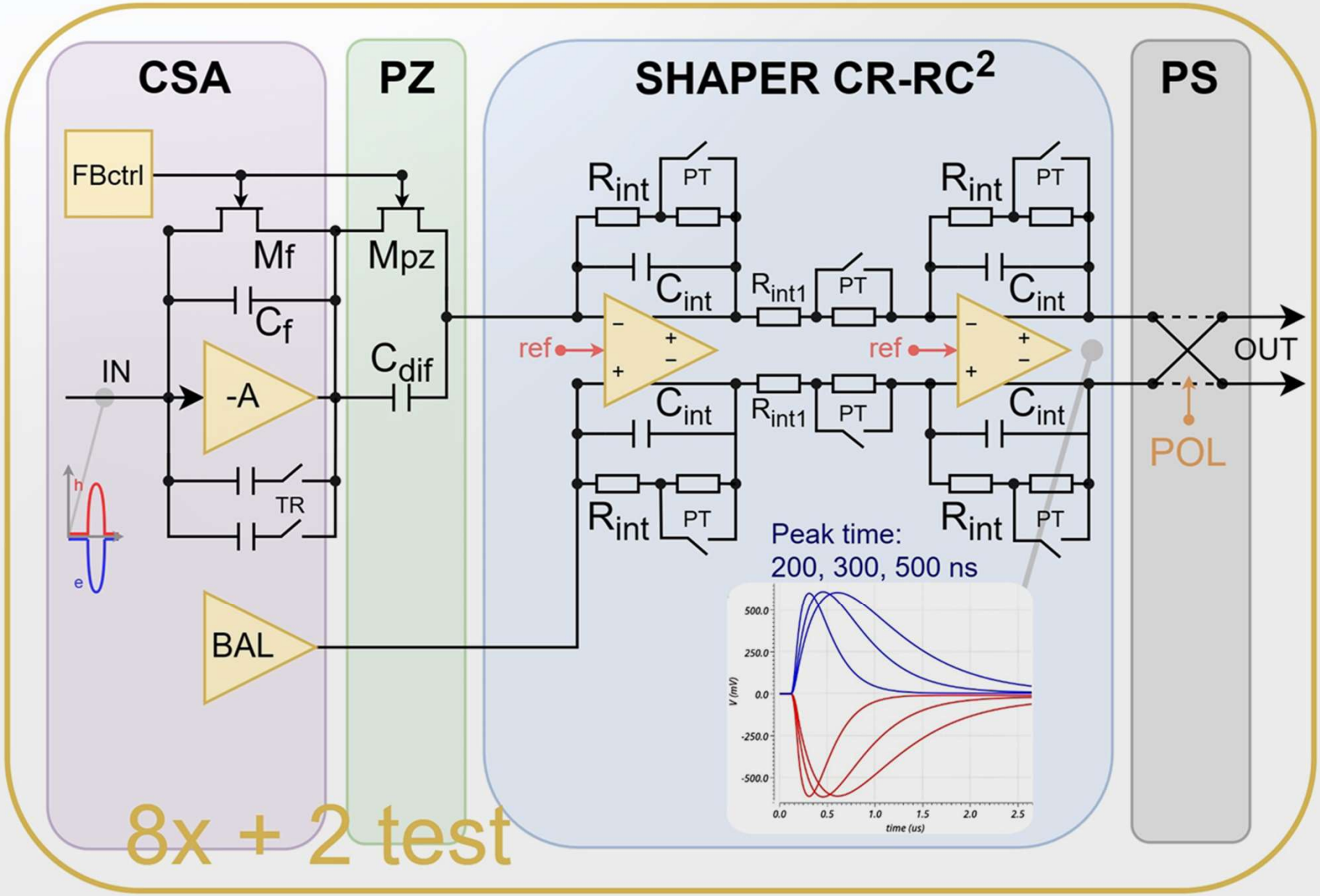

MAIN parts:

- Analog front-end
- Mixed signal (analog & digital)
- Digital
- Supporting blocks for: calibration, control (parameter set), trimming, lab tests, backup solutions

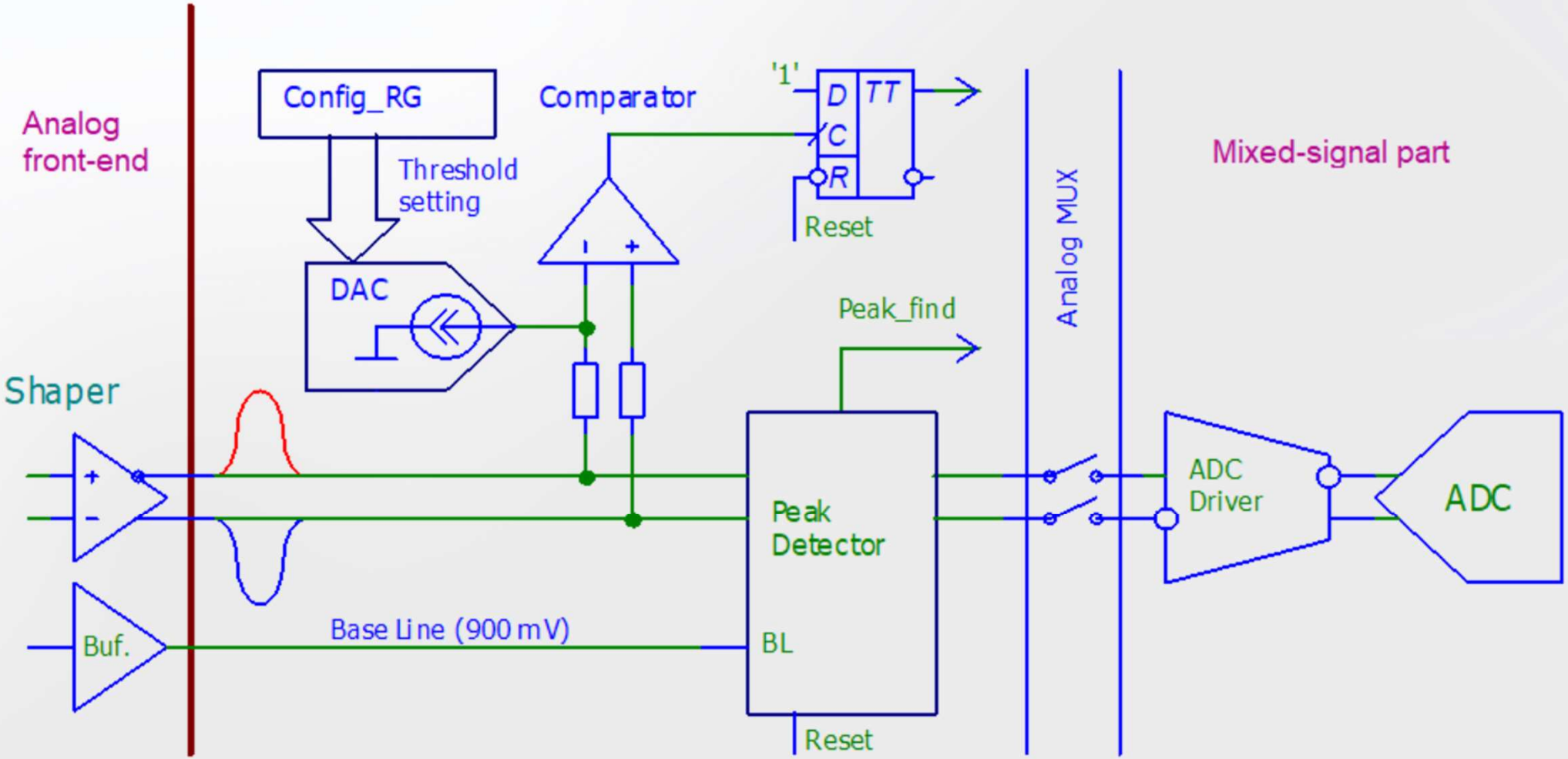
# Typical signal chronograms



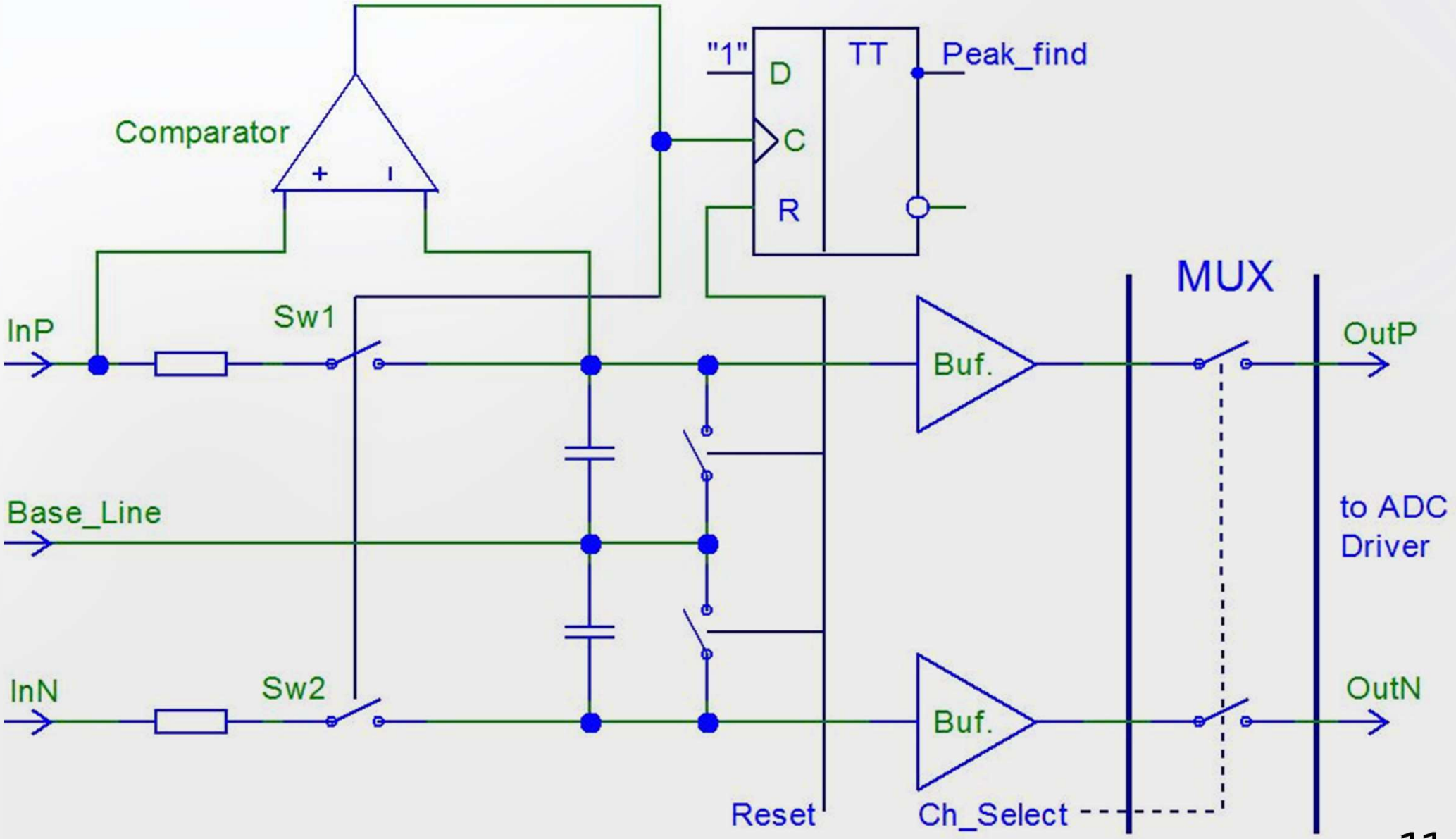
# Analog front-end



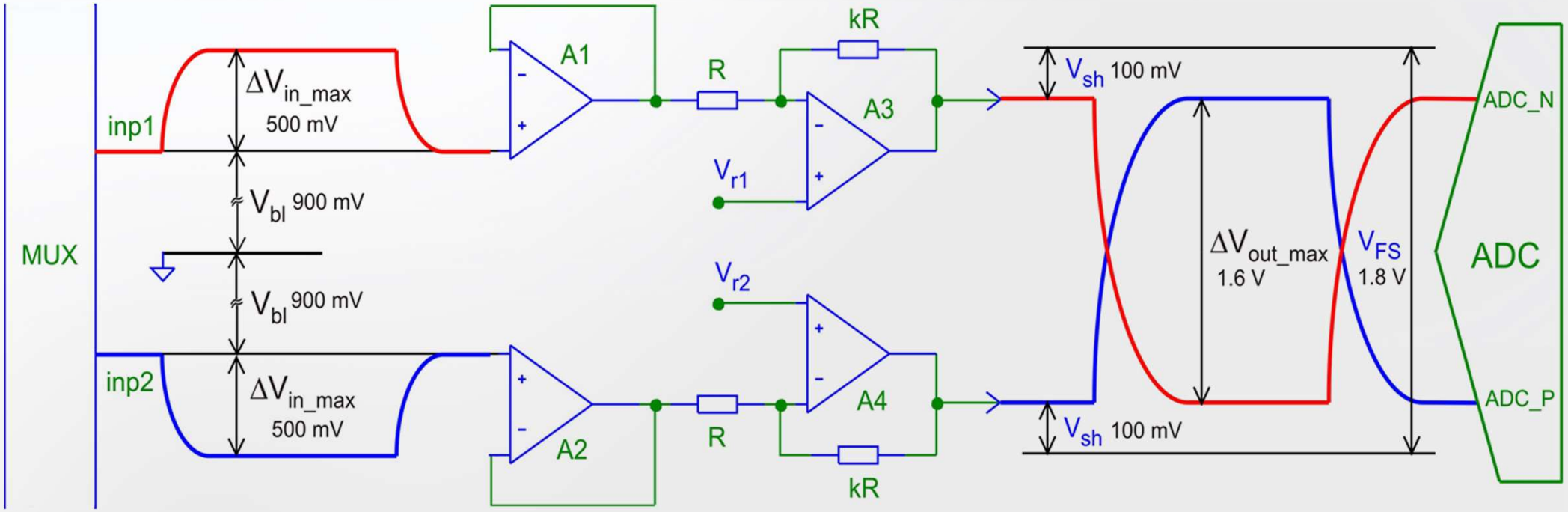
# Mixed-signal part

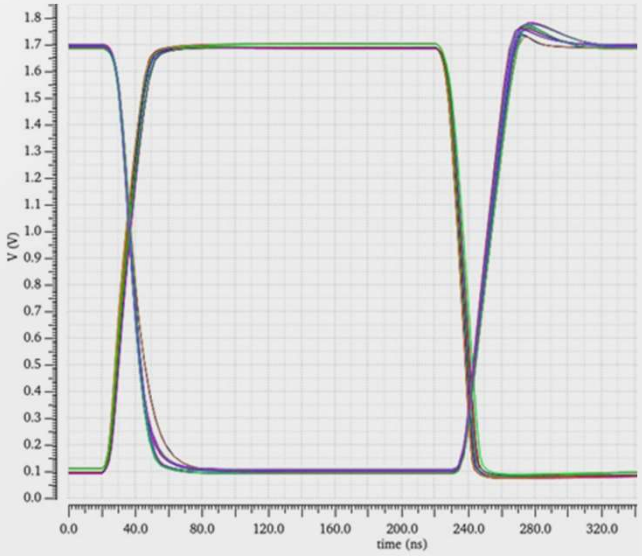


# Peak Detector



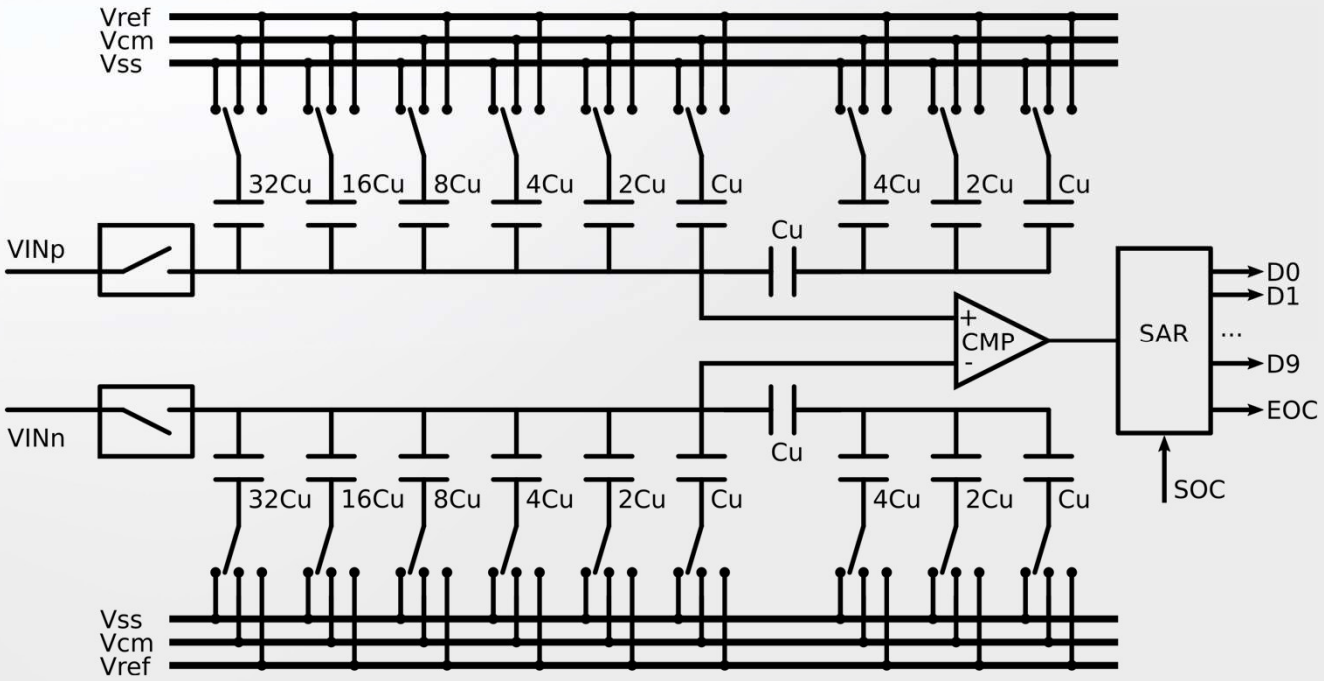
# ADC Driver



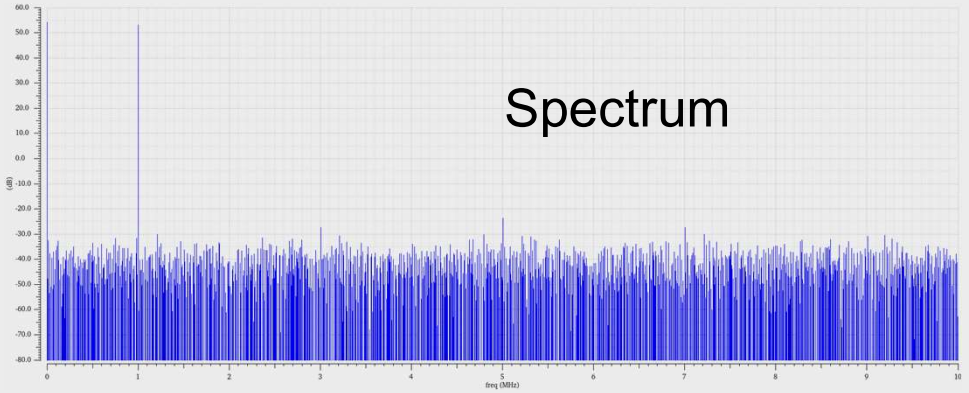




An example of timing diagrams at the driver outputs when a signal with an amplitude of 500 mV is applied to its input.

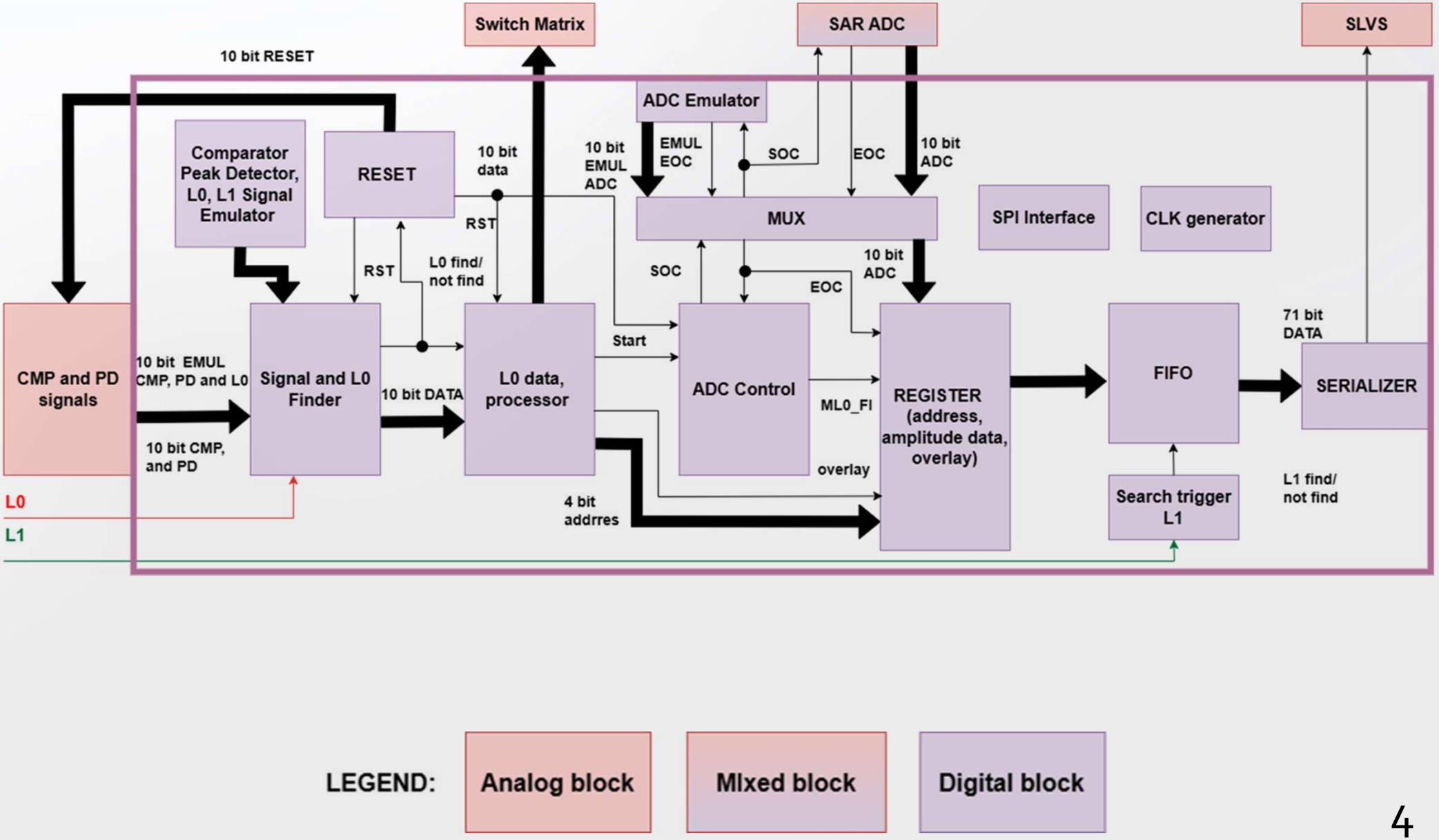
# ADC structure and simulation results




- Self-clocked SAR ADC
- Resolution – 10 bits
- Conversion time – 40 ns
- ENOB@20MHz – 9.7 LSB
- Power consumption – 2 mW



# Digital part



# Outcomes and plans

- Design of the first prototype ASIC (10 channel) for silicon tracker is underway
- Deadline for submission of the GDSII file for prototyping (tapeout for 180 nm CMOS process)  is July 2023
- JINR contract for manufacturing of first batch of chips (50+ pcs) is in negociation phase with Chinese MPW integrator company
- Fabrication and in parallel measuring testbench development will be done in 6 months. The first lab functionality results are expected to be made in early 2024