

Система считывания света в жидком аргоне модульной ТРС ближнего детектора эксперимента DUNE

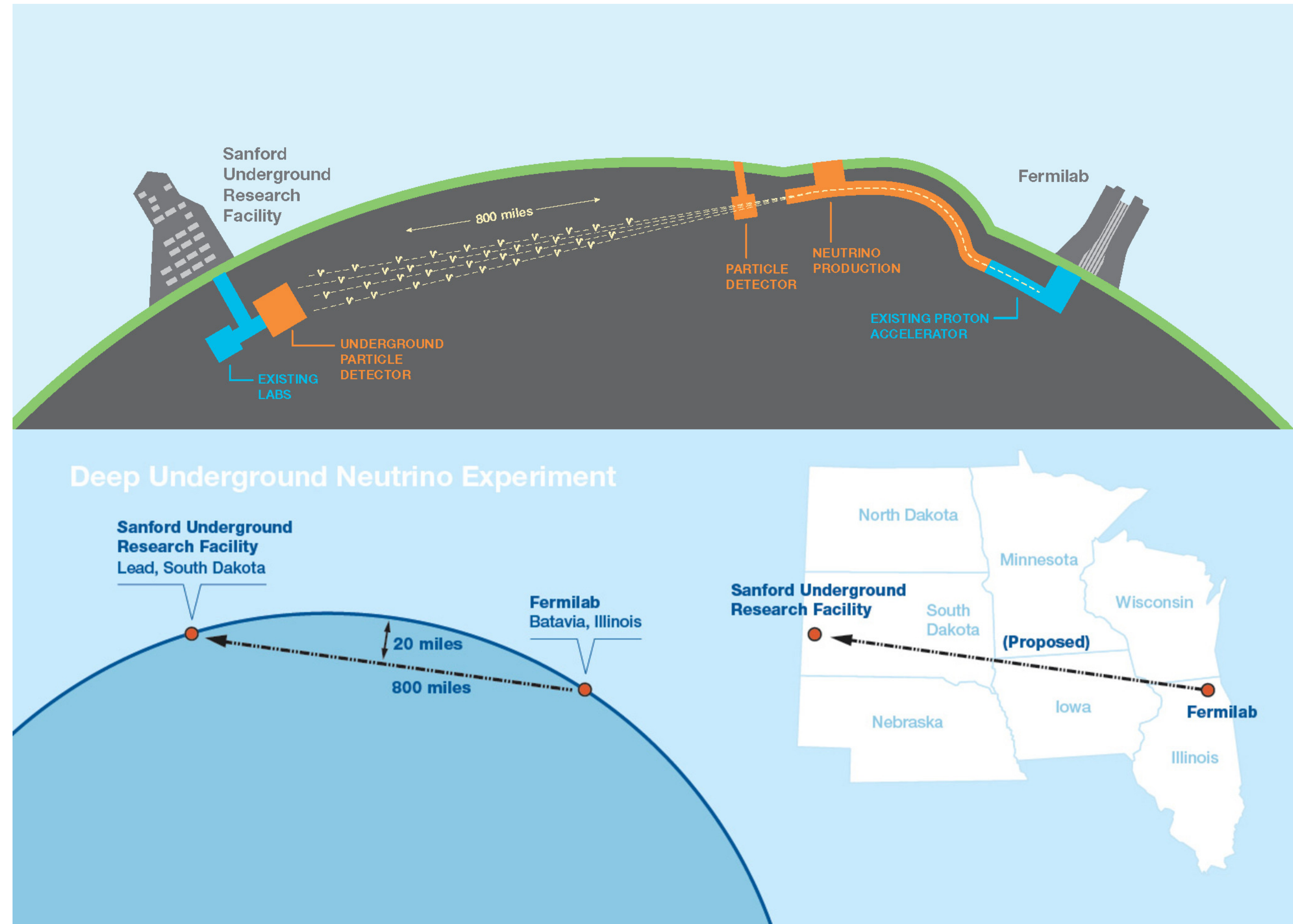
Научно-методический семинар ЛЯП

Содержание

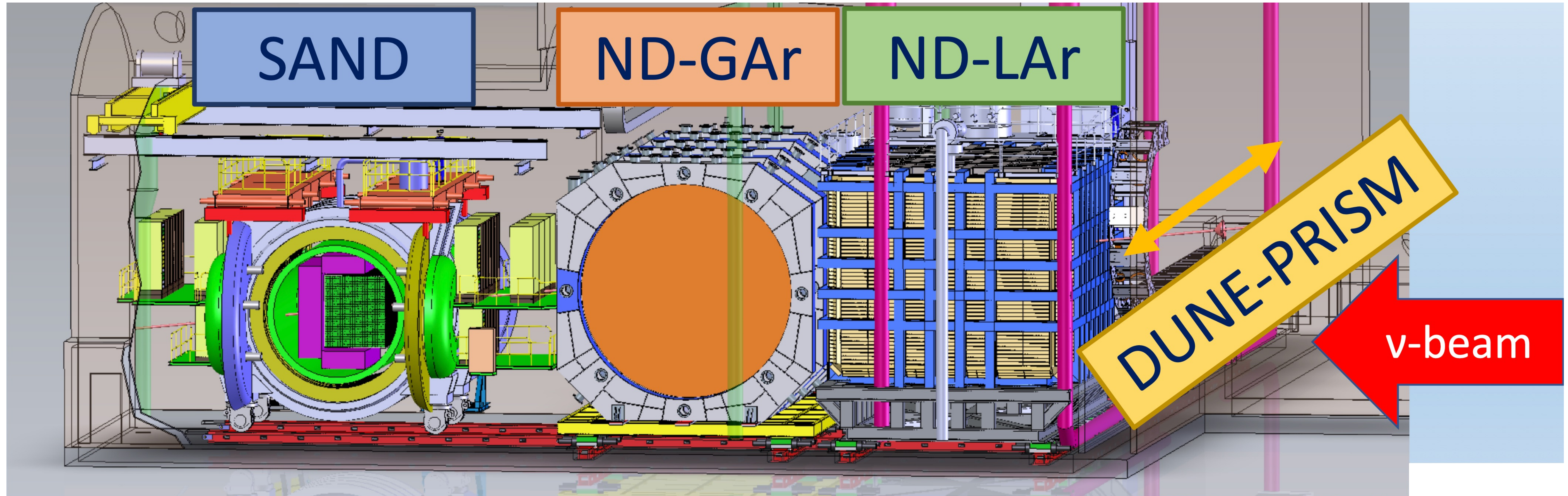
- Вступление:
 - эксперимент DUNE
 - Ближний детектор DUNE
 - Жидкоаргоновая ВПК
 - Зарядовая и световая системы
- Компоненты световой системы
- Прототип 2x2. Результаты испытаний в Берне. Подготовка 2x2 для тестов на пучке нейтрино.
- Подготовка к испытаниям полноразмерного модуля ВПК
- Планы на 2024-2026 гг.

Эксперимент DUNE

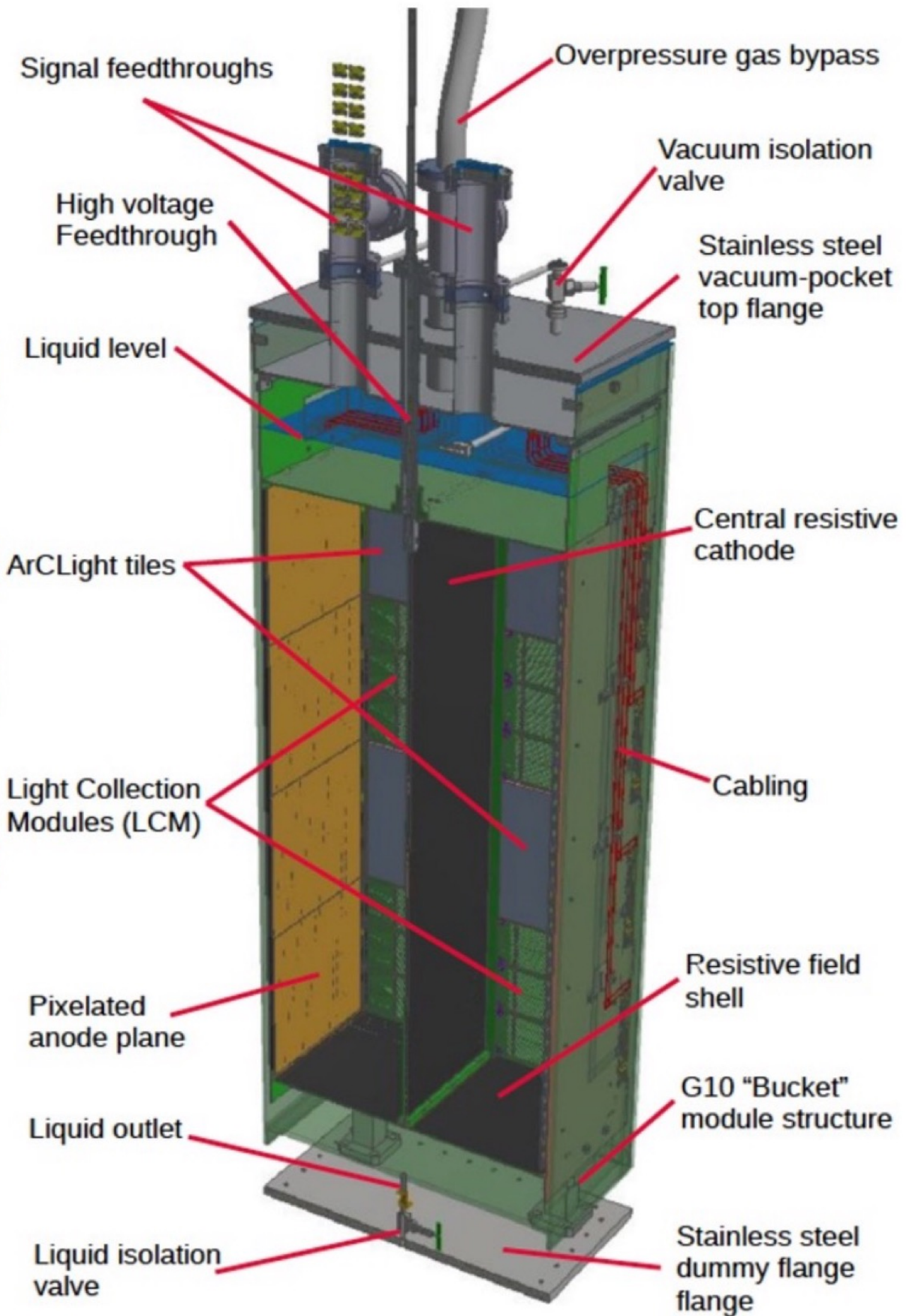
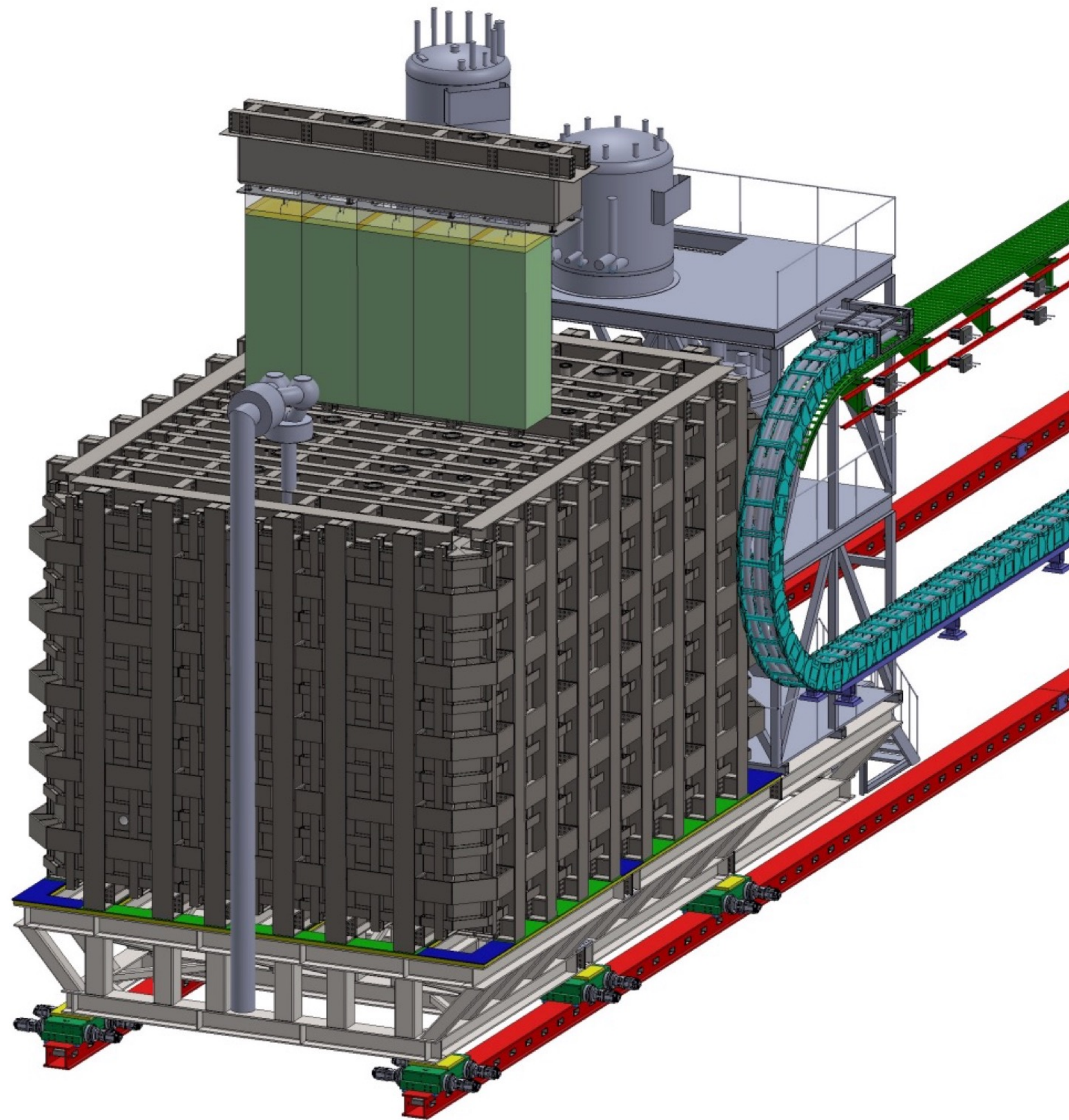
- Ускорительный нейтринный эксперимент с длинной базой (1300 км)
- Последователь эксперимента NOVA
- Два детекторных комплекса: ближний и дальний детектор
- Нацелен на изучение параметров осцилляции нейтрино, иерархии масс нейтрино, фазы нарушения CP инвариантности



DUNE Near Detector



DUNE ND-LAr TPCs



Key Design Features:

Active size:

5m deep, 7m wide, 3m tall
→ For ν signal containment

Signal rate: ~ 10 M / yr

Modular design:

- 5 x 7 hermetic TPC modules
- 3m active height
- Minimal inactive material
- Material density (G10) similar to LAr
- Short drift (50 cm)
- Pixelated charge readout
- Optical segmentation
- High-performance light detection
- System reliability and capability to operate in high-rate environment

5 x 7 = 35 TPC modules

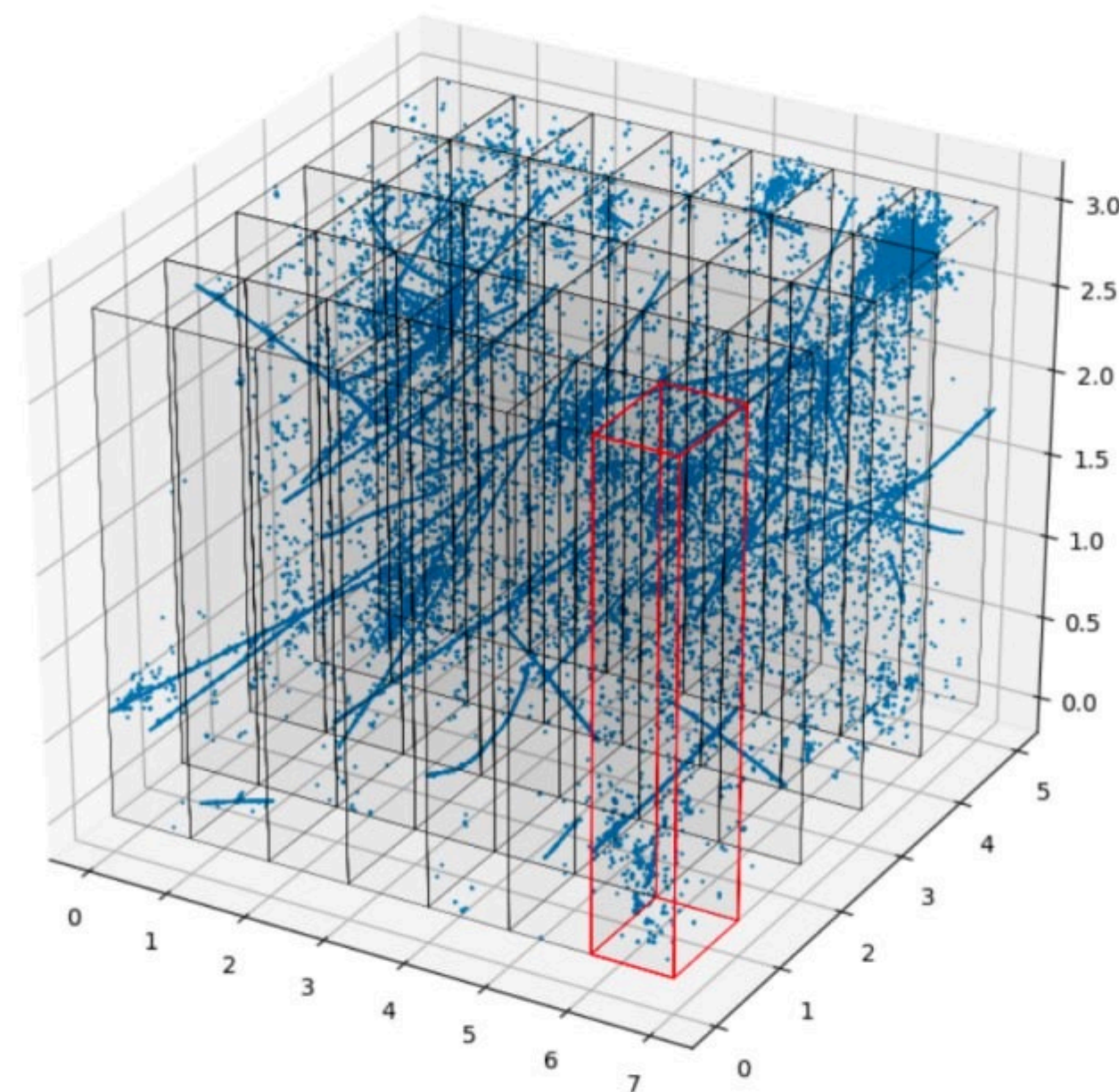
ND module size – 1m x 1m x 3m

Light detectors are along the electric field

By J. Raaf

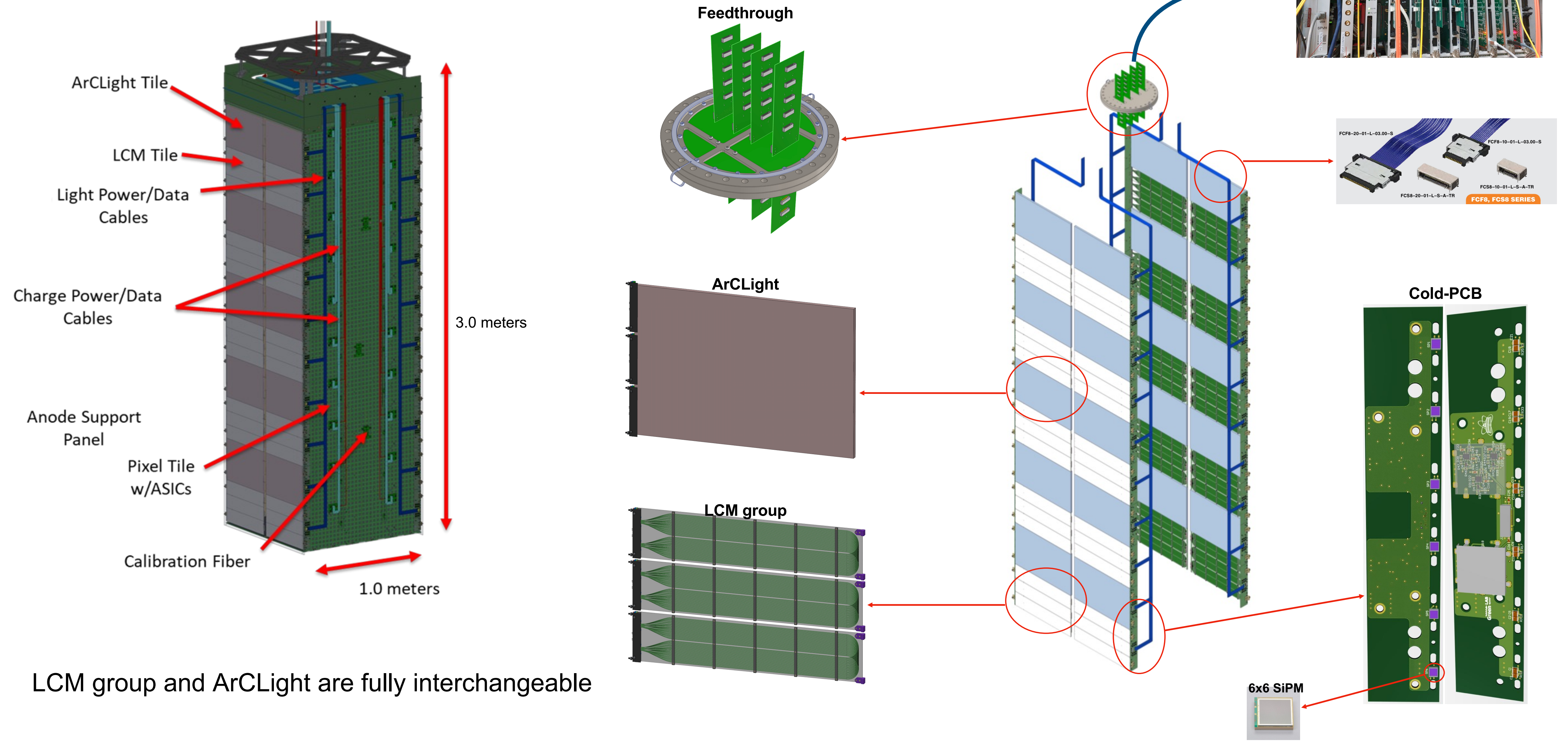
Intention of the Light detection system

- Provide t0-trigger for track correction
- Resolve pile-ups and associate tracks in time
- Assign detached energy events (\sim ns)



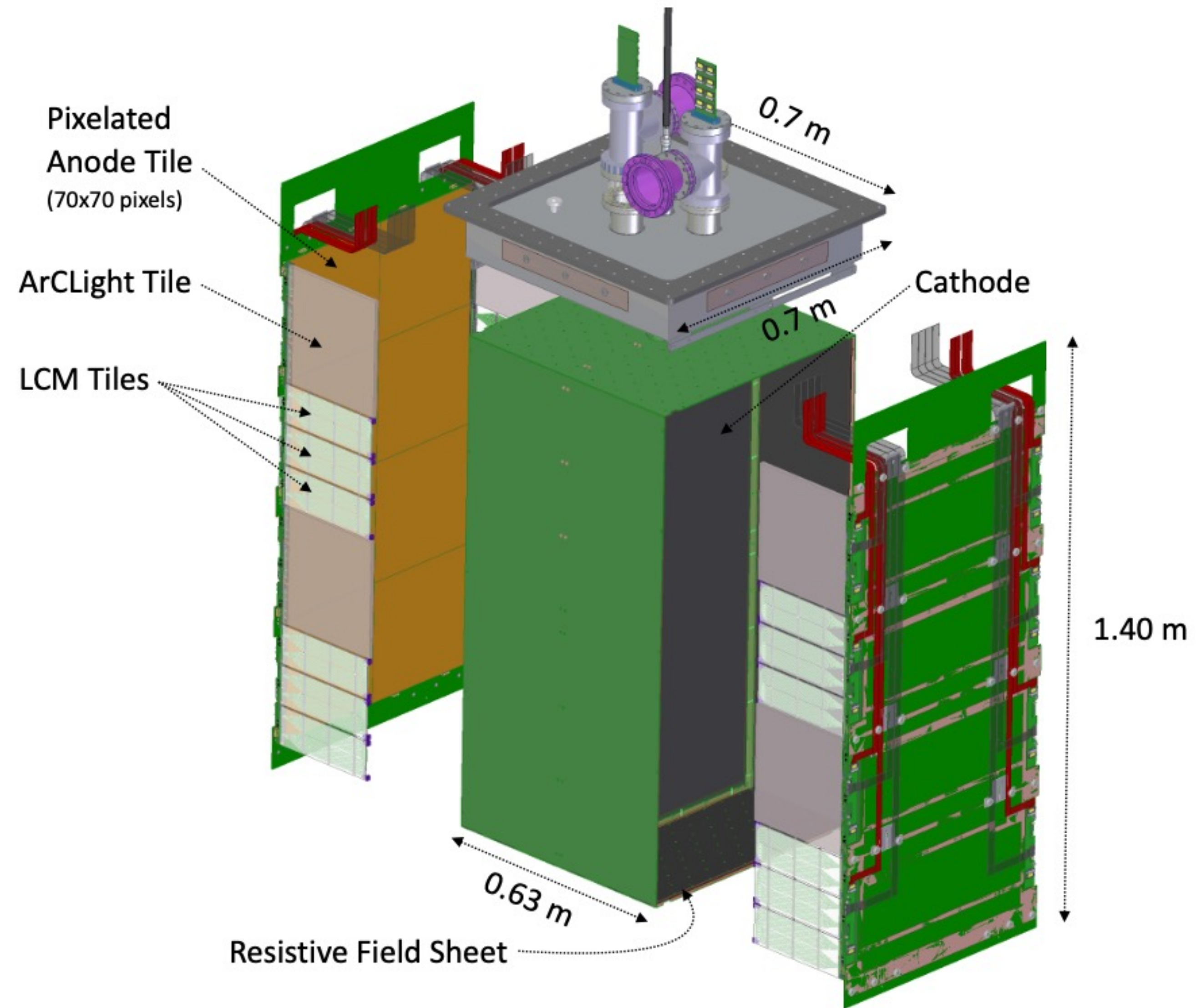
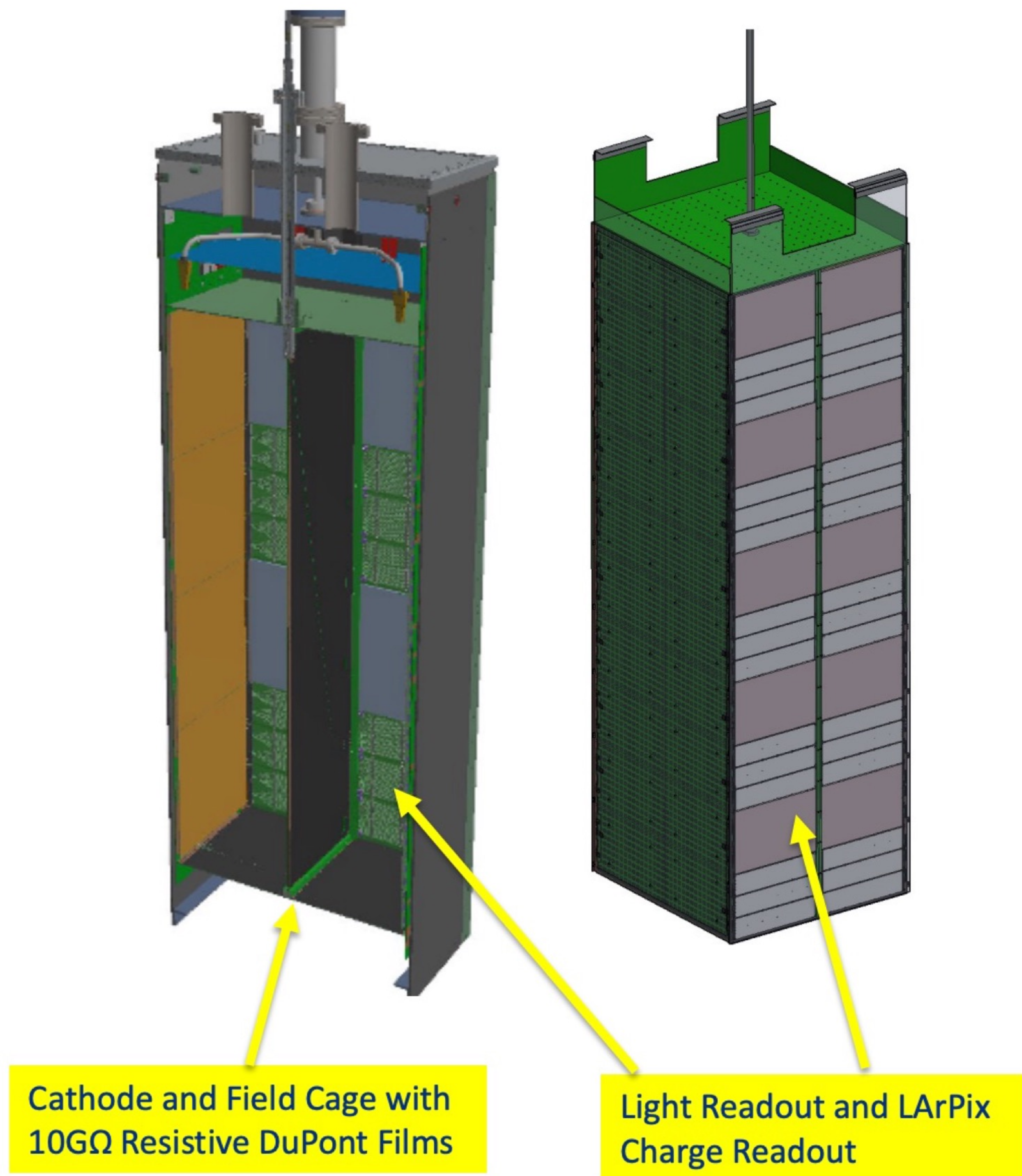
An event display of the visible energy for a typical spill from the 1.2 MW beam spill coming from the LBNF neutrino beam. The large number of crossing muons and multiple neutrino interactions can be seen along with the segmentation offered by the modular structure of the ND-LAr system

ND LArTPC Module Design



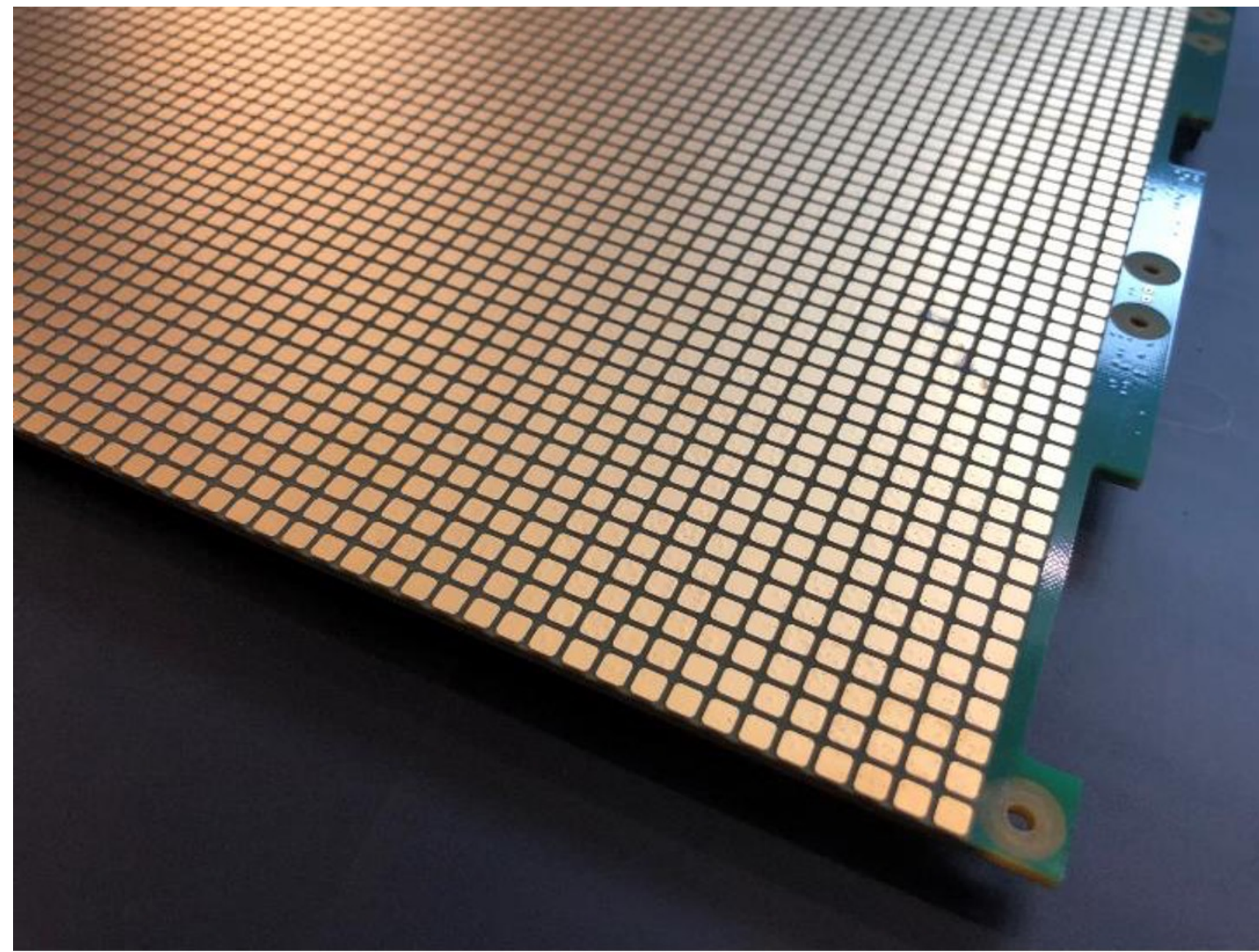
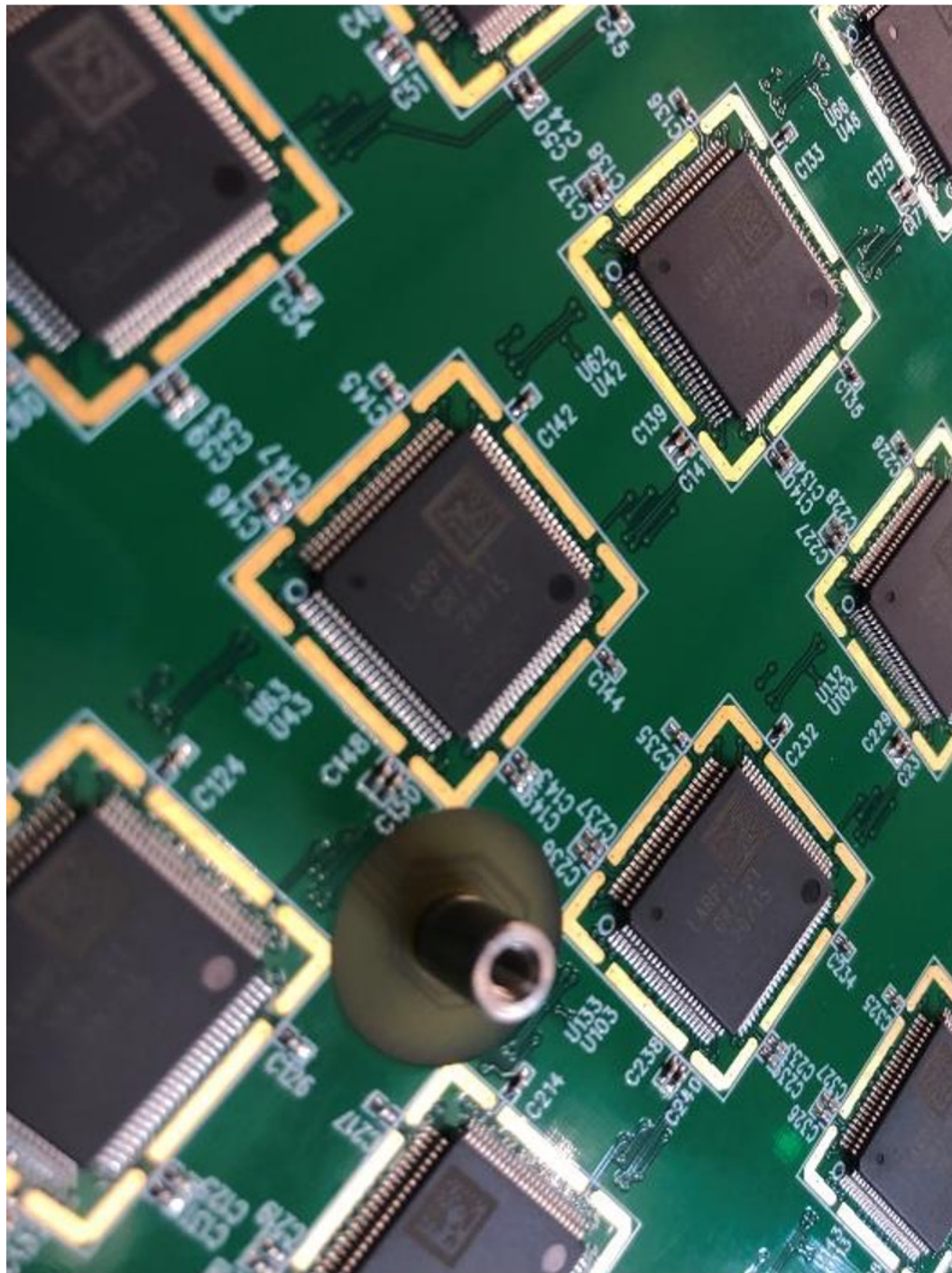
LCM group and ArCLight are fully interchangeable

2x2 Modules: 0.75m x 0.75m x 1.6m



Charge readout

- Pixel Size - $4 \times 4 \text{ mm}^2$, Pitch = 4.4 mm, 4900 pixels
- LArPix ASIC reads out up to 64 pixels
- Pixel tile $300 \times 300 \text{ mm}$ (prototype), 100 ASICs
- Full Scale Demonstrator: $\sim 300 \times 500 \text{ mm}$

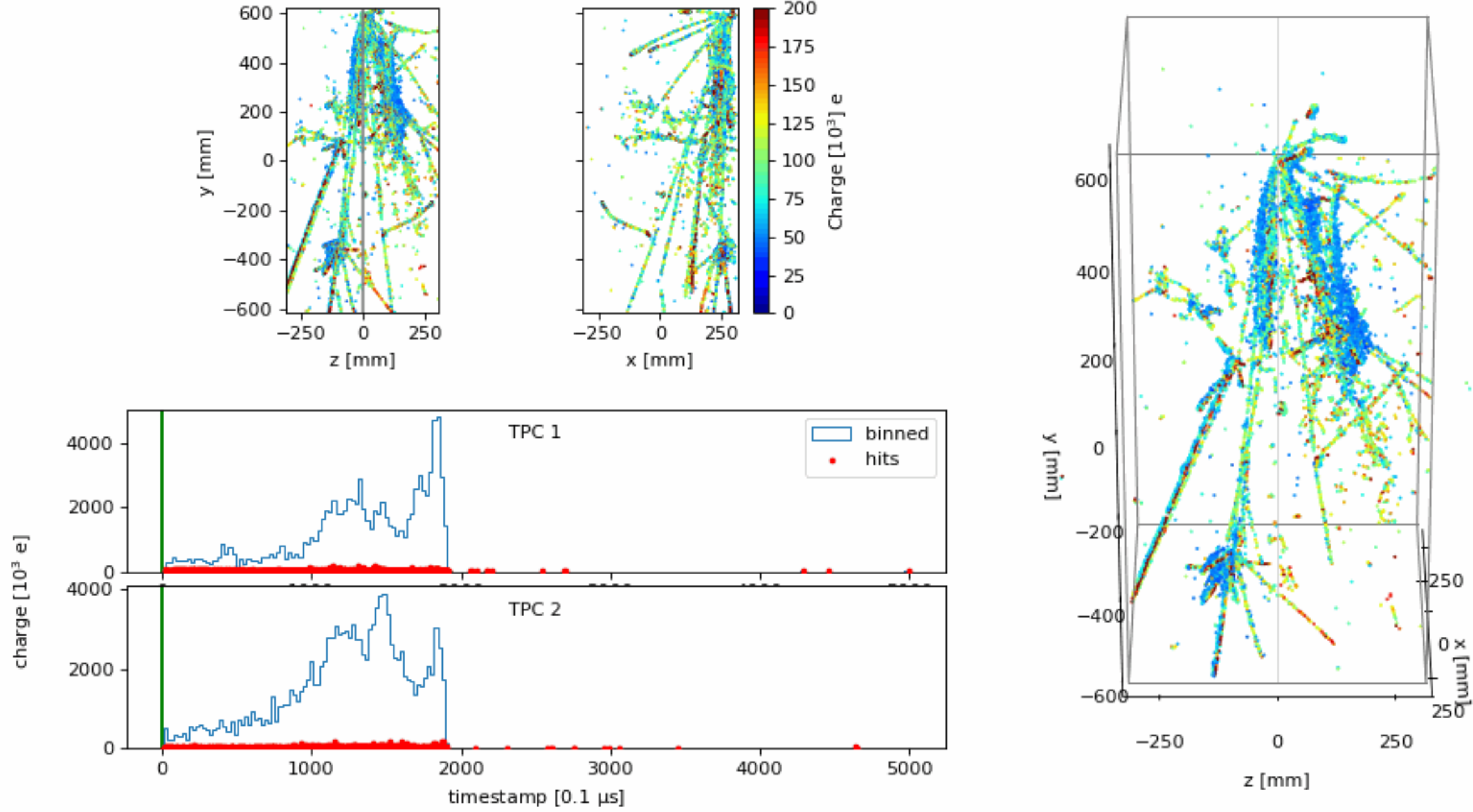


Institutions: LBNL, Caltech, CSU, Rutgers, UC-Davis, UC-Irvine, UCSB, UPenn, UTA

- ◆ Drift velocity $\sim 180 \mu\text{s} / 30 \text{ cm} @ 0.5 \text{ kV}$
- ◆ MIP energy loss $2.1 \text{ MeV} / \text{cm}$
- ◆ Electron-Ion pair energy 23.5 eV
- ◆ Recombination $\sim 0.6 @ 0.5 \text{ kV}$
- ◆ Pixel size $\sim 4 \text{ mm} \rightarrow 2 \cdot 10^4 \text{ e}^- \text{ per MIP}$
- ◆ Resampling time $2.2 \mu\text{s} \rightarrow \text{Time pixel} \sim 4 \text{ mm}$
- ◆ Hit time stamp $\sim 100 \text{ ns} \rightarrow \text{Spatial resolution} \sim 0.15 \text{ mm}$

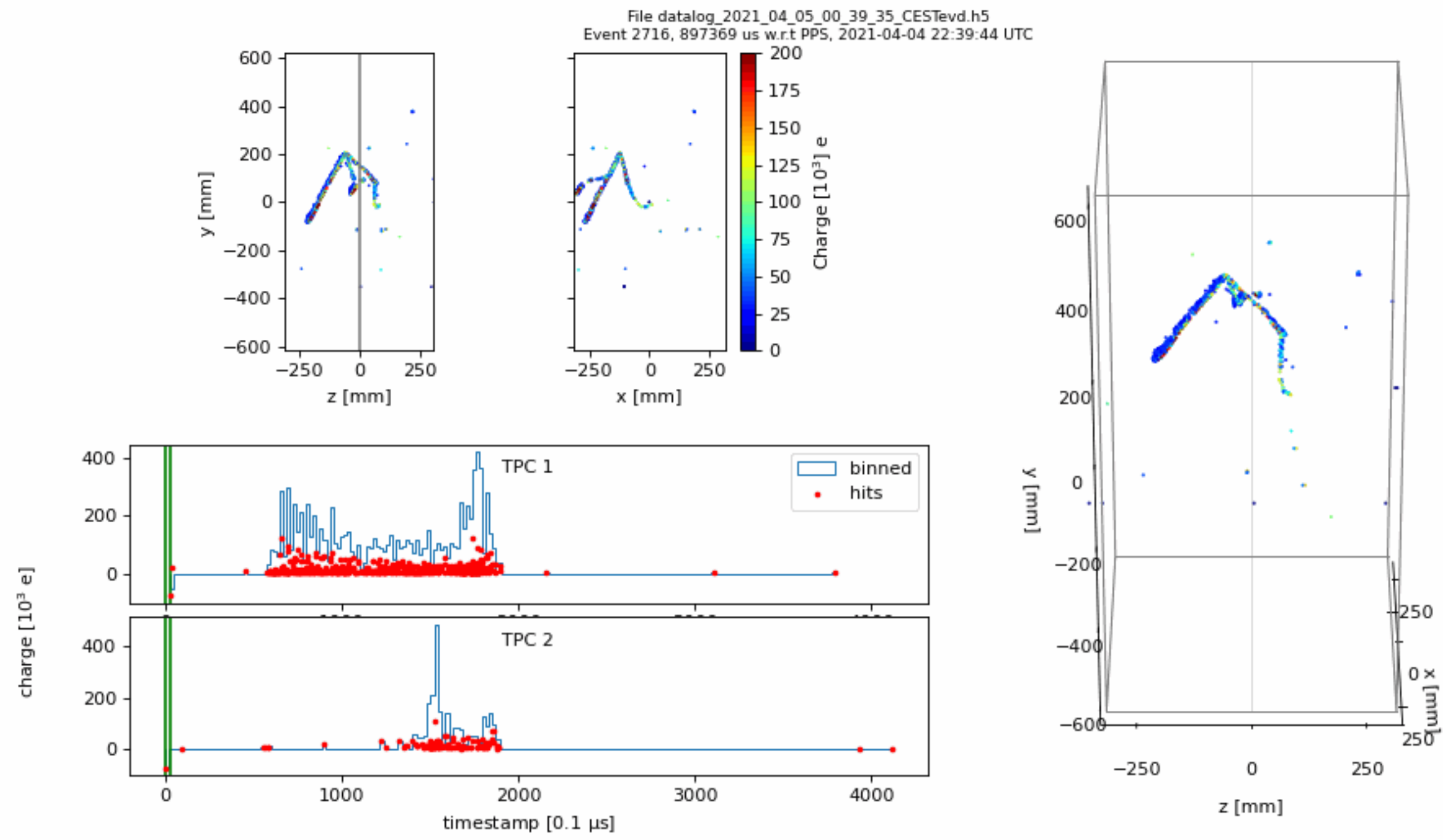
<https://argoncube.org/tracks.html>

File datalog_2021_04_02_04_57_26_CESTevd.h5
Event 14374, 4110 us w.r.t PPS, 2021-04-02 03:00:45 UTC

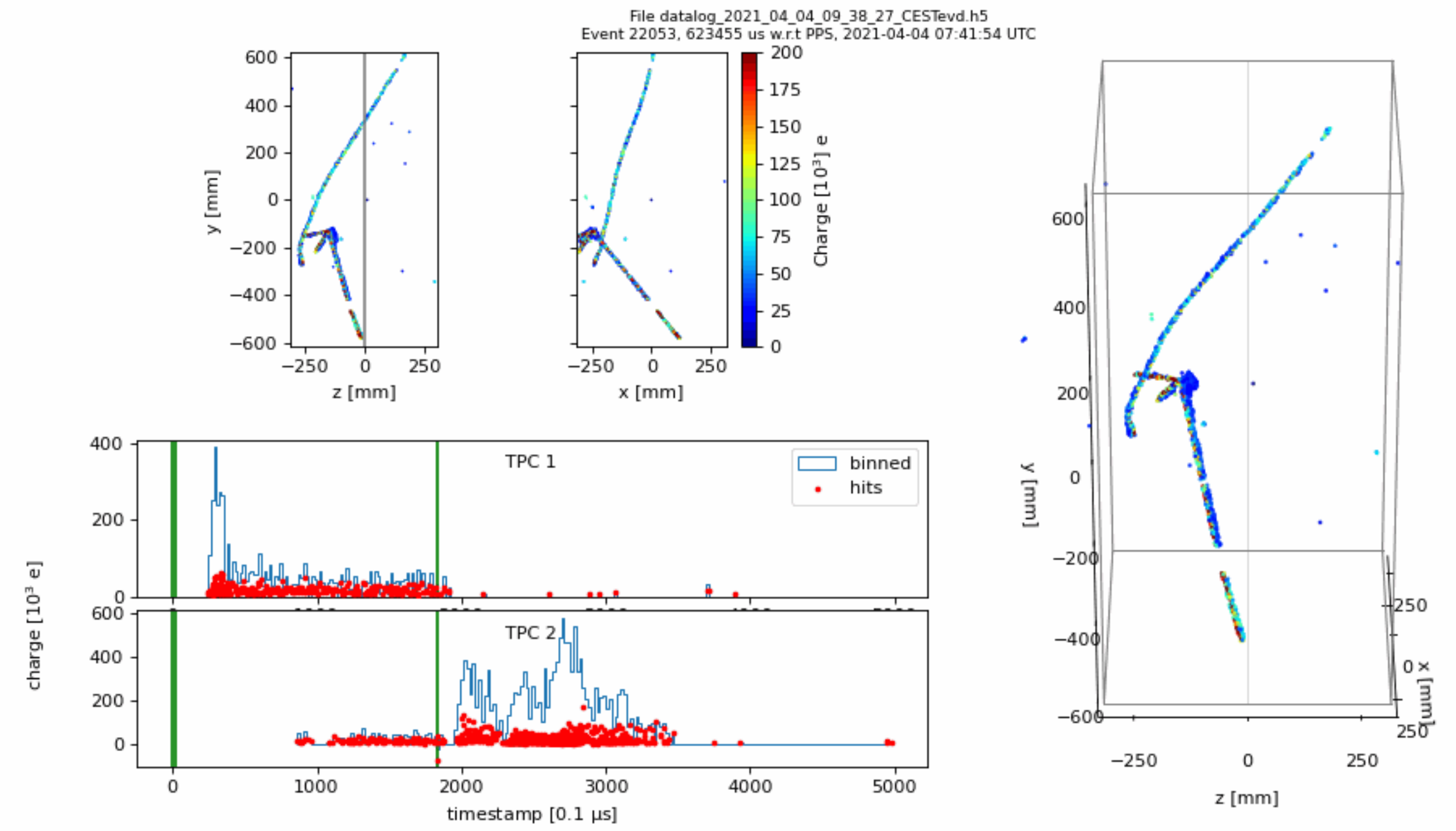


<https://argoncube.org/tracks.html>

Multi vertex interaction.



Neutrino like event with two pions and a proton.



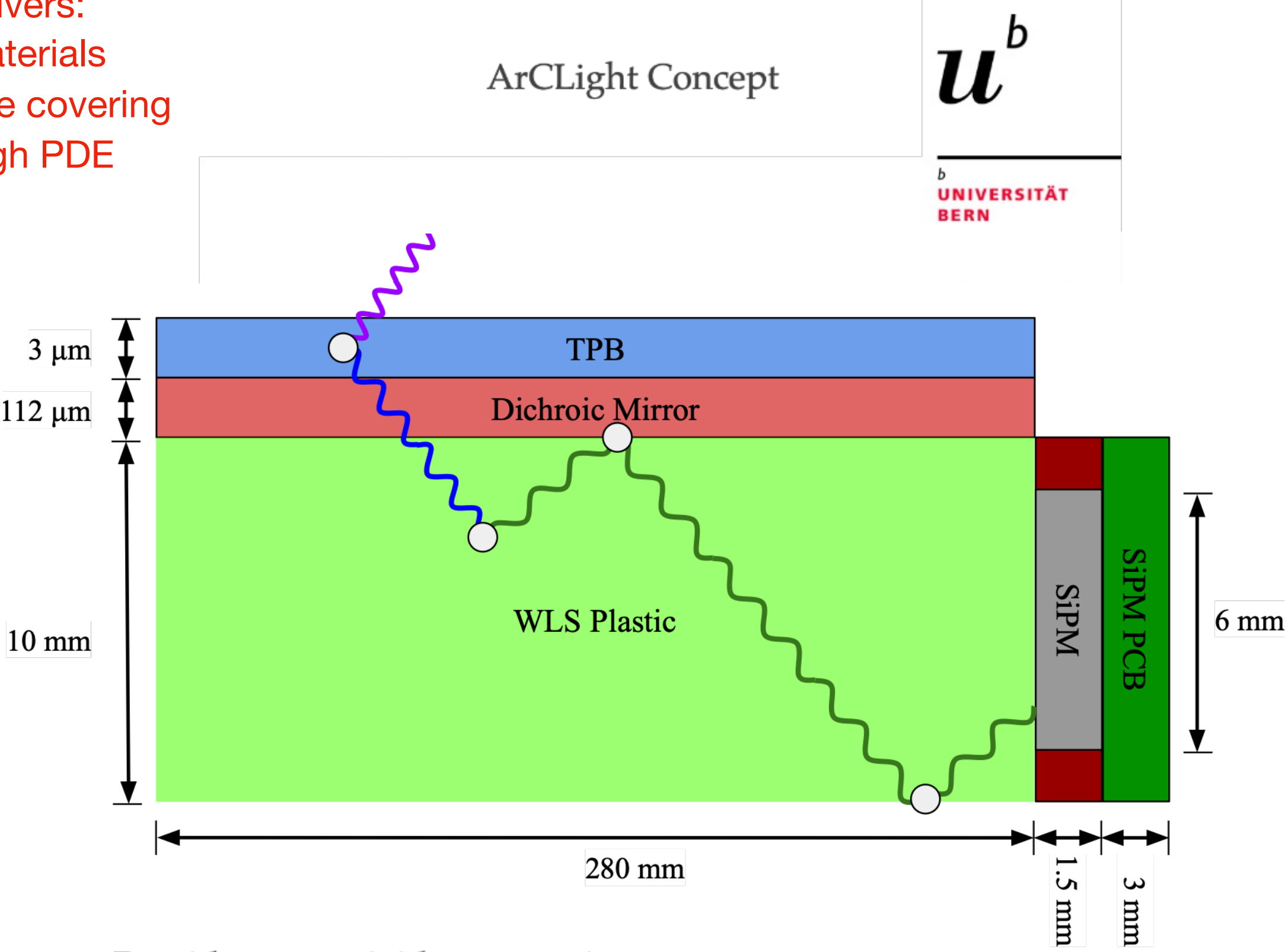
Neutrino like event with a muon and three protons.

<https://argoncube.org/tracks.html>

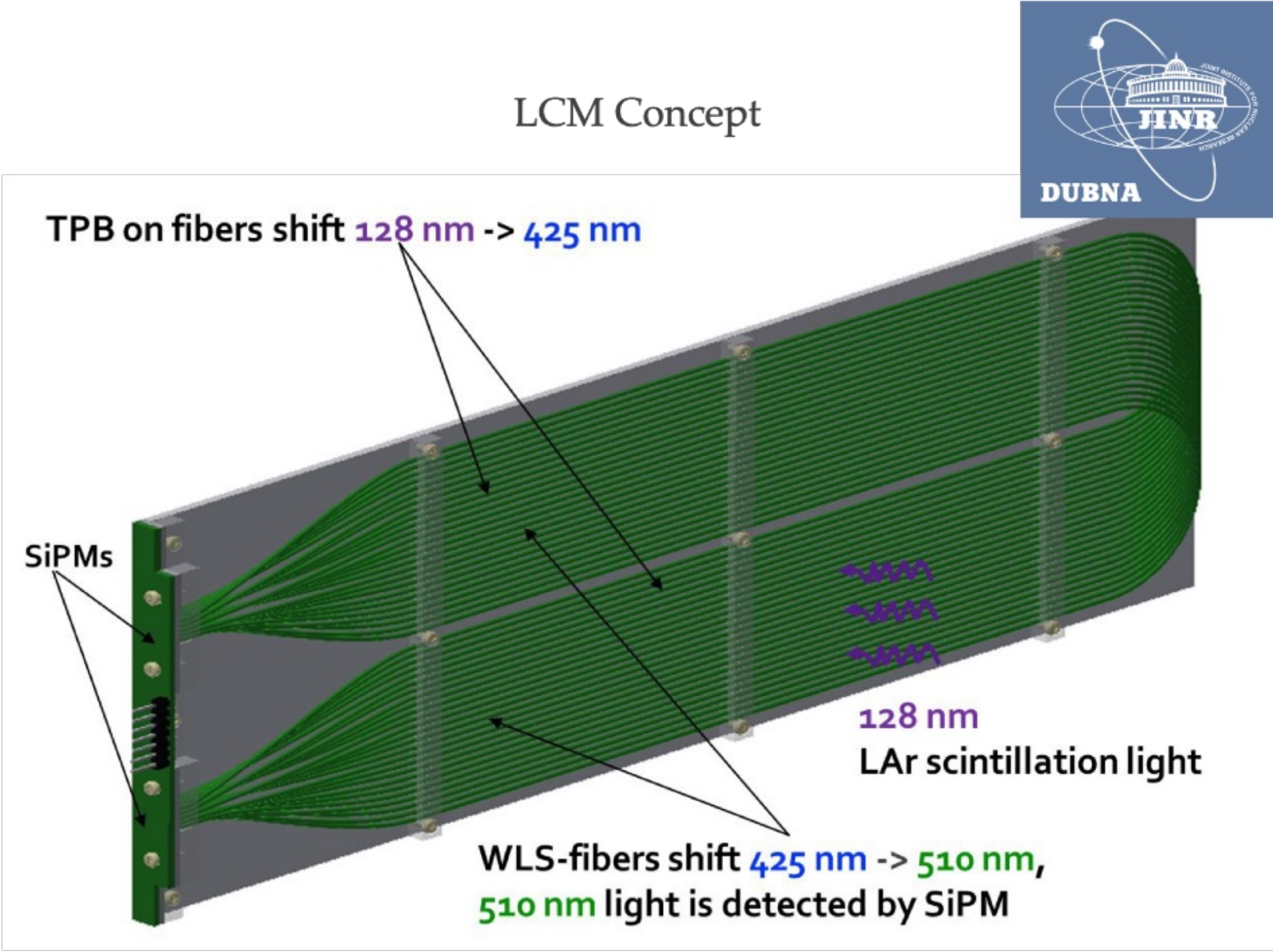
Light detectors

- Design drivers:
- Dielectric materials
 - Large surface covering
 - Relatively high PDE

Both approaches are based on shifting UV light (128 nm) into visible (425 nm) by TPB



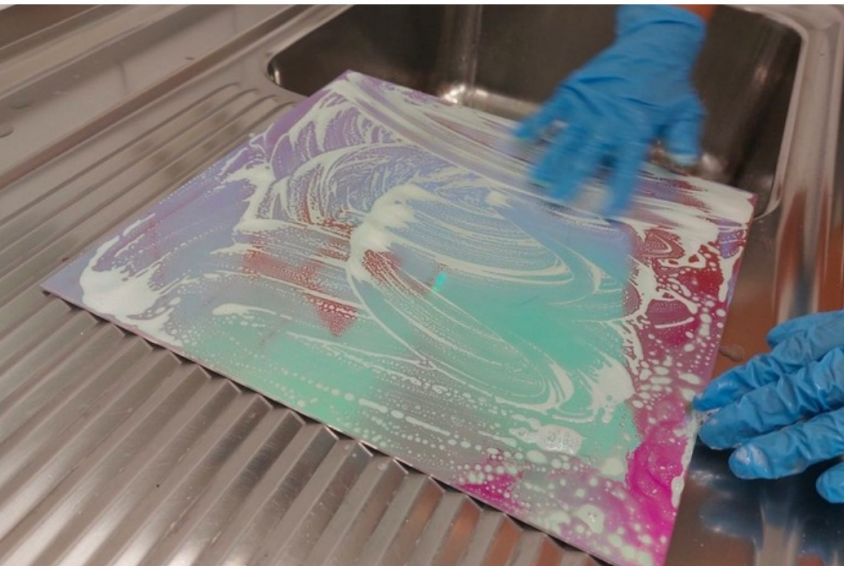
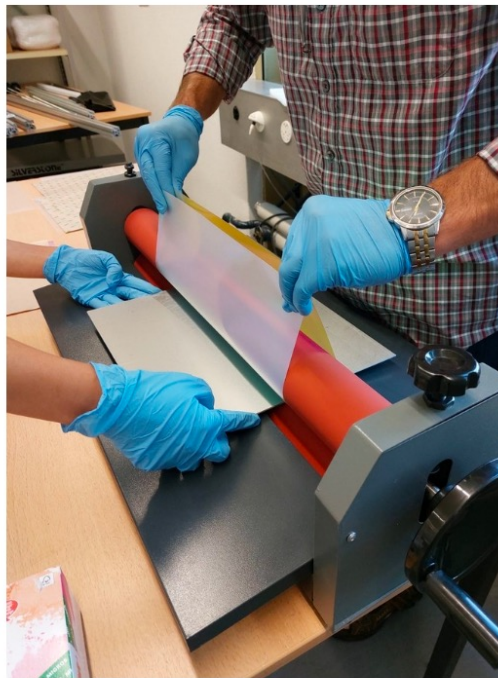
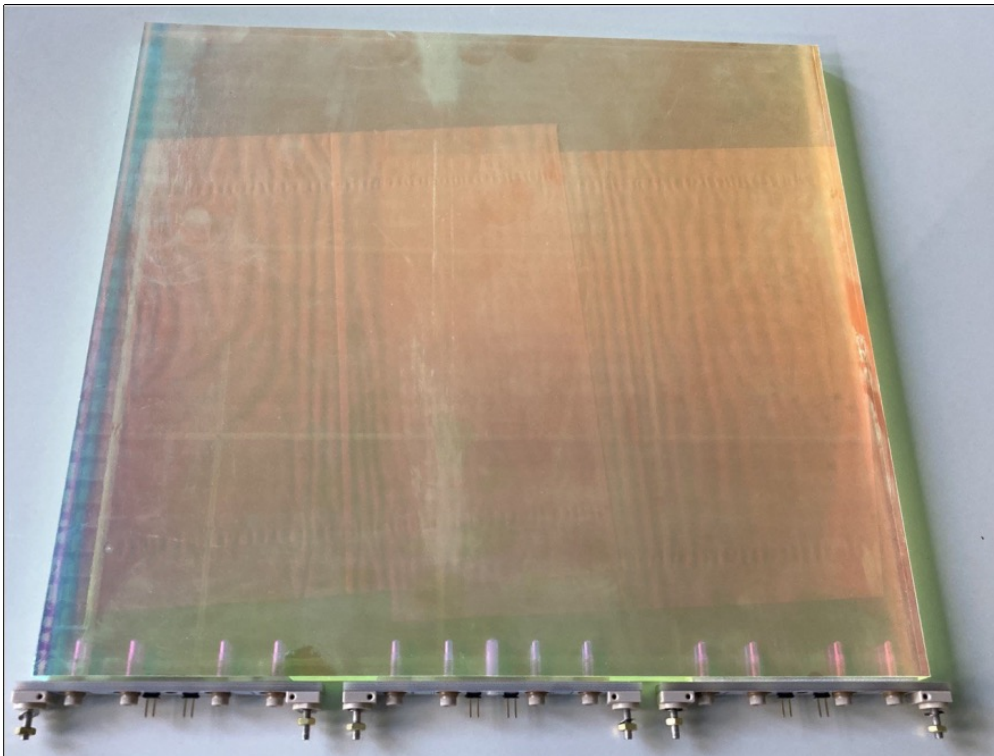
- + Provides more rigid construction
- + Spacial resolution in depth.
- PDE ~ 0.2% (Currently)
- Heavier



- + Easy to scale -> Fibers have long attenuation
- + Doesn't loose efficiency (PDE) with scaling up. PDE ~ 0.6%
- + Can be used as 1 DAQ channel
- Complex and flexible
- No spacial resolution in depth

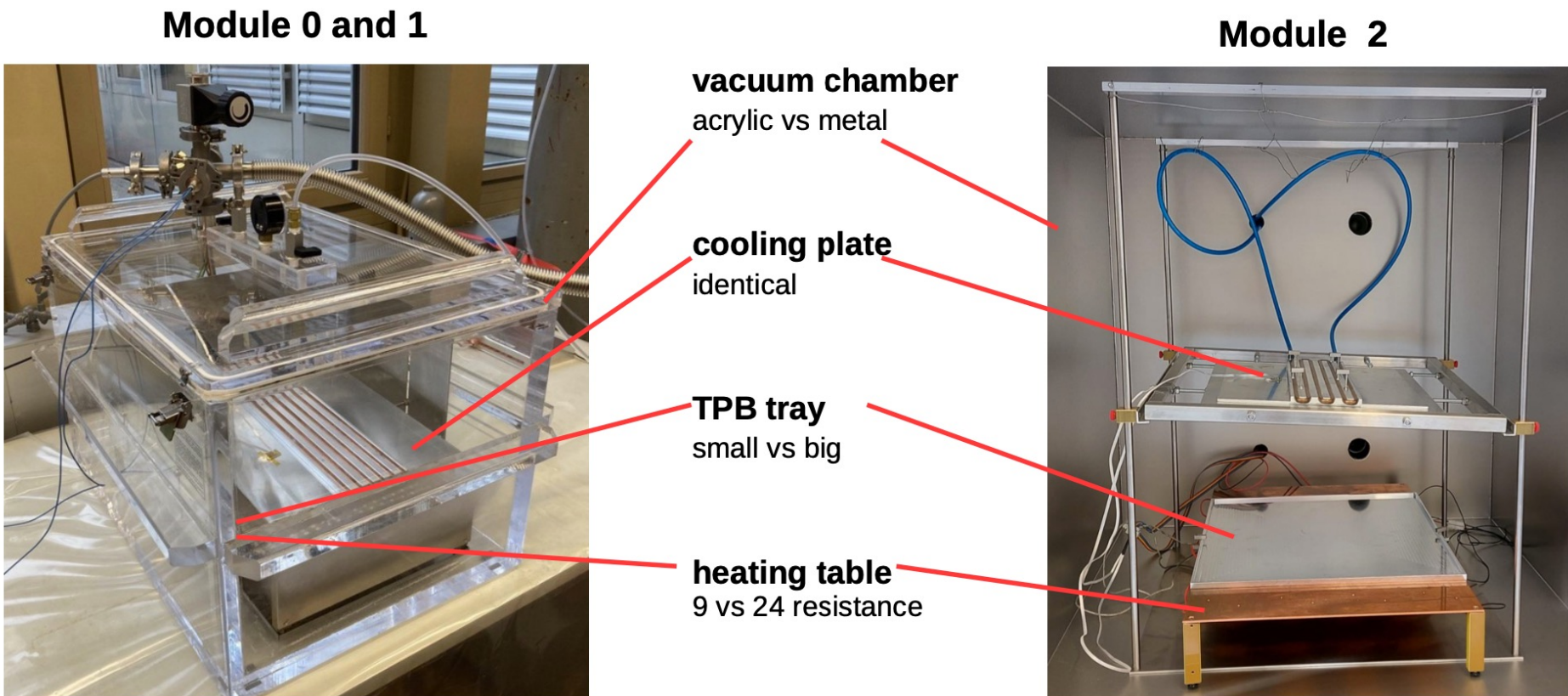
Light detectors

ArCLight



The film is cleaned with soap

The dichroic film is fixed on an aluminum plate

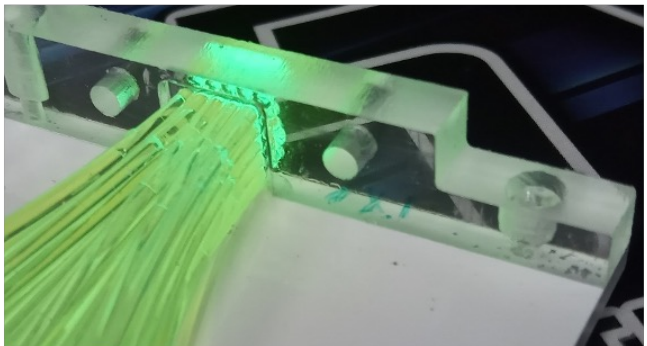


- vacuum chamber**
acrylic vs metal
- cooling plate**
identical
- TPB tray**
small vs big
- heating table**
9 vs 24 resistance

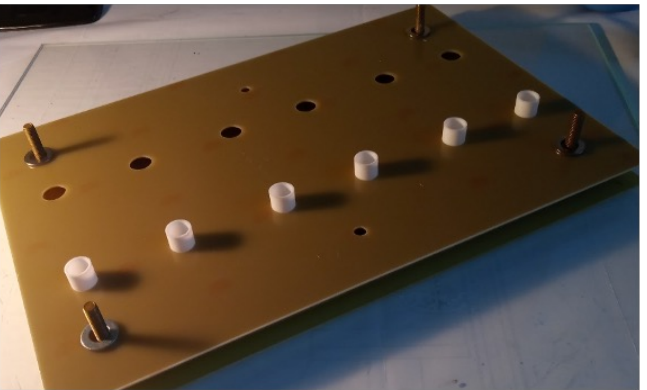


Coated film is removed from aluminum plate

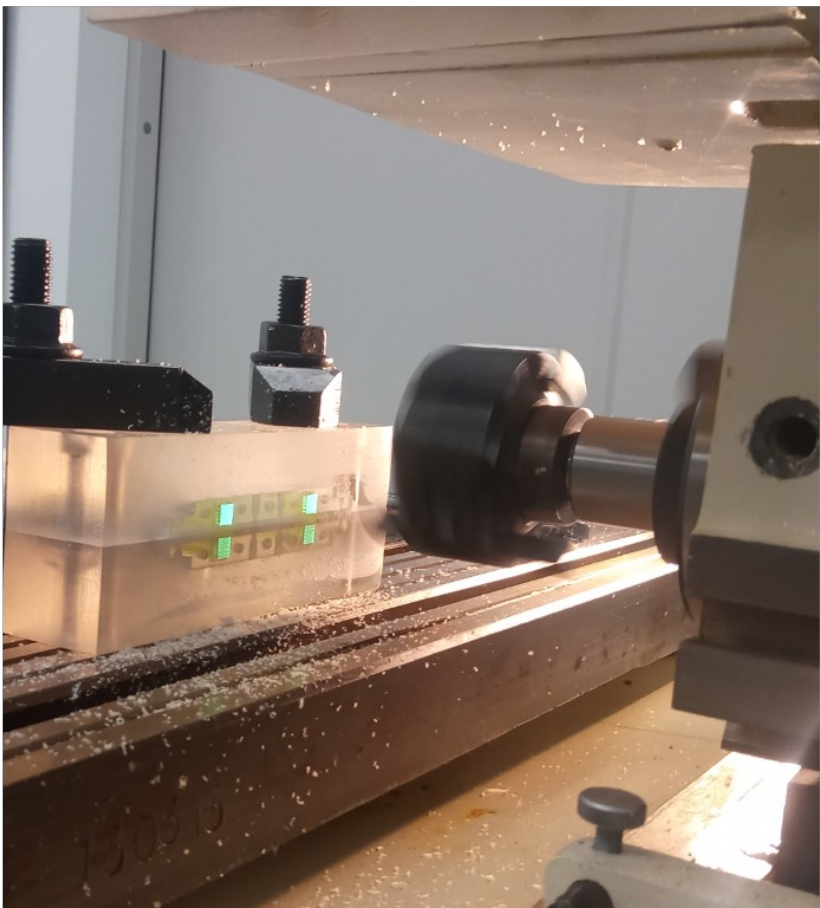
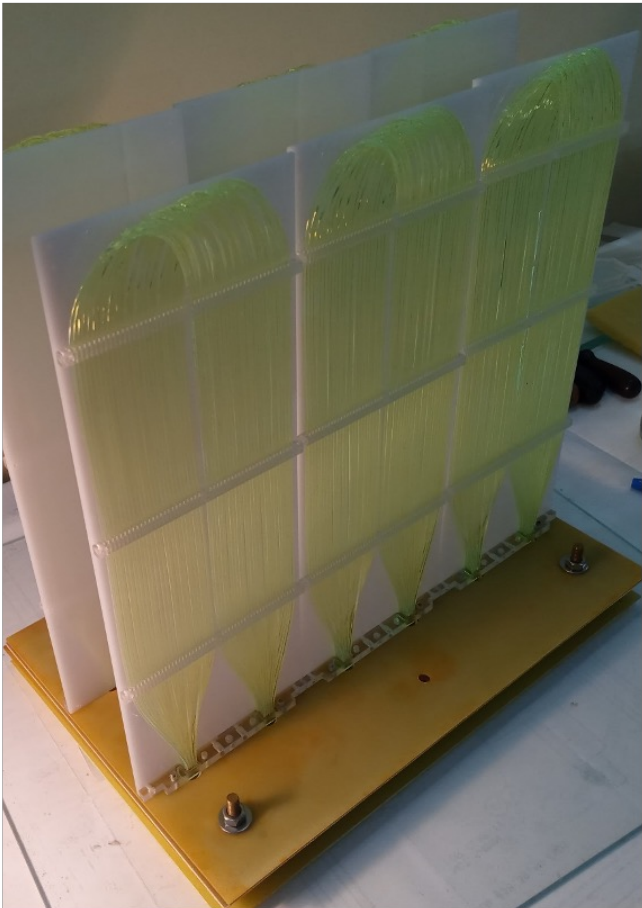
LCM



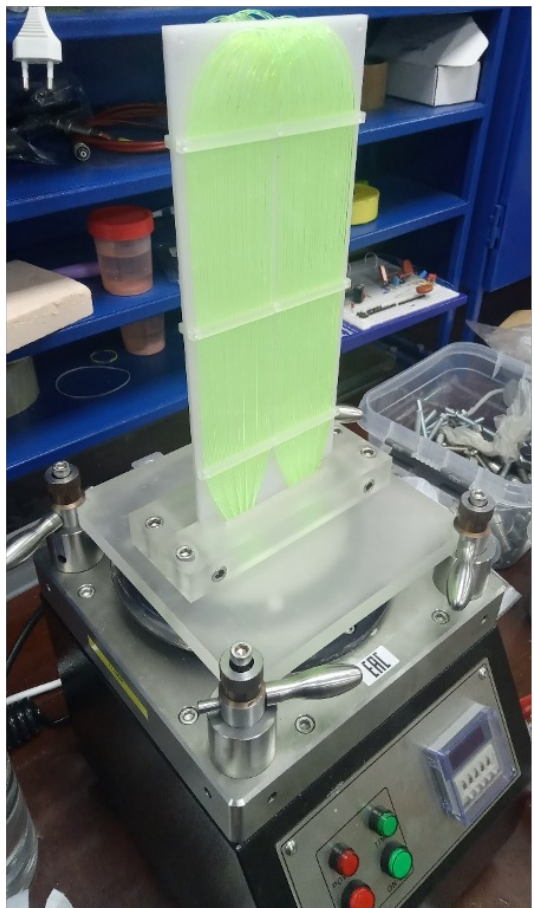
1x1mm groove for glue



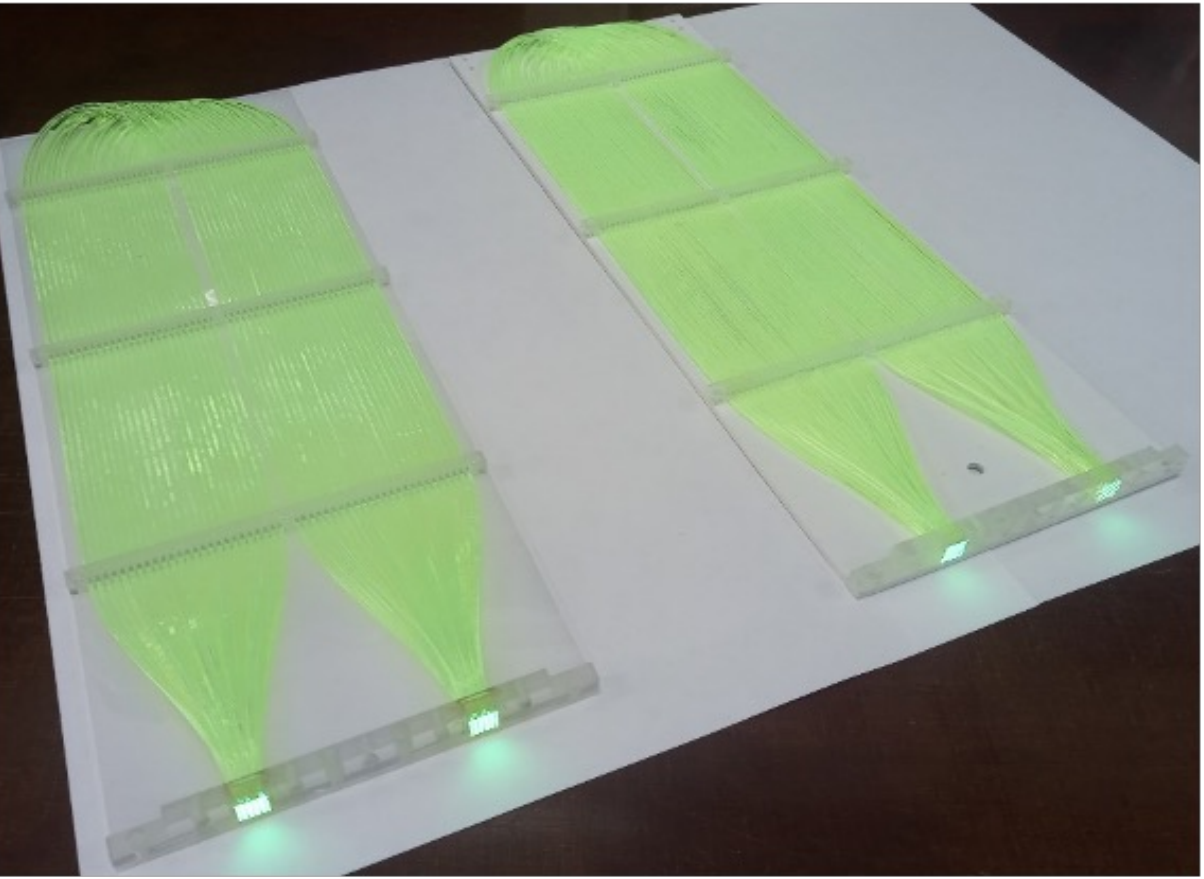
PTFE containers for bundle's fibers (capillary effect)



To process with MCD diamond tool



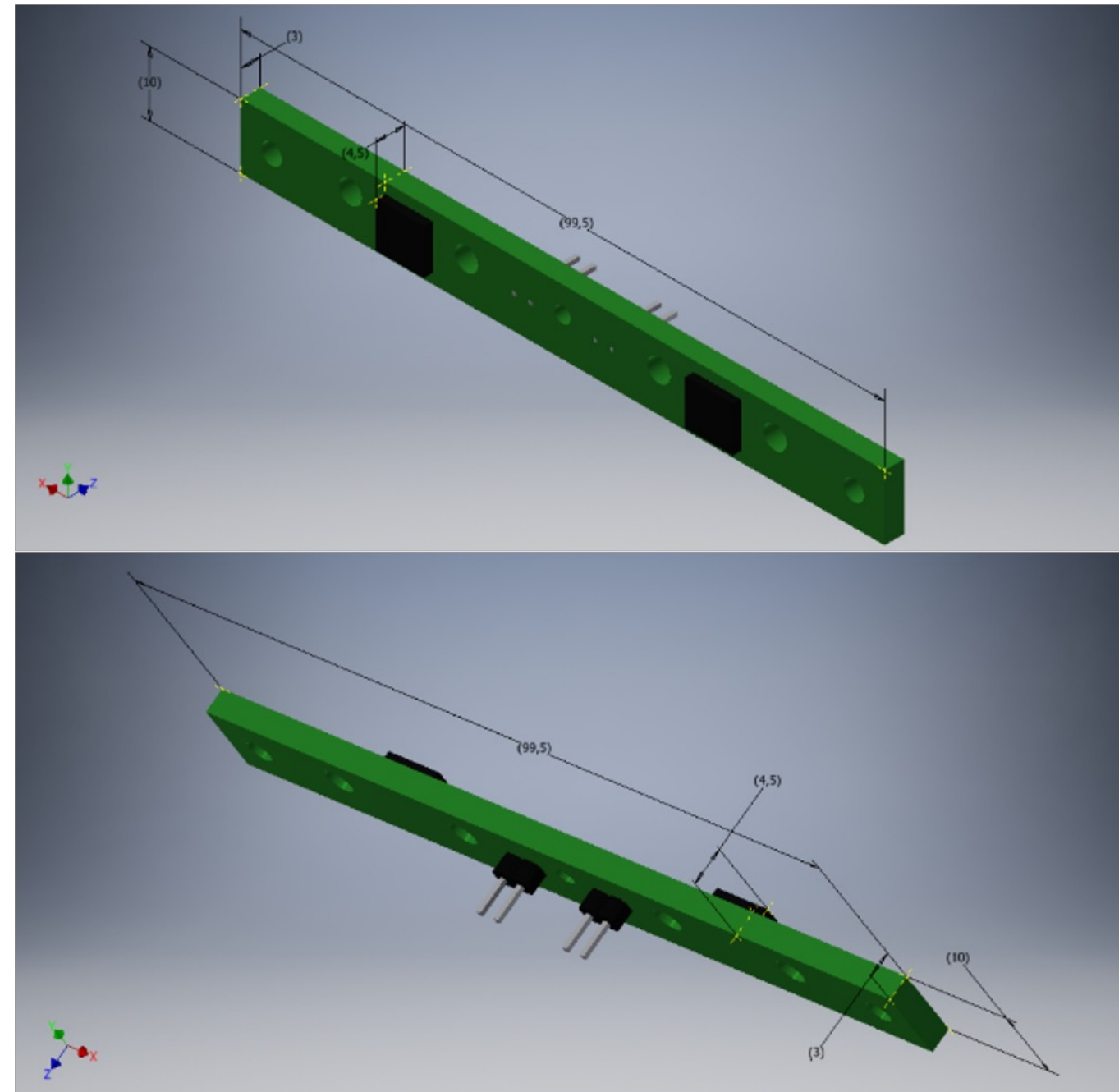
Apply polishing machine for fabric optical connectors



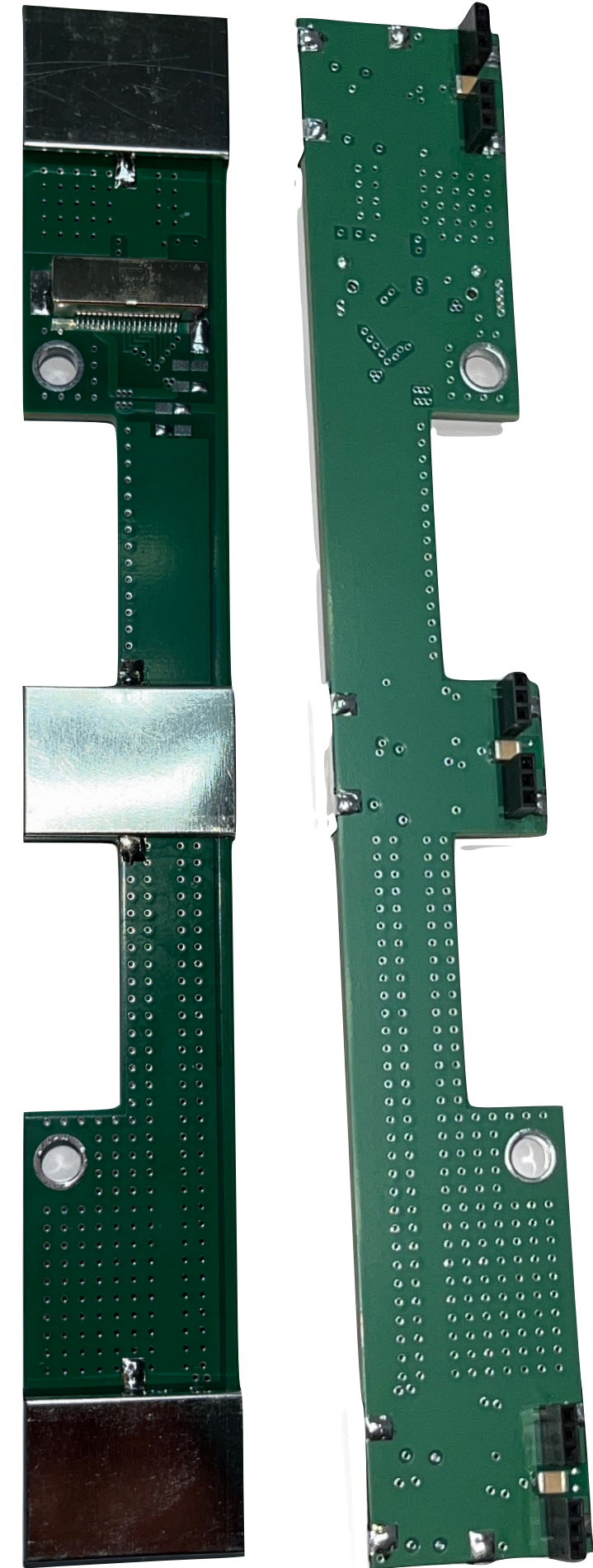
Change all the components to polycarbonate

Cold electronics

- PCB with SiPMs is attached to the LCM
- PCB connected to E-pcb board with embedded pre-amps by means of pins



- E-PCB carrying 6 preamps
- Cold preamps (LMH6624) Gain ~ 5
- Power ~ 30-40~mW each @ BW of ~ 30MHZ (~10 ns rise time).
- Interface to 3 SiPM boards (3 LCMs or 1 ArCLight)
- Metal screens use to cancel clock pick up from Charge readout.
- Samtec connectors
- Left and right boards

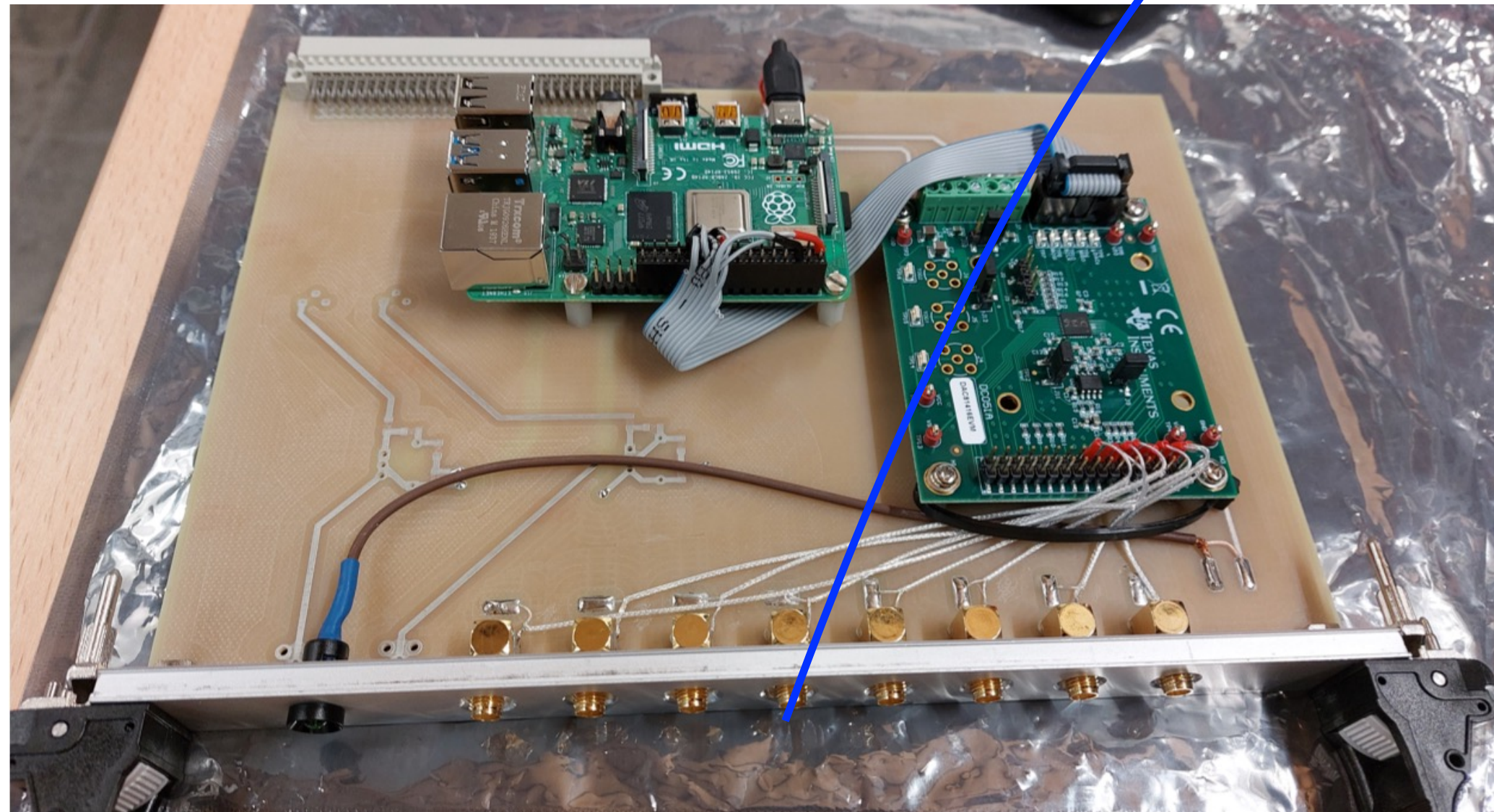


Samtec microcoax cable

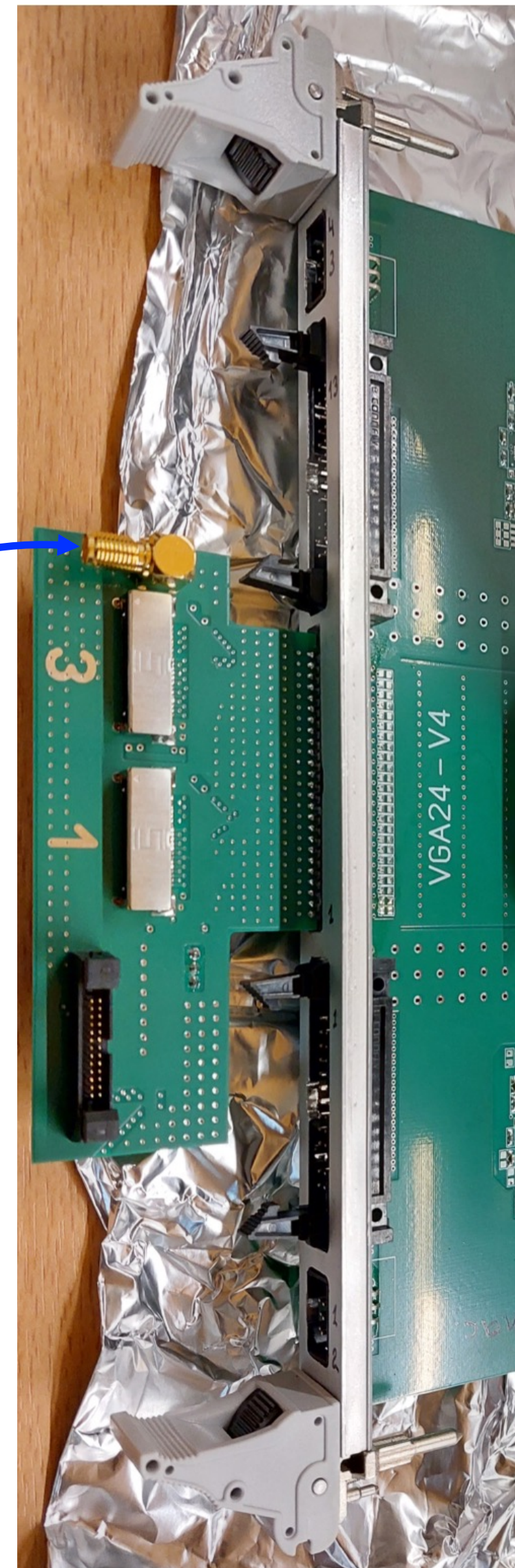


Front-end electronics

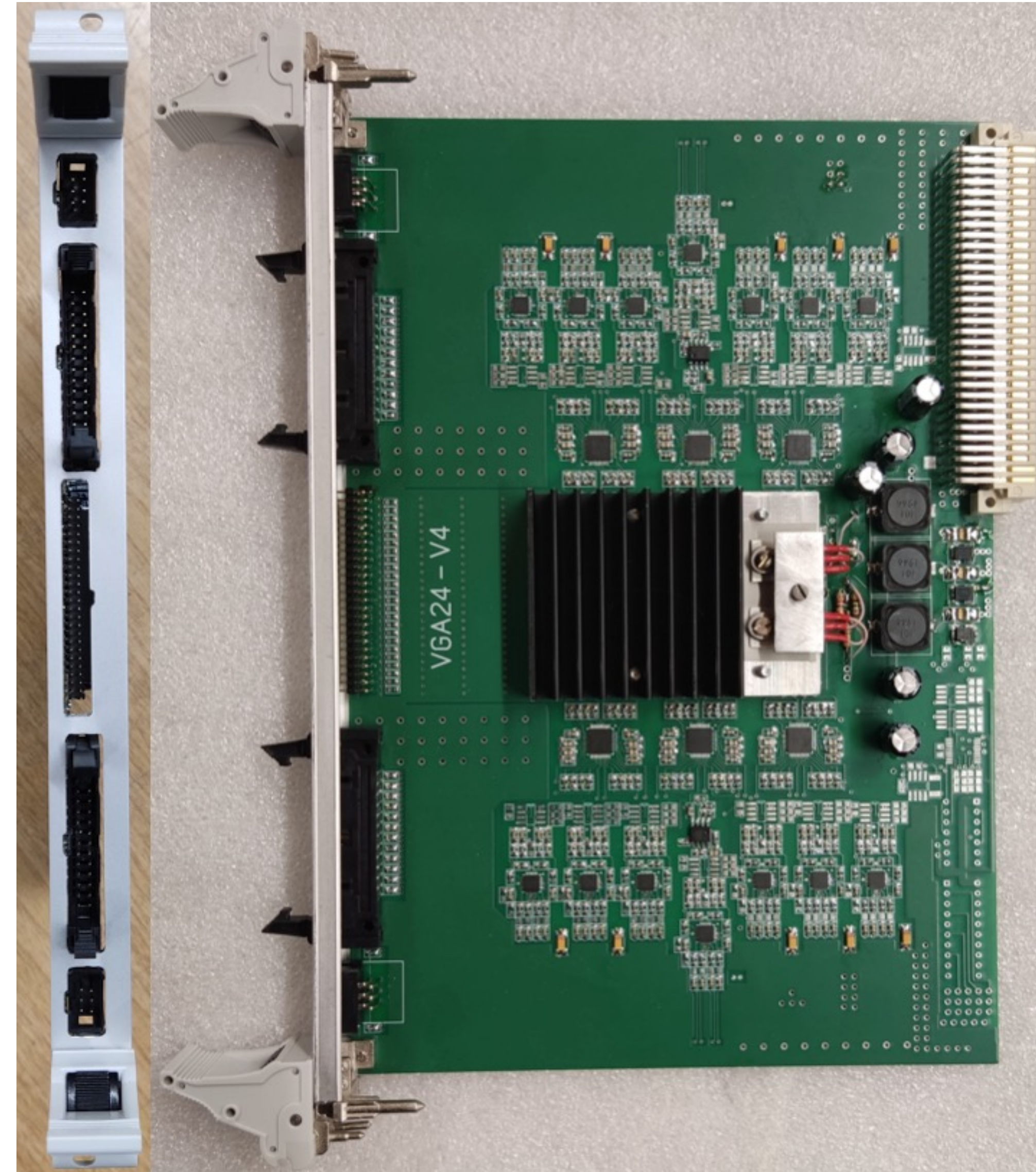
- Variable gain from 0 to 26 dB
- 2x2 Version - 24 channels/module. Drivers to long signal line
- **FSD Version - 60 channels/module. No long lines**
- Adapter board: Interface Microcoax cables to VGA and SiPM PS and Preamps power
- 2x2 Version - Controlled by means of external analogue signal (VGA control unit DAC+RPi)
- **FSD Version - Controlled via CAN-open (DAC onboard)**



VGA Control Unit (2x2)



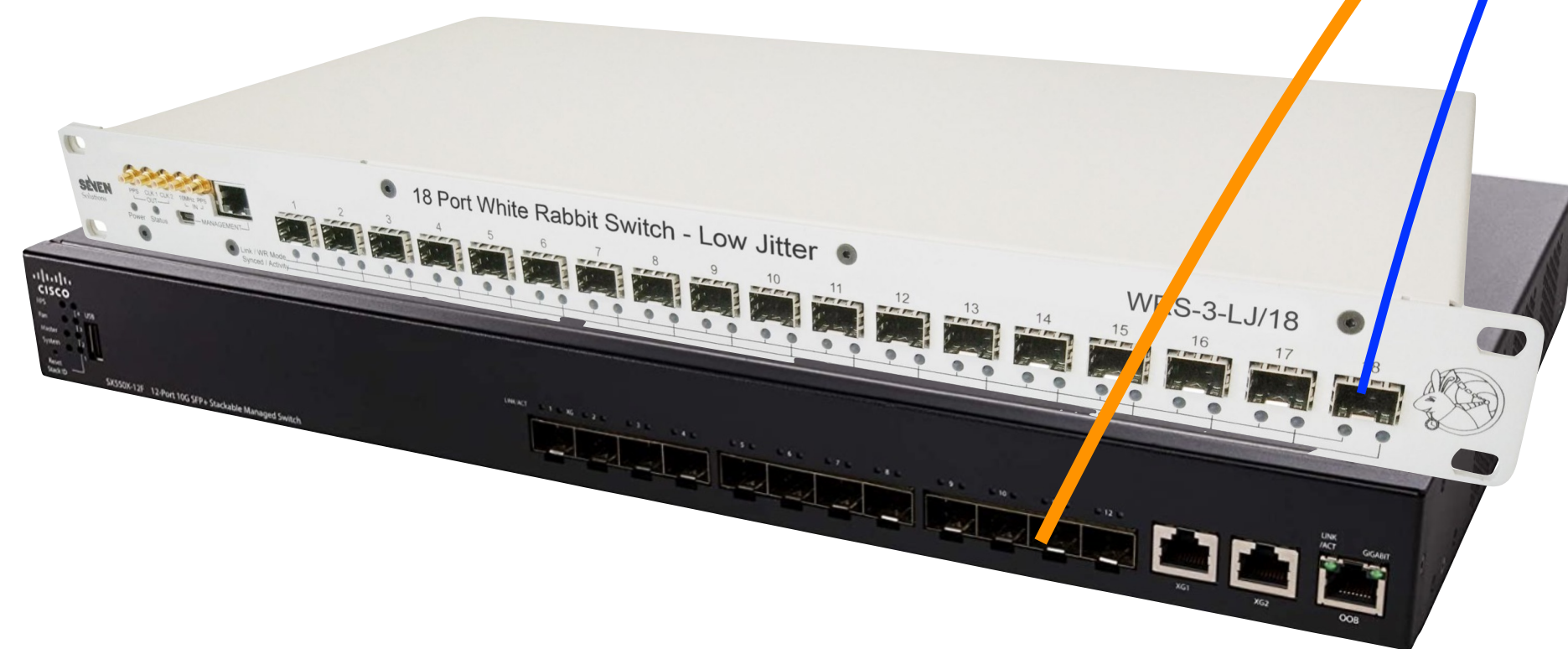
Adapter Board (2x2)



Variable Gain Amplifier Module (2x2 Version)

ADC

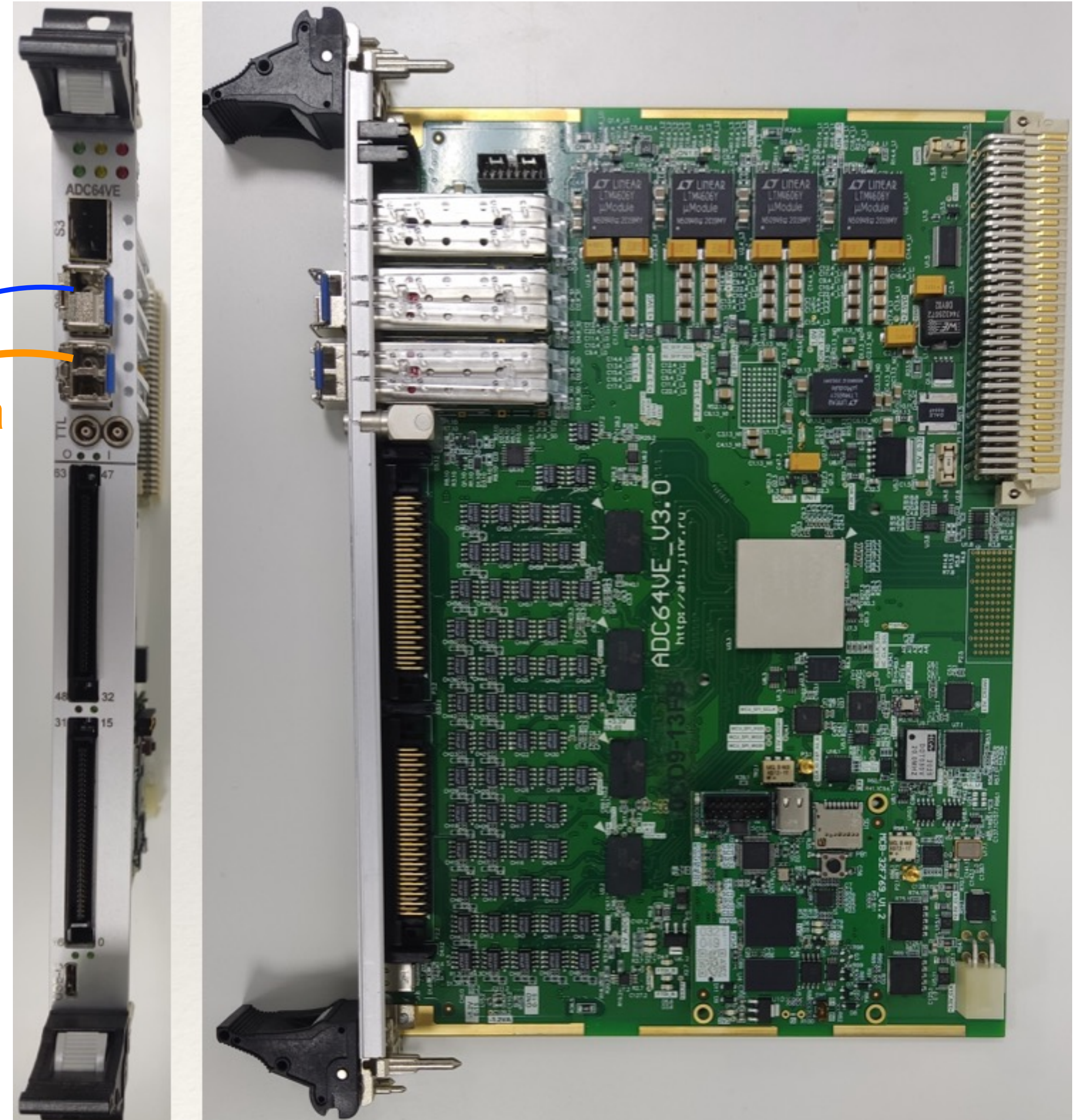
- 14-bit @ 62.5 MS/s (16 ns) - Buffer of 2 kSamples = 32 μ sec, full range ± 1 V
- Analog inputs on 2x32 channel Diff-pairs connectors
- Self-triggering mode by a digital threshold
- 64 channels, 1-unit wide 6U VME64 module, standalone
- VME64 VXS
- Optical link 10 Gbps
- ADC stream UDP/TCP data packets via M-link MStream ADCs
- White Rabbit protocol with 8 ns timestamp, <100 ps clock sync
- Spill = 10 μ sec, Light pulse ~ few μ sec, ADC window ~ 32 μ sec



Synchronization with other subsystems by means of absolute time given by GPS

WR

Data



SiPM power supply

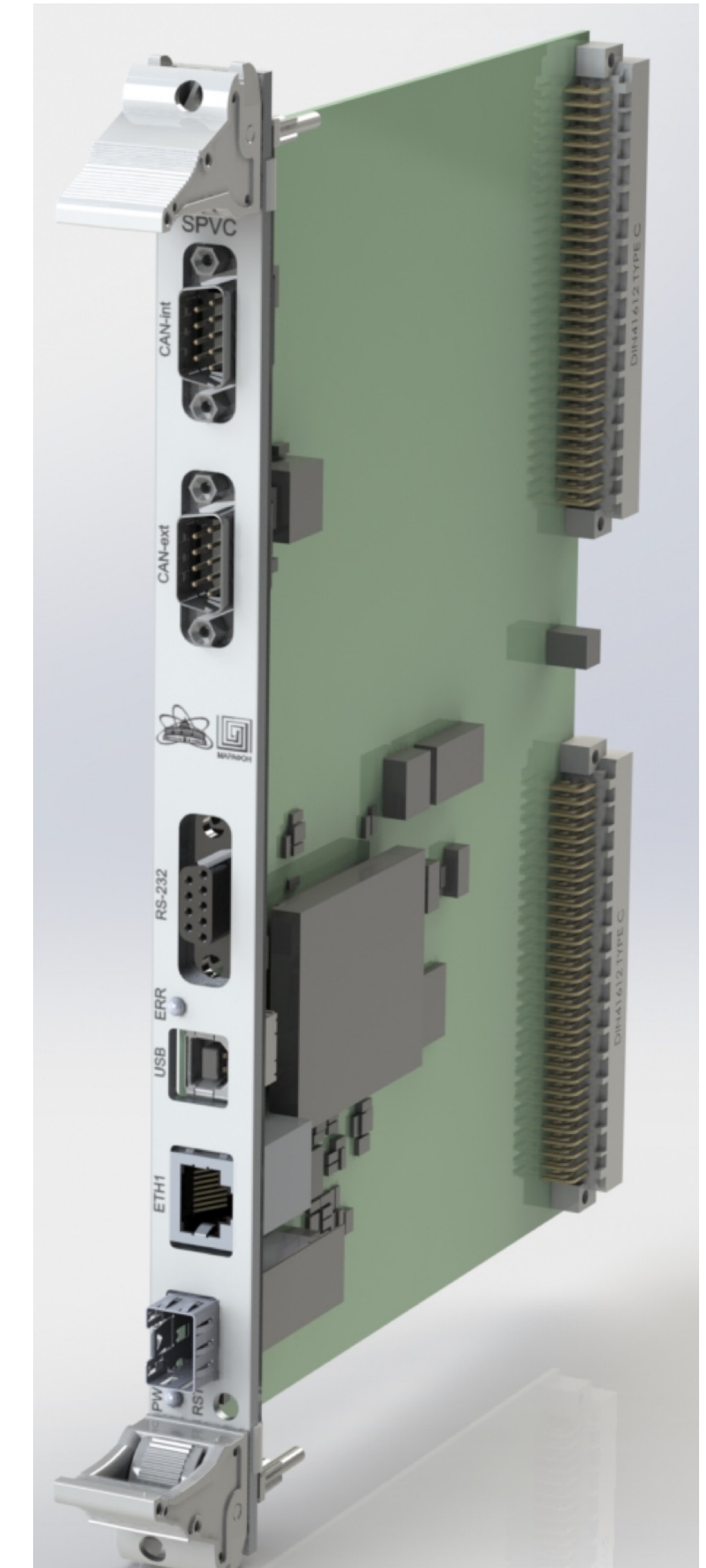
Main Features:

- VME mechanics
- Based on AD5535B chip
- Voltage up to 200 V, 14-bit
- Max current 500 μA / ch
- CAN-open protocol



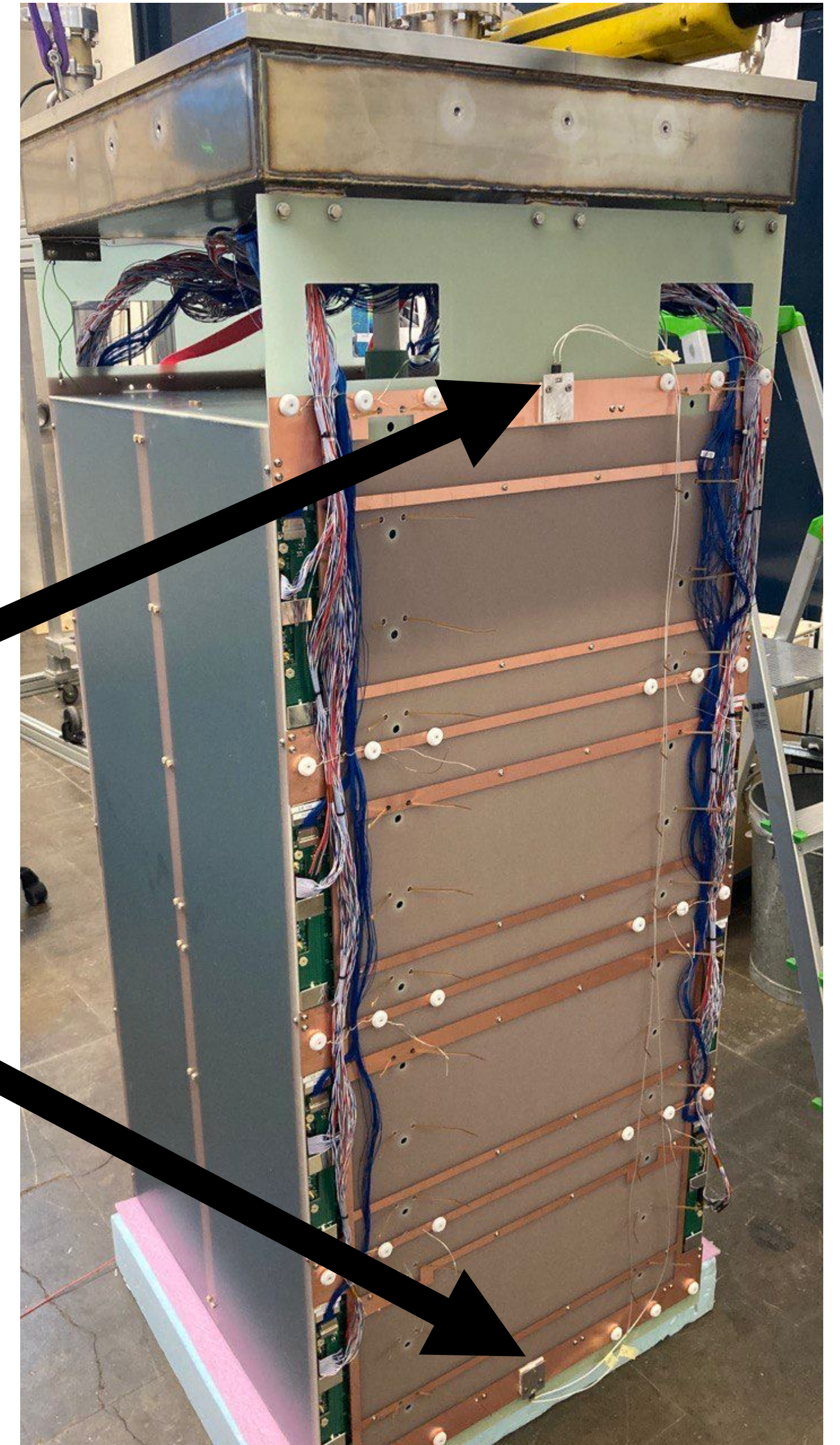
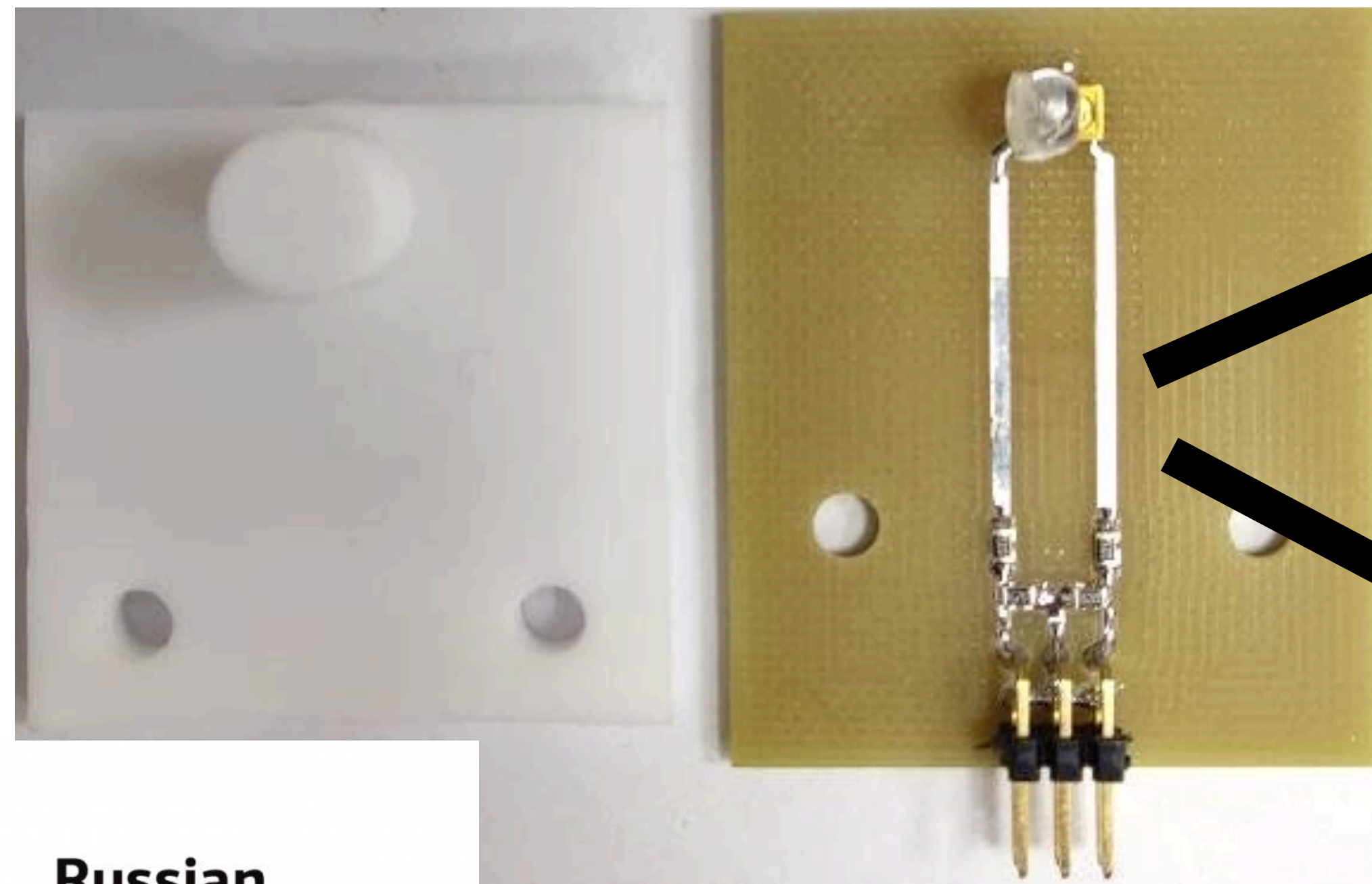
Design by Marathon
Company (MSU)

JINR is the License owner



Calibration system

- LED unit on board: $\lambda = 425 \text{ nm}$
- PTFE Diffuser - Unifies the light field
- 4 Calibration units per TPC: TOP & BOTTOM // LEFT & RIGHT
- 50Ω impedance matched



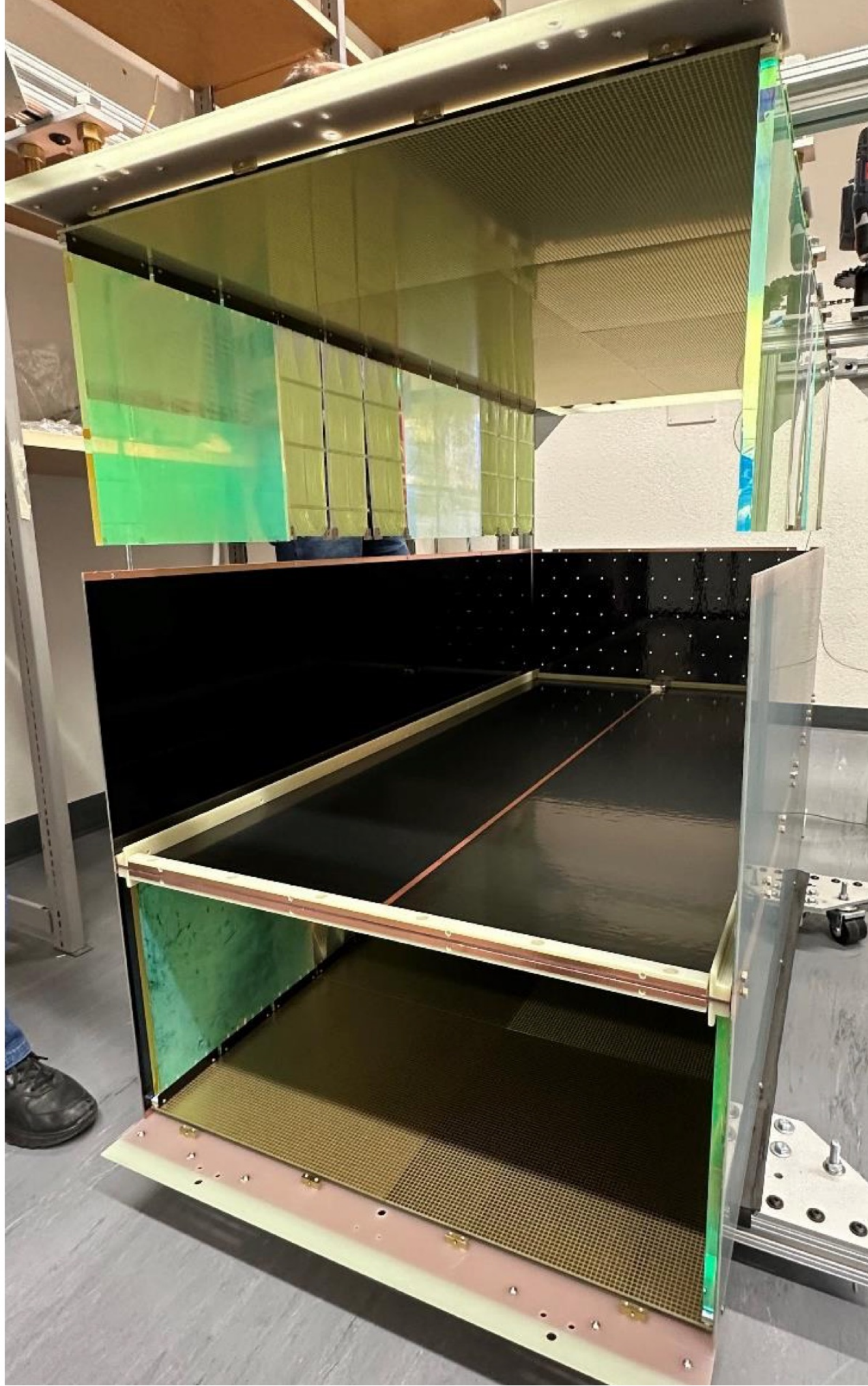
Supported by



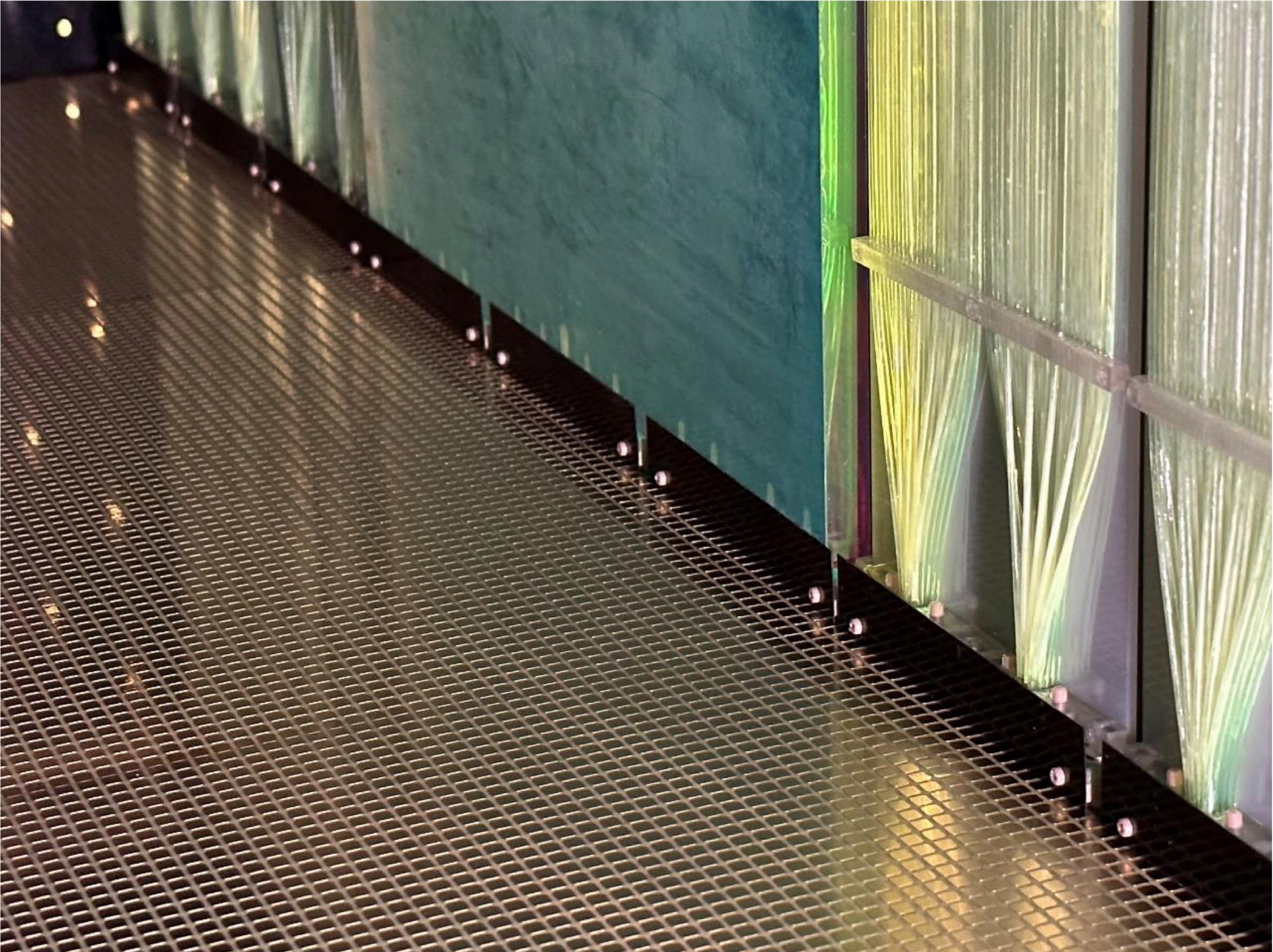
Russian
Science
Foundation

under grant #22-22-00389

Module assembly at Bern



Module assembly at Bern



Light system electronics shipped to Bern



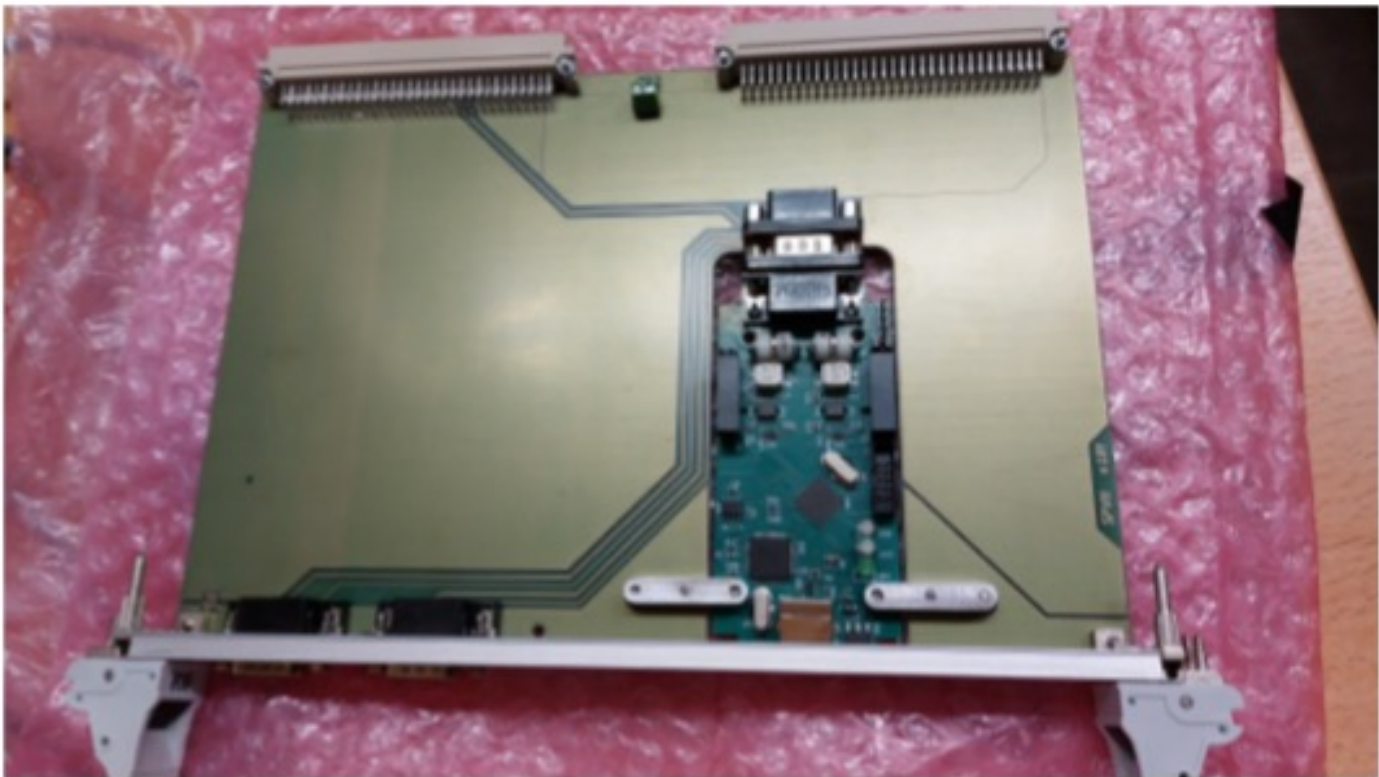
VGA board + Adaptor card for input micro coaxial cables



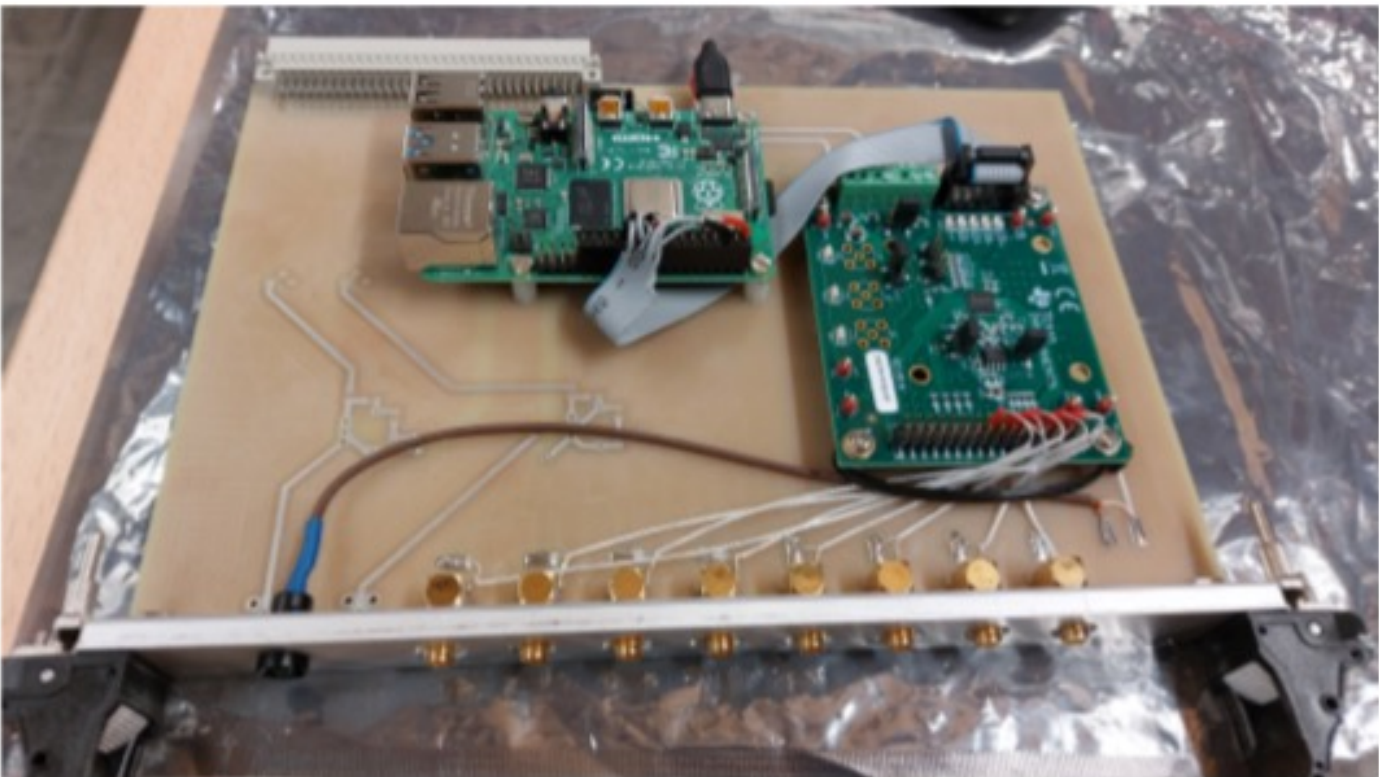
ADC board



Bias Power Supply



PS control unit



VGA control unit

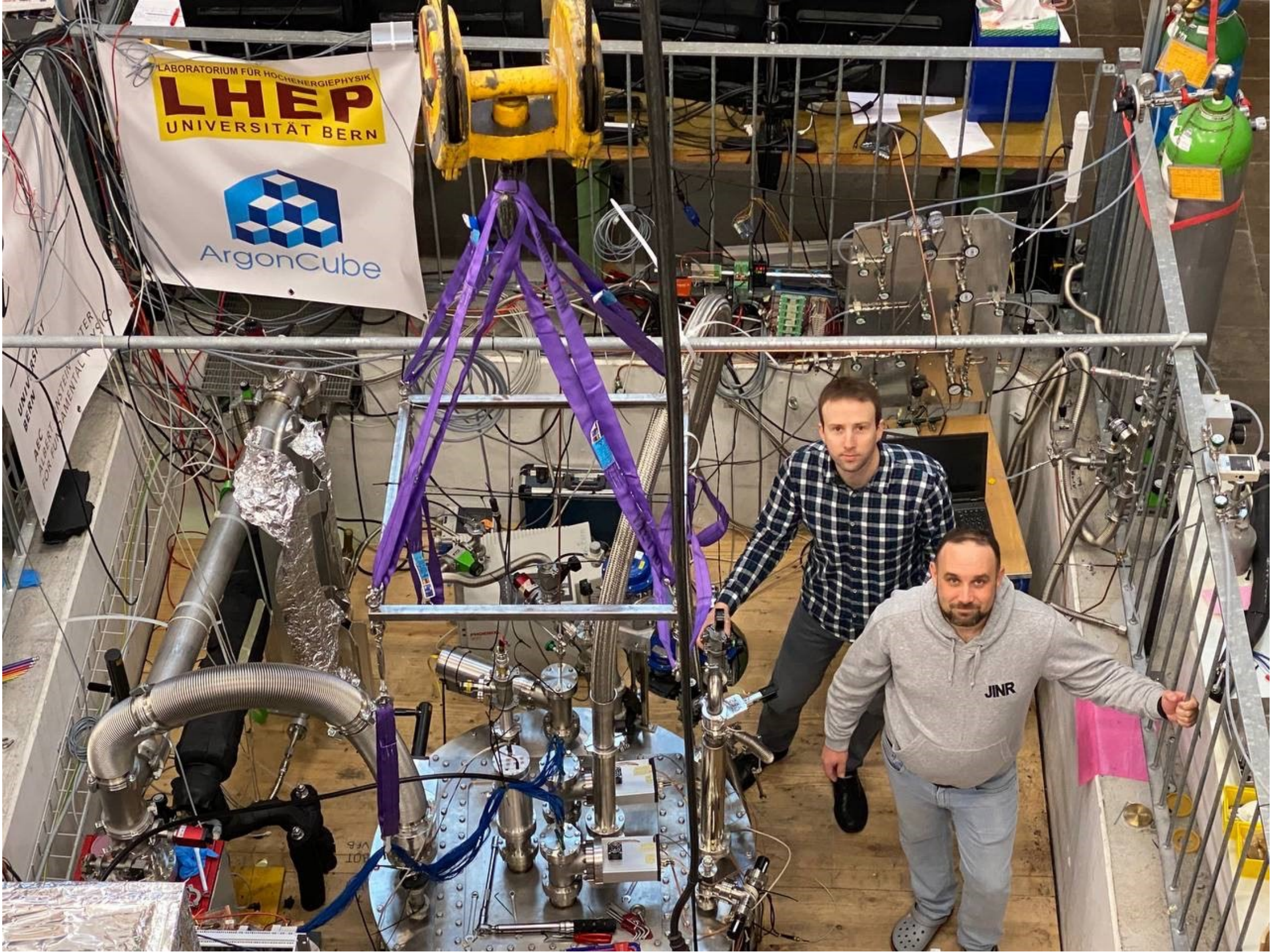
Module test at Bern



PS control VGA control PS bias

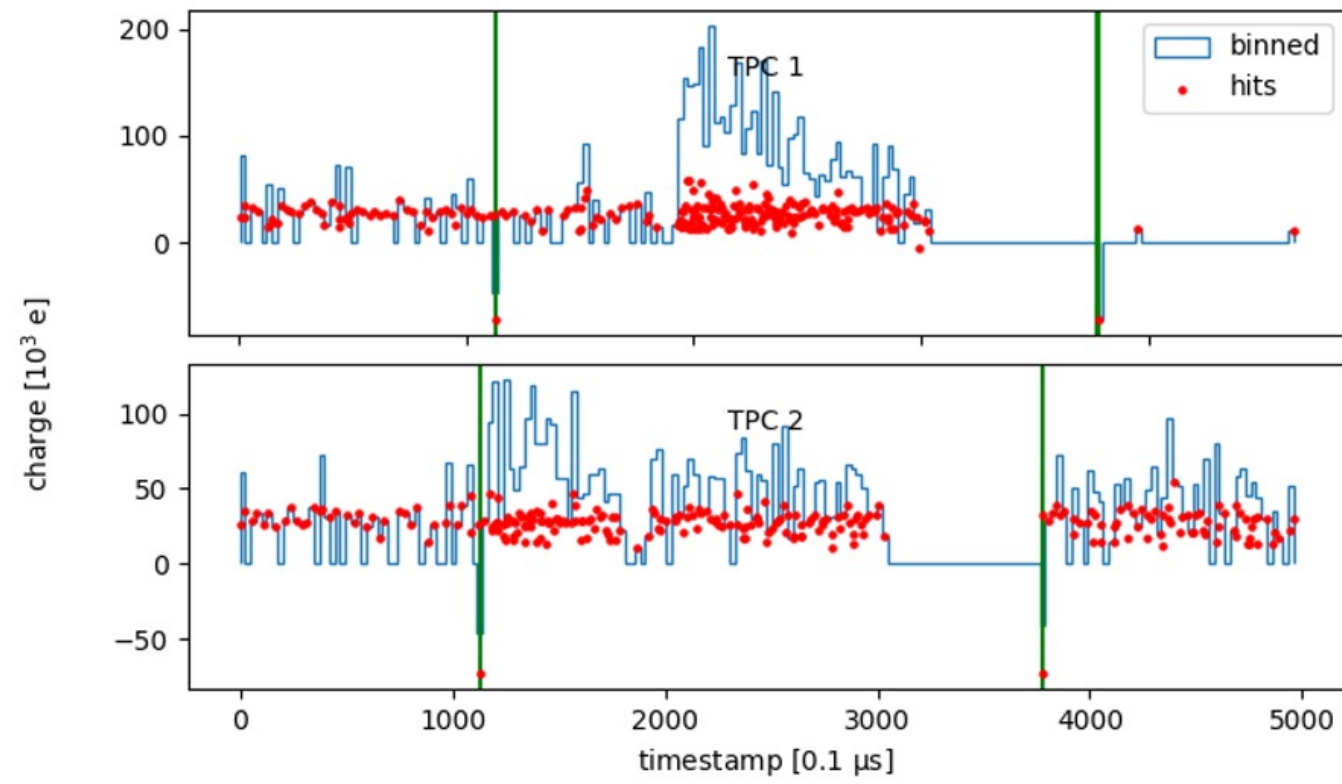
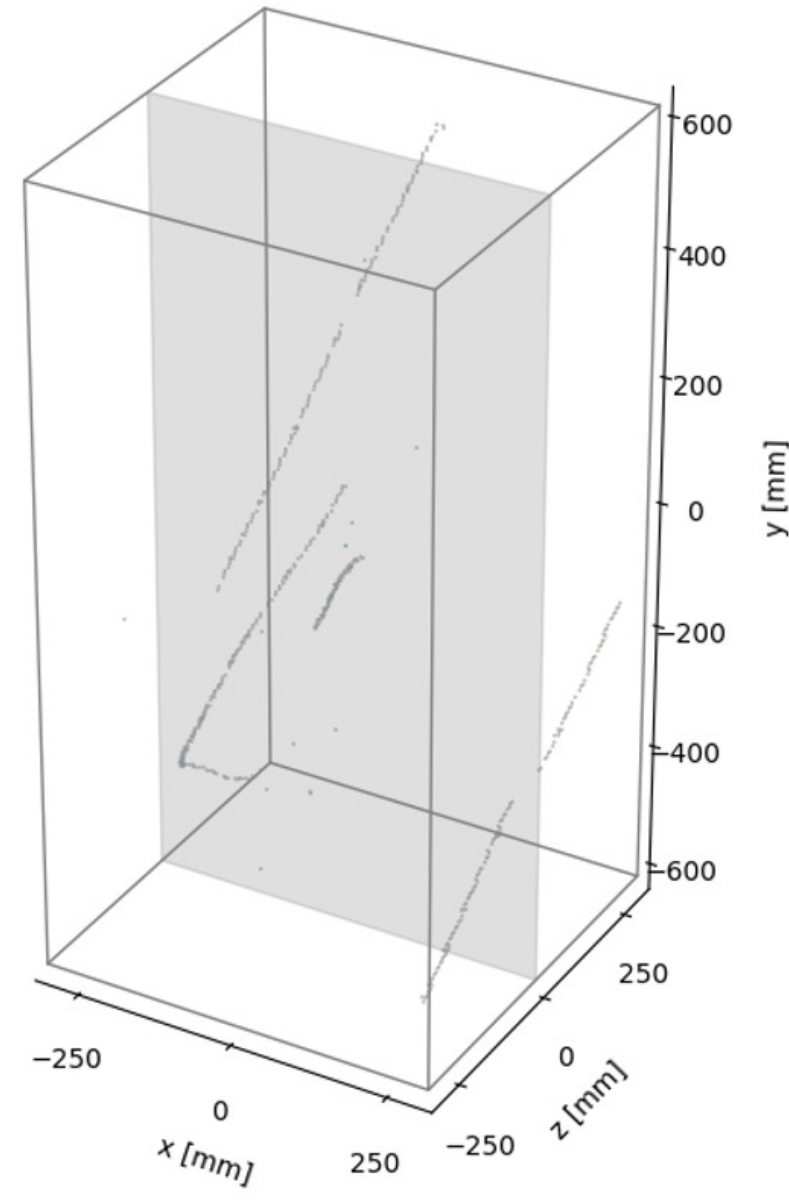
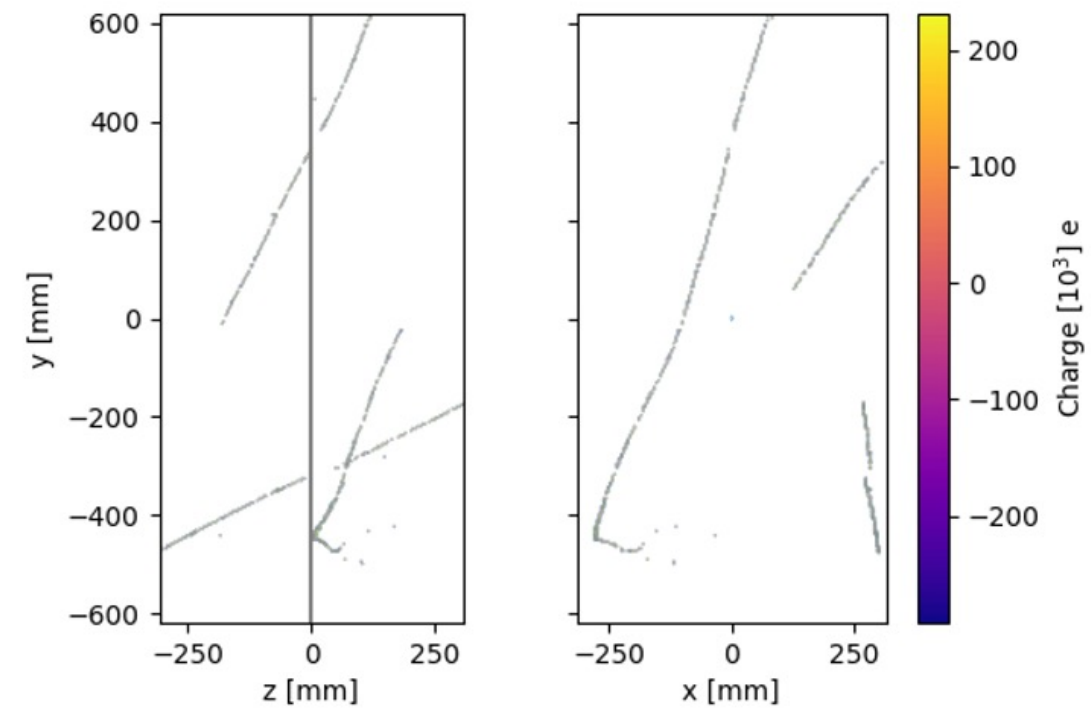
4 VGA

3 ADC

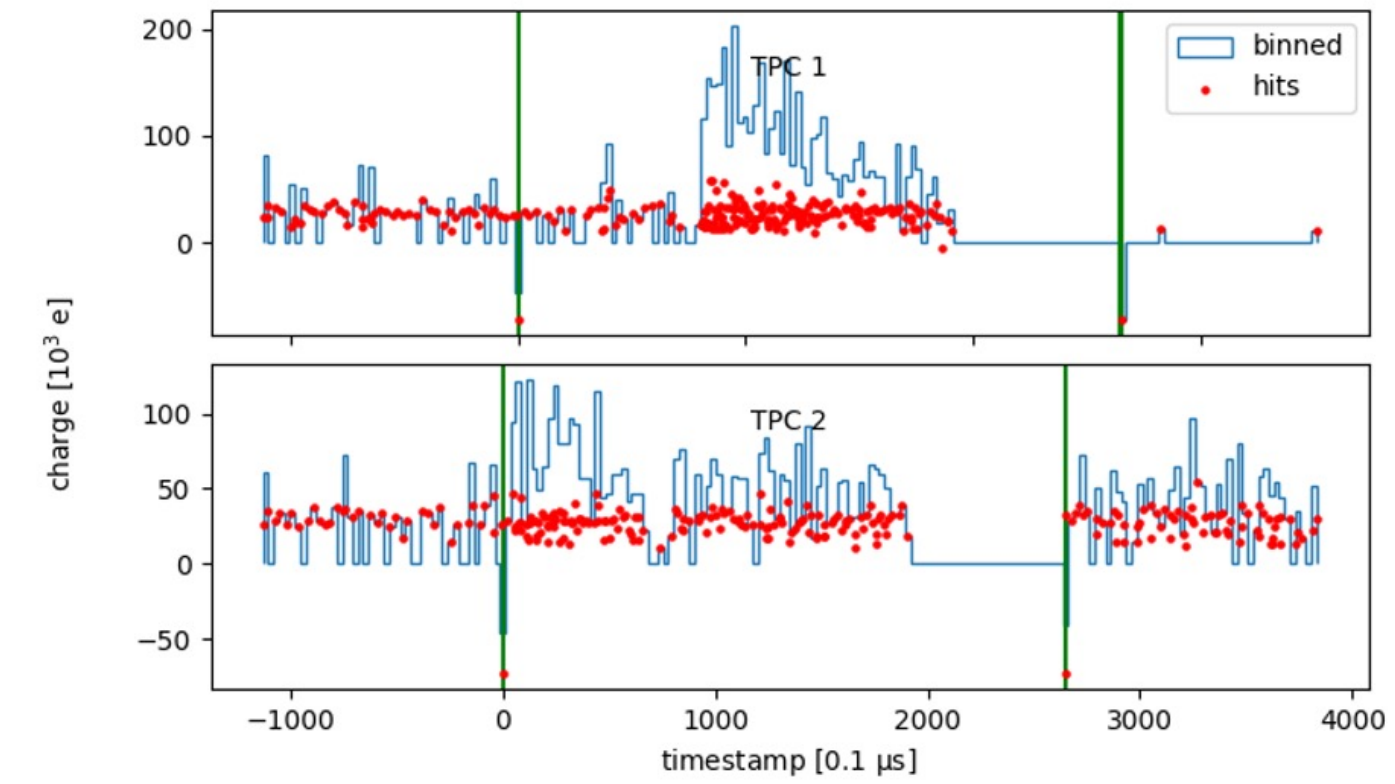
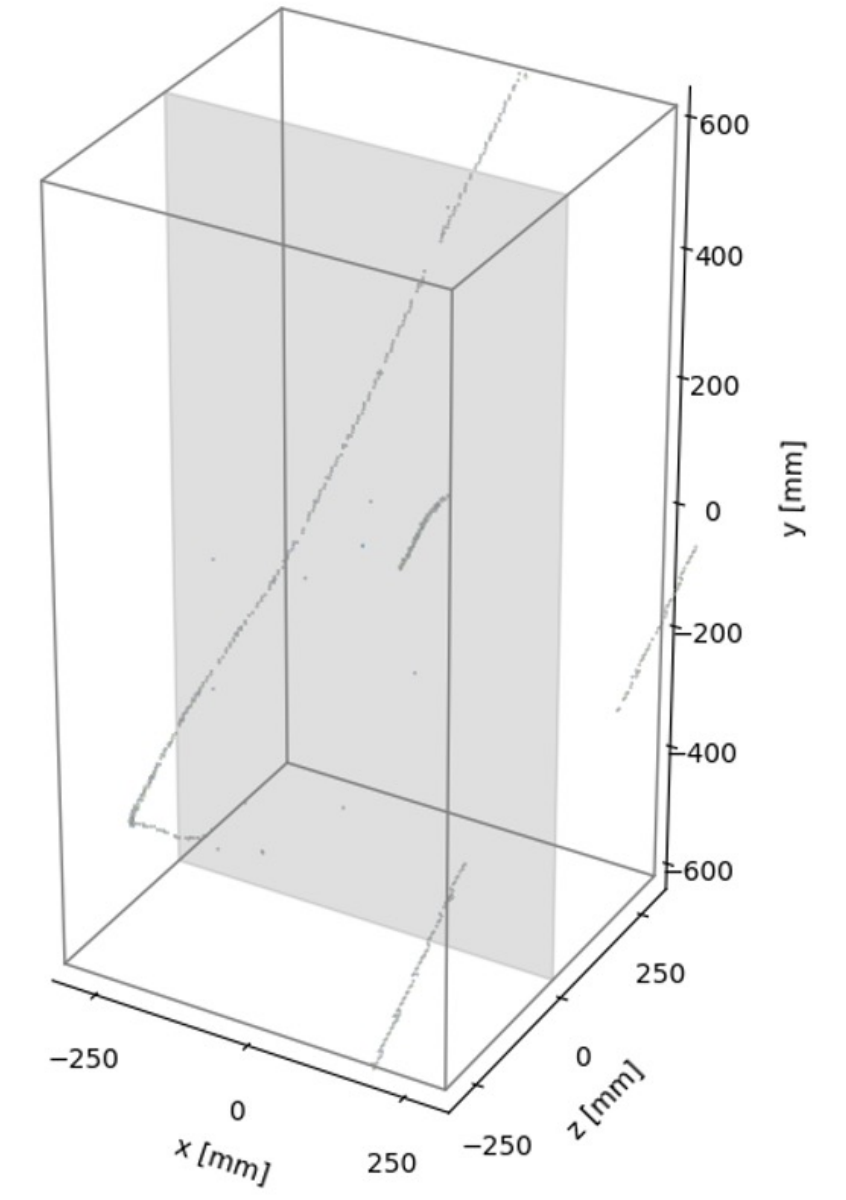
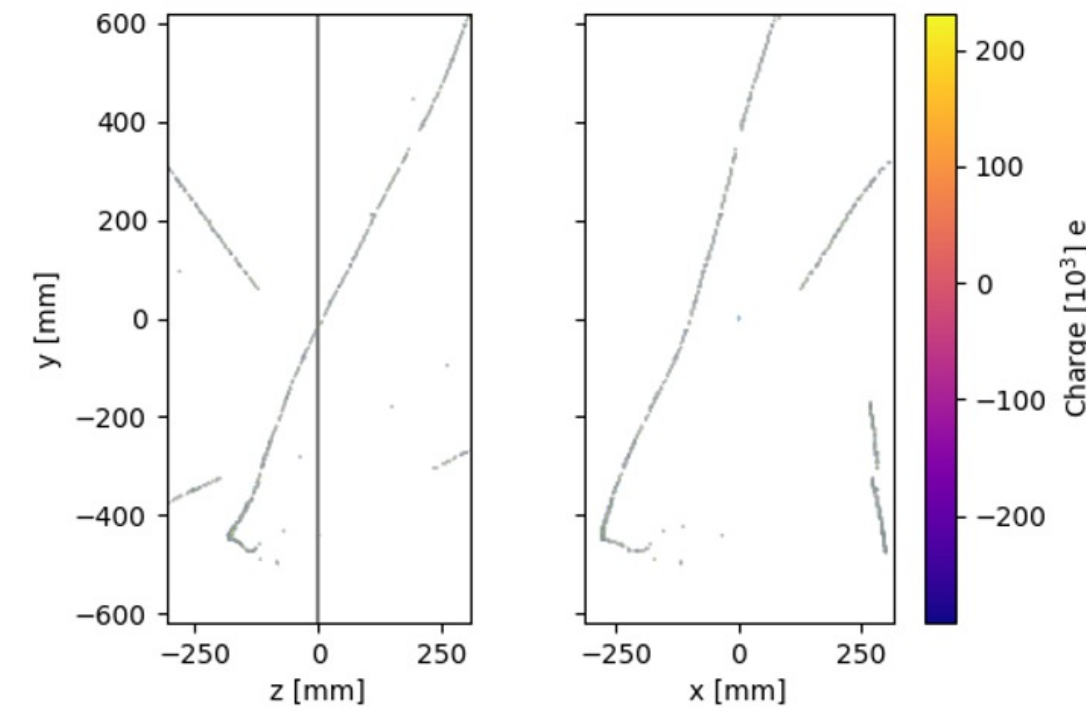


t0 correction using light detection system

Event 46, ID 130 - 2021-04-02 04:17:37 UTC

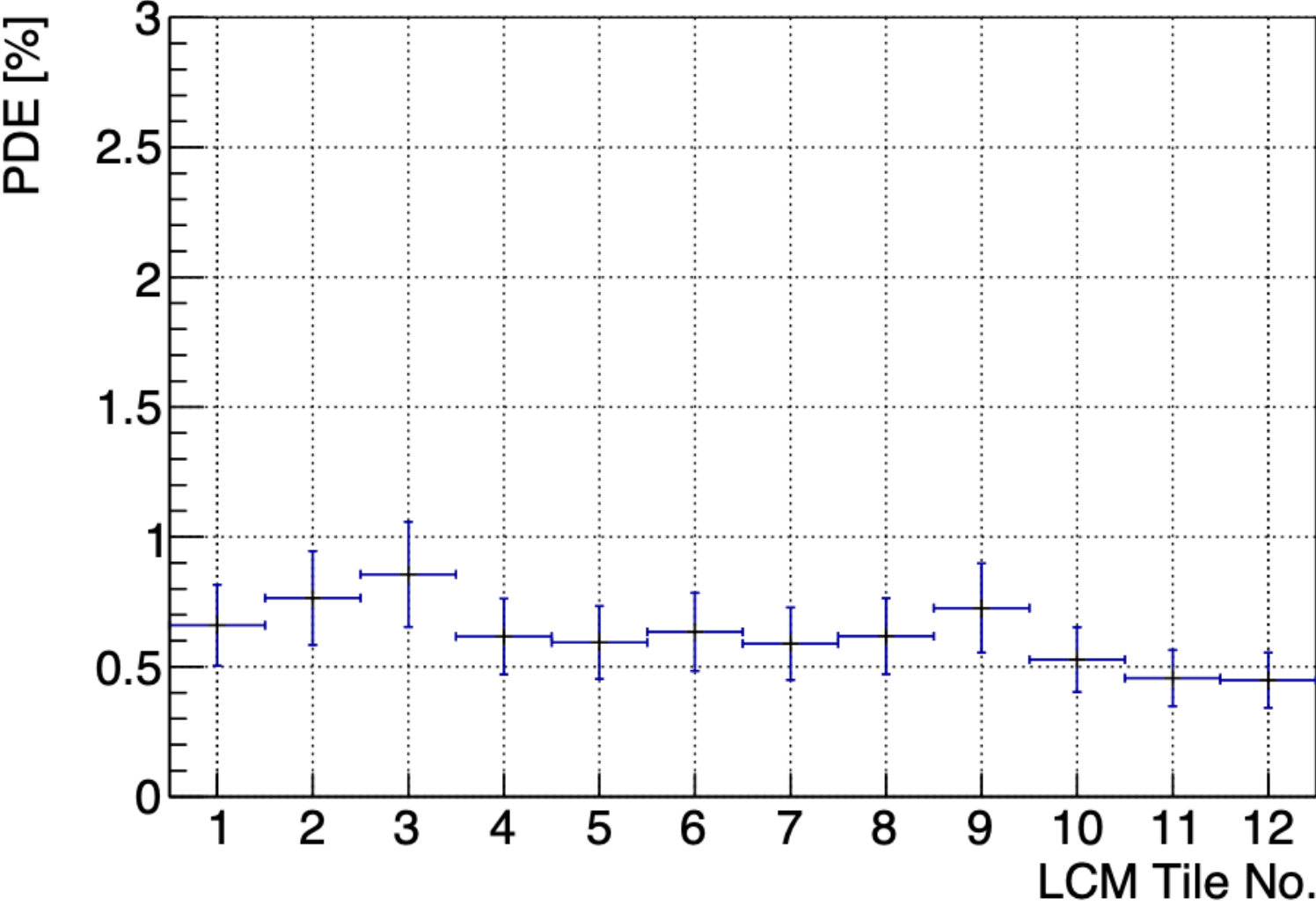


Event 46, ID 130 - 2021-04-02 04:17:37 UTC

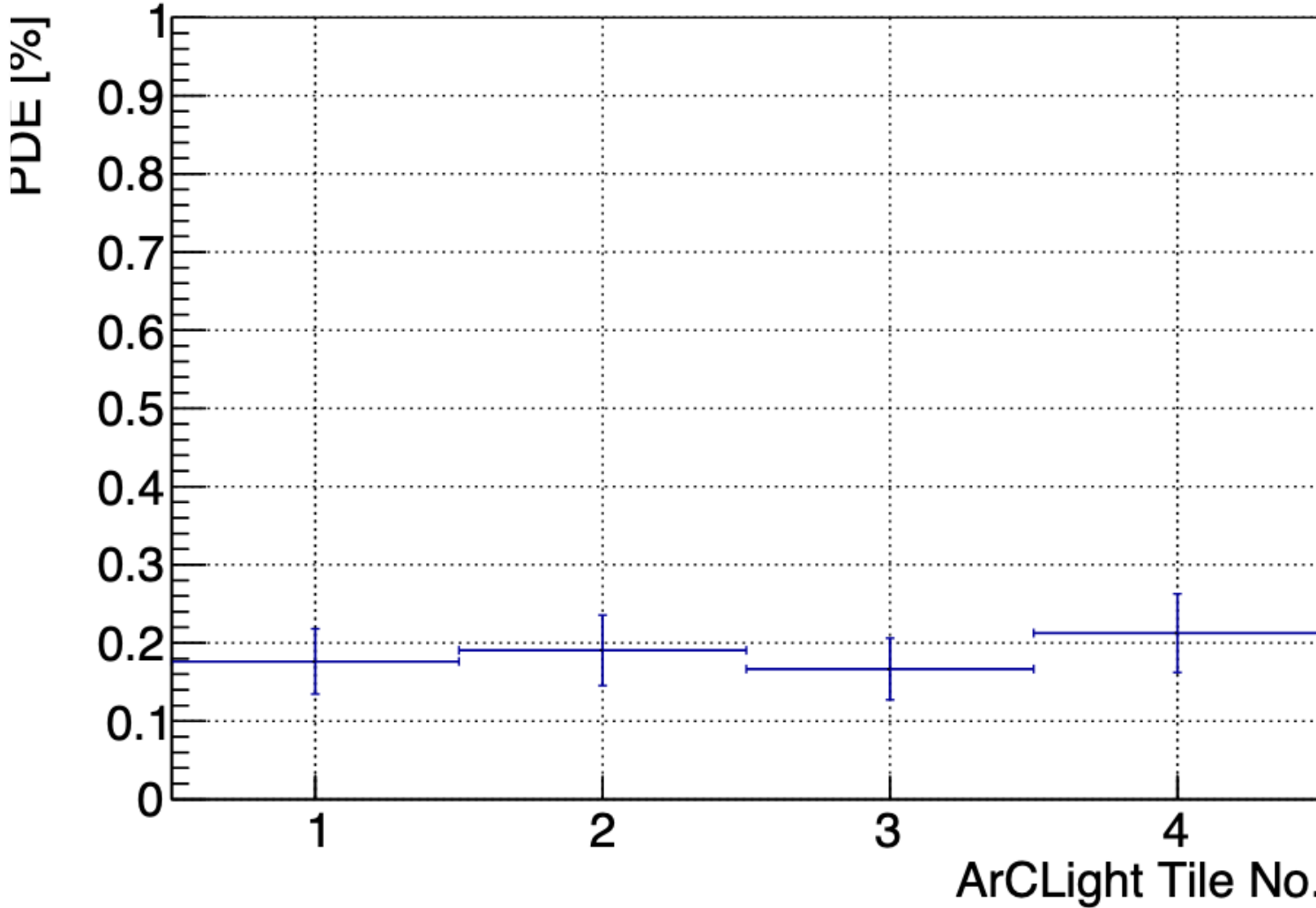


Light system performance

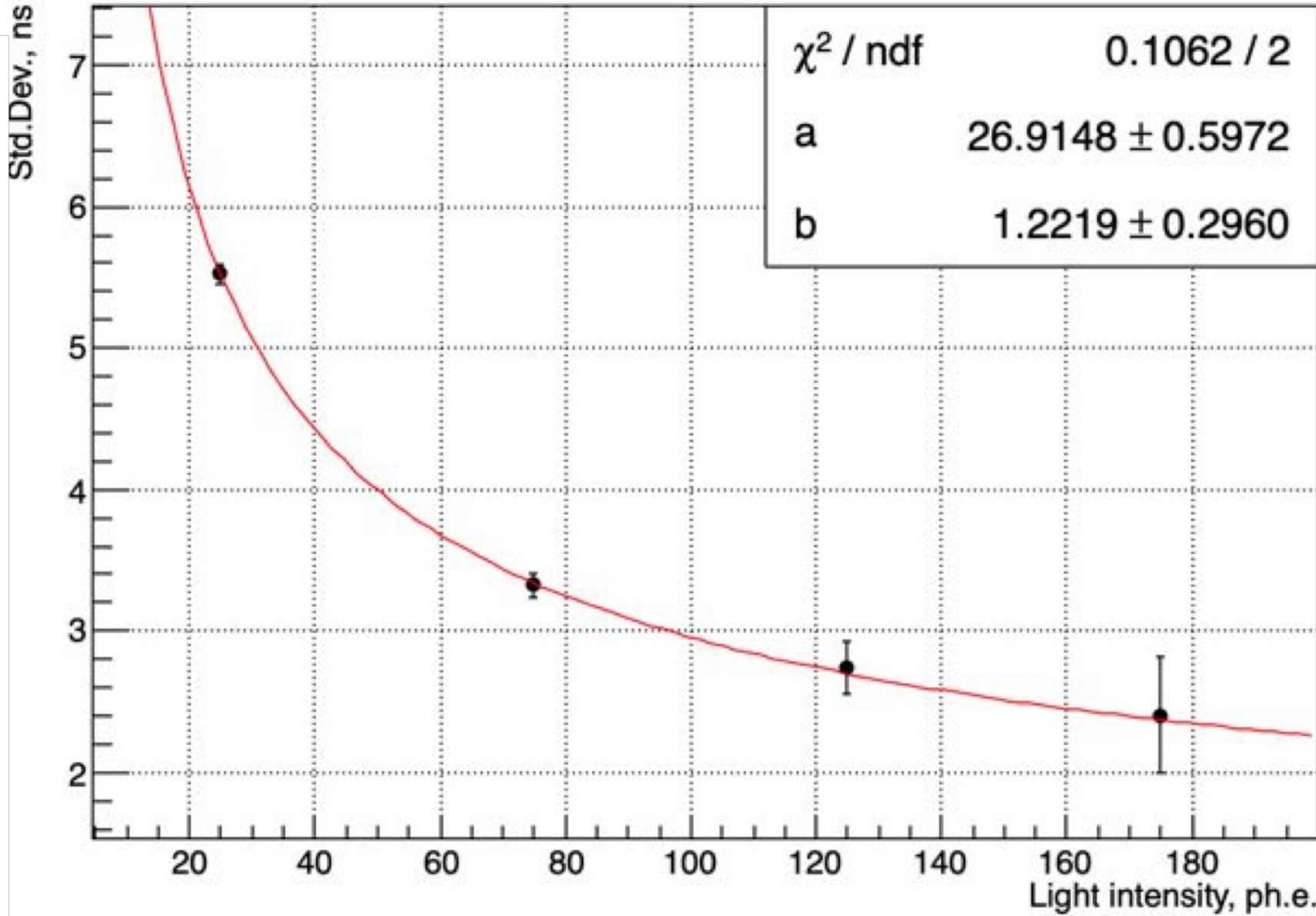
LCM PDE ~ 0.67 %



ACL PDE ~ 0.2%



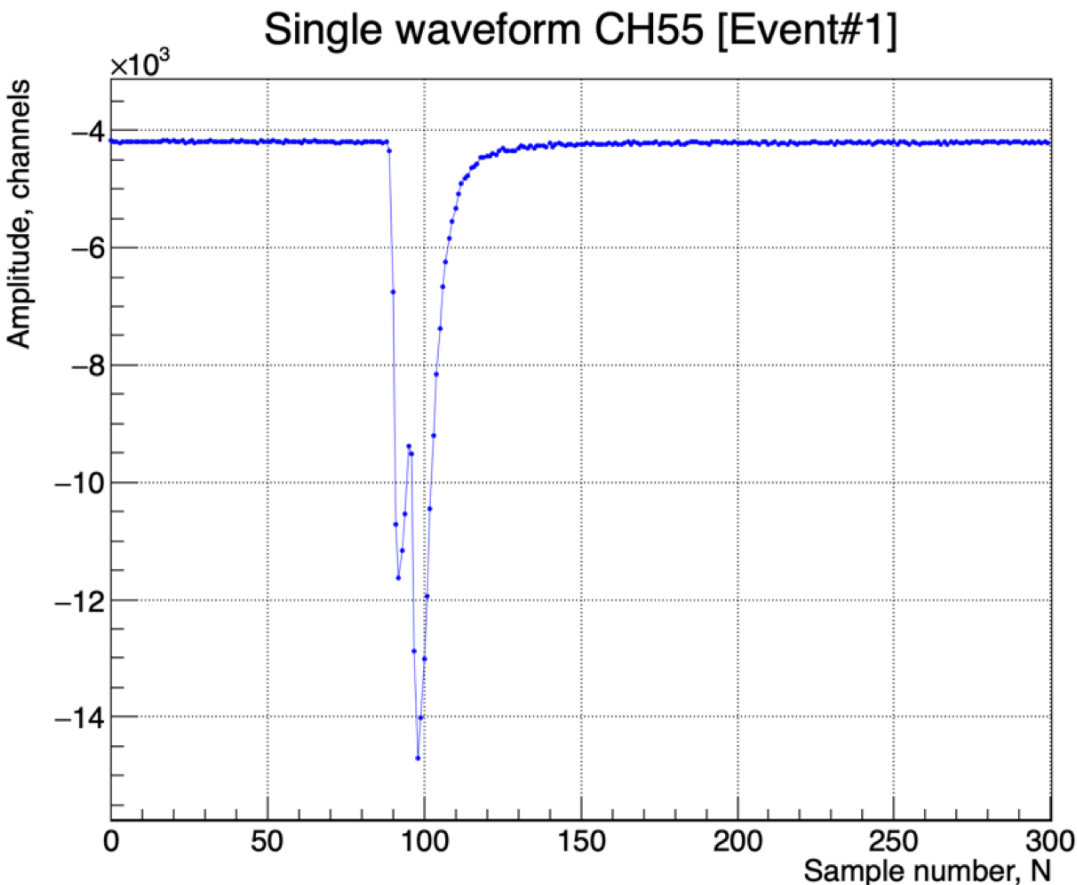
Time resolution [CH07&CH39]



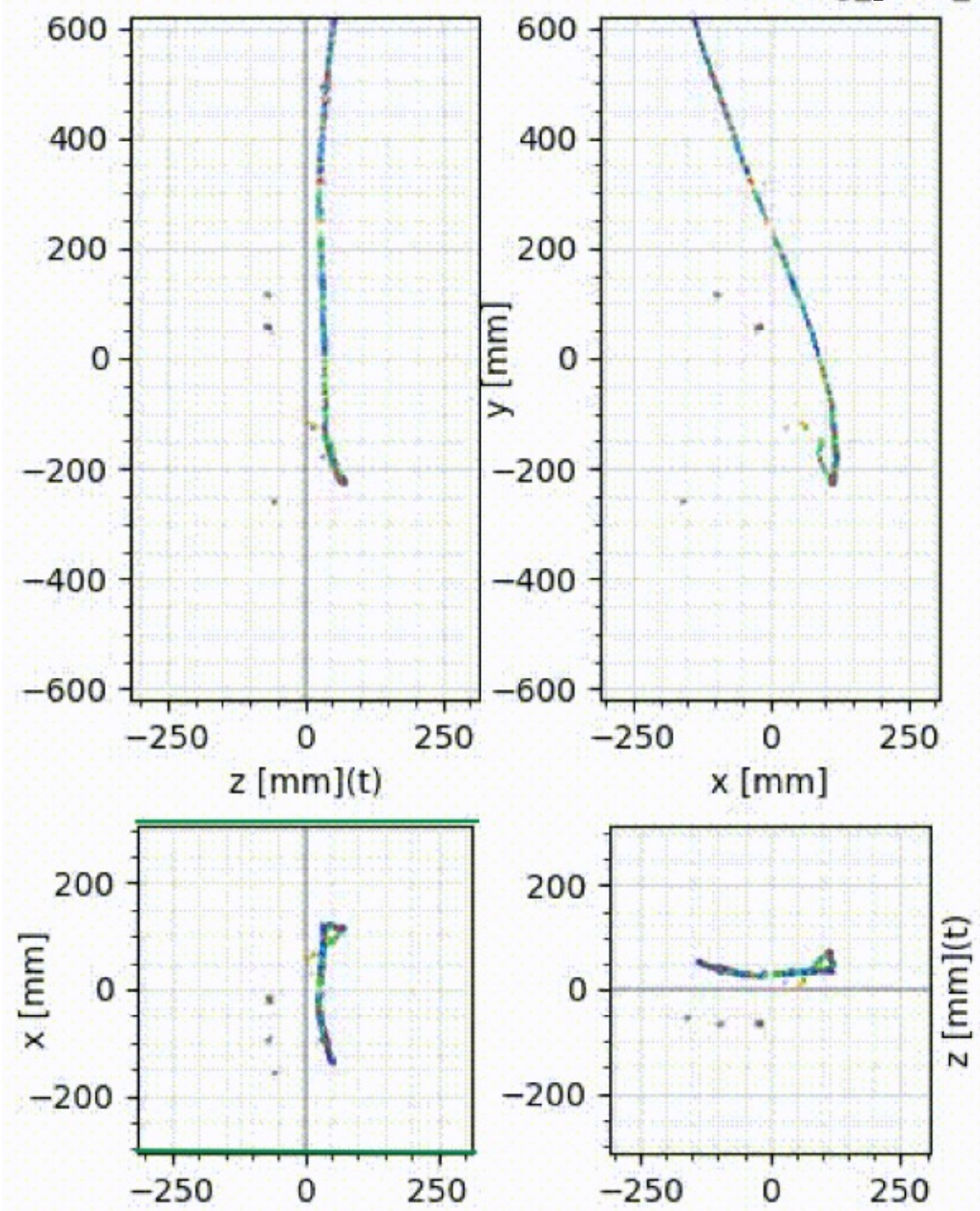
Light system performance

pile-up ~ 3-5 events/10us

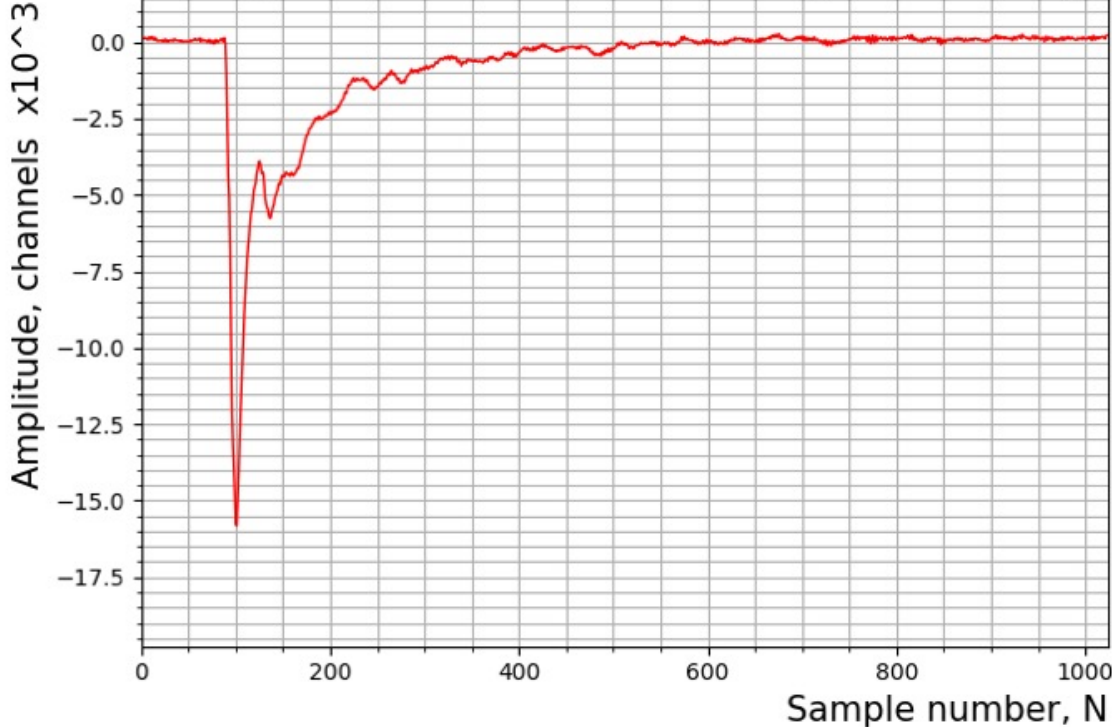
100 ns, LED double pulse



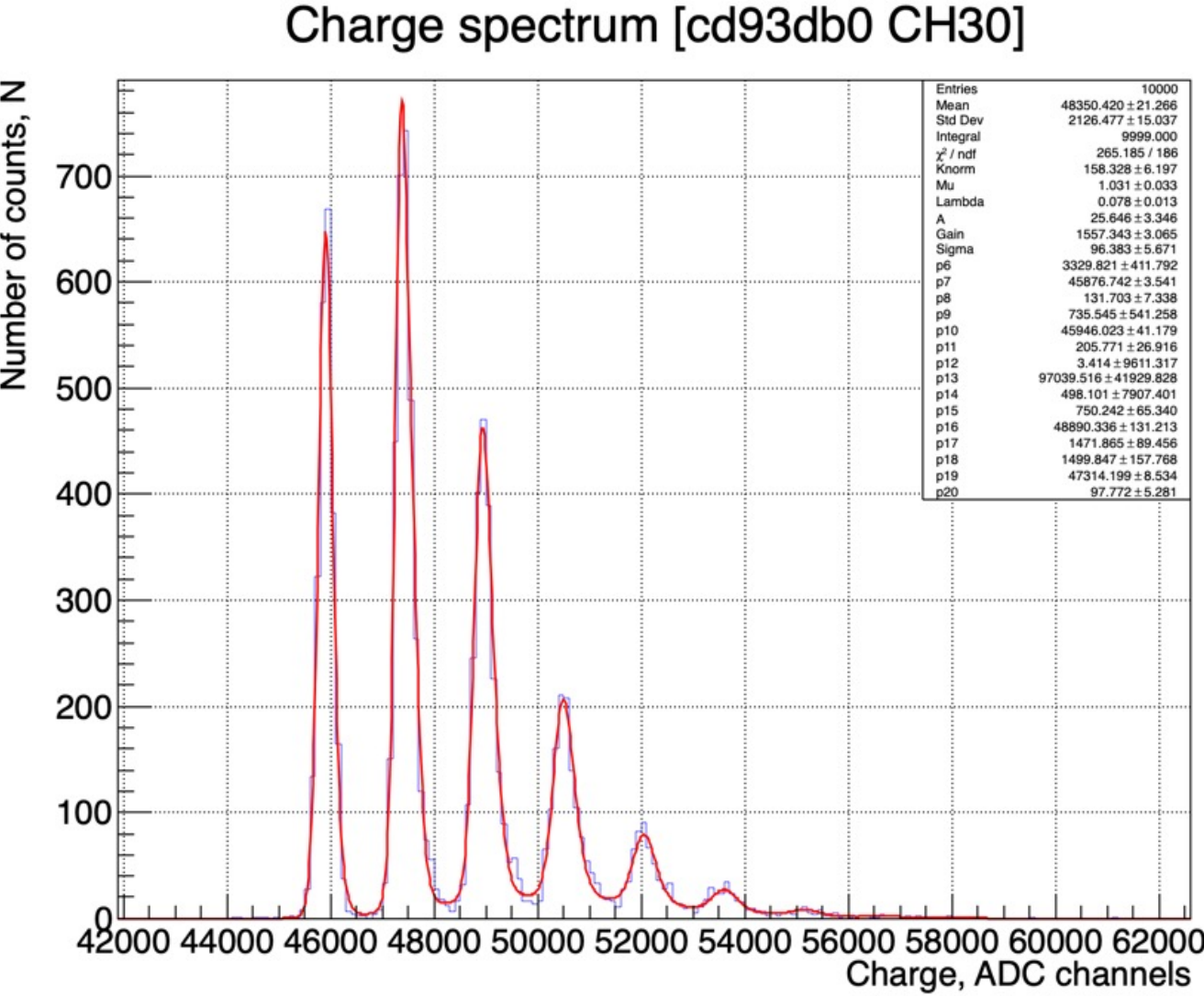
~250 ns pile-up, Michel event



Single wavform CH47 Event[# 139924]



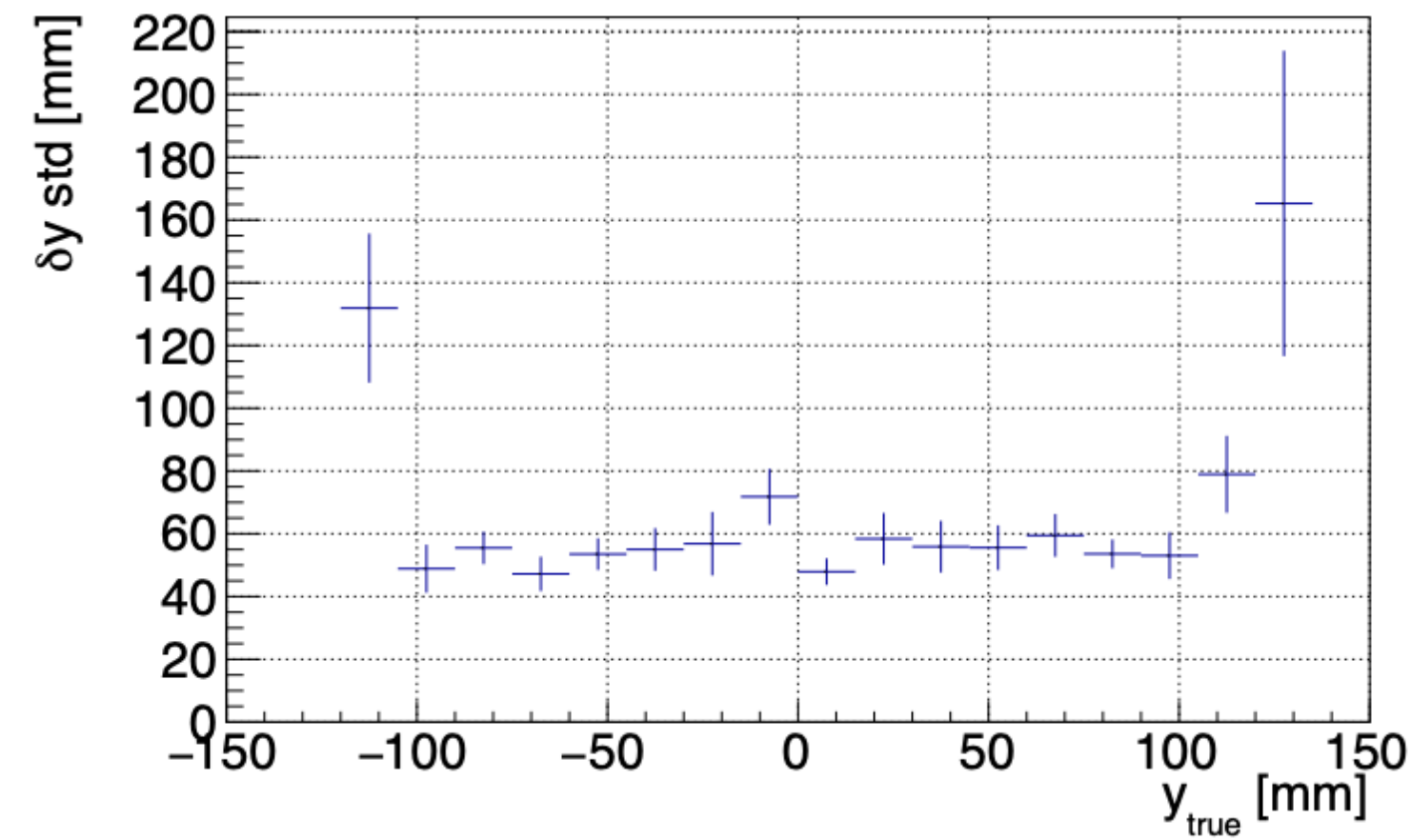
Calibration spectrum



Light system performance

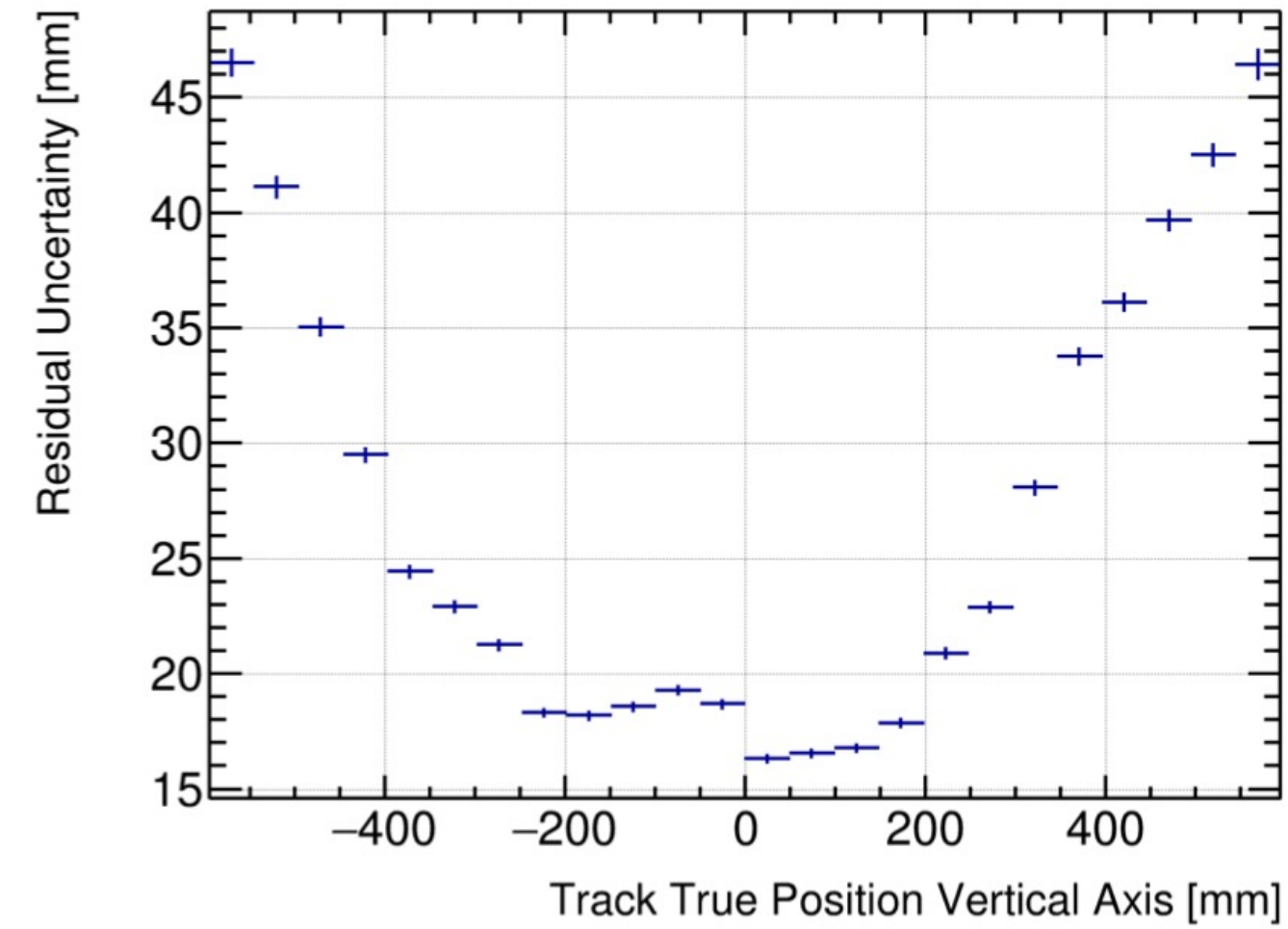
Spatial resolution (preliminary, Bern simulation)

ArCLight spatial resolution ~ 5-6cm



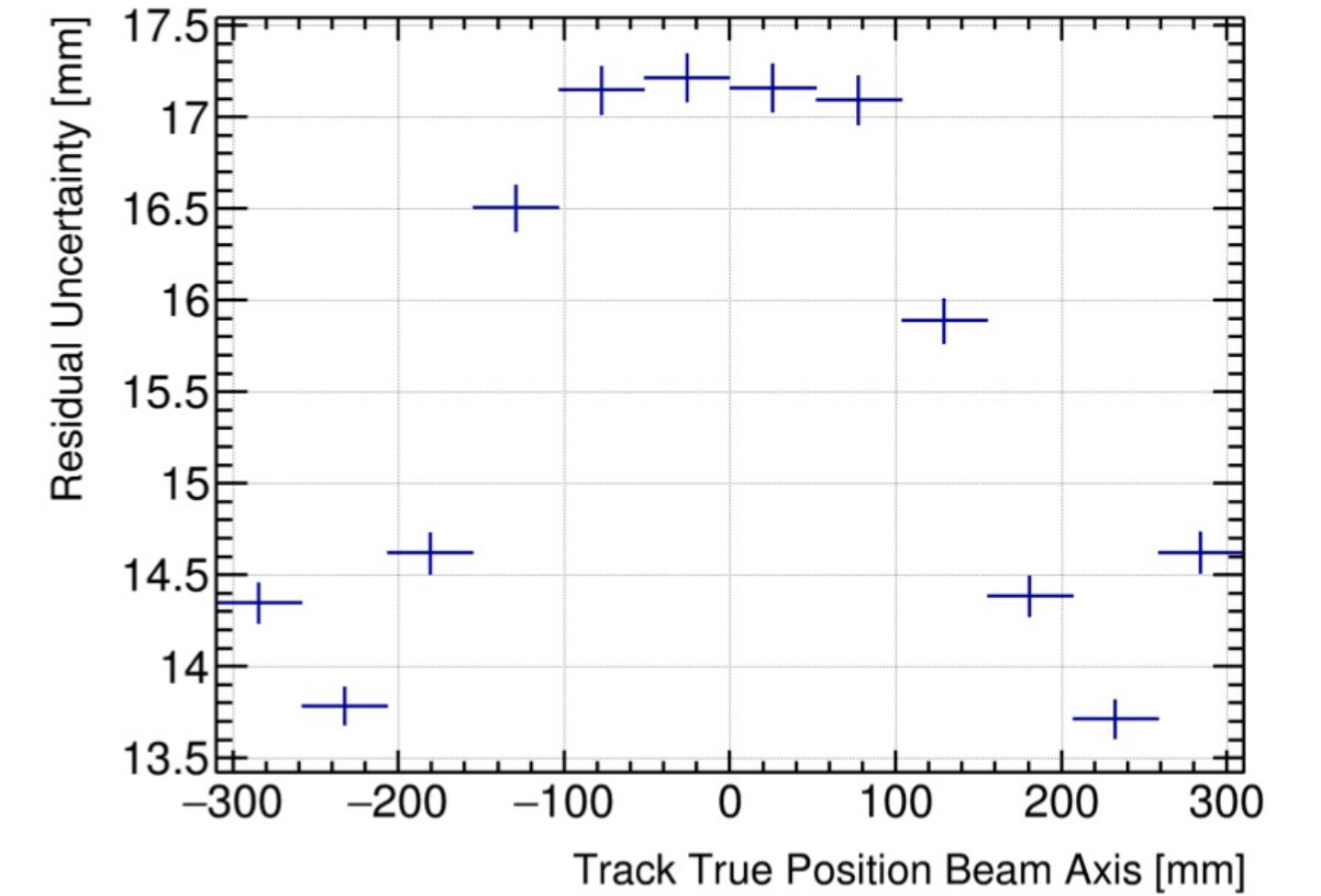
ArCLight spatial resolution reconstructed from SingleCube data (Vertical direction)

Common vertical spatial resolution ~ 2-4 cm



Light Readout spatial resolution simulation for ArgonCube TPC (Vertical direction)

Common spatial resolution along beam ~ 2 cm



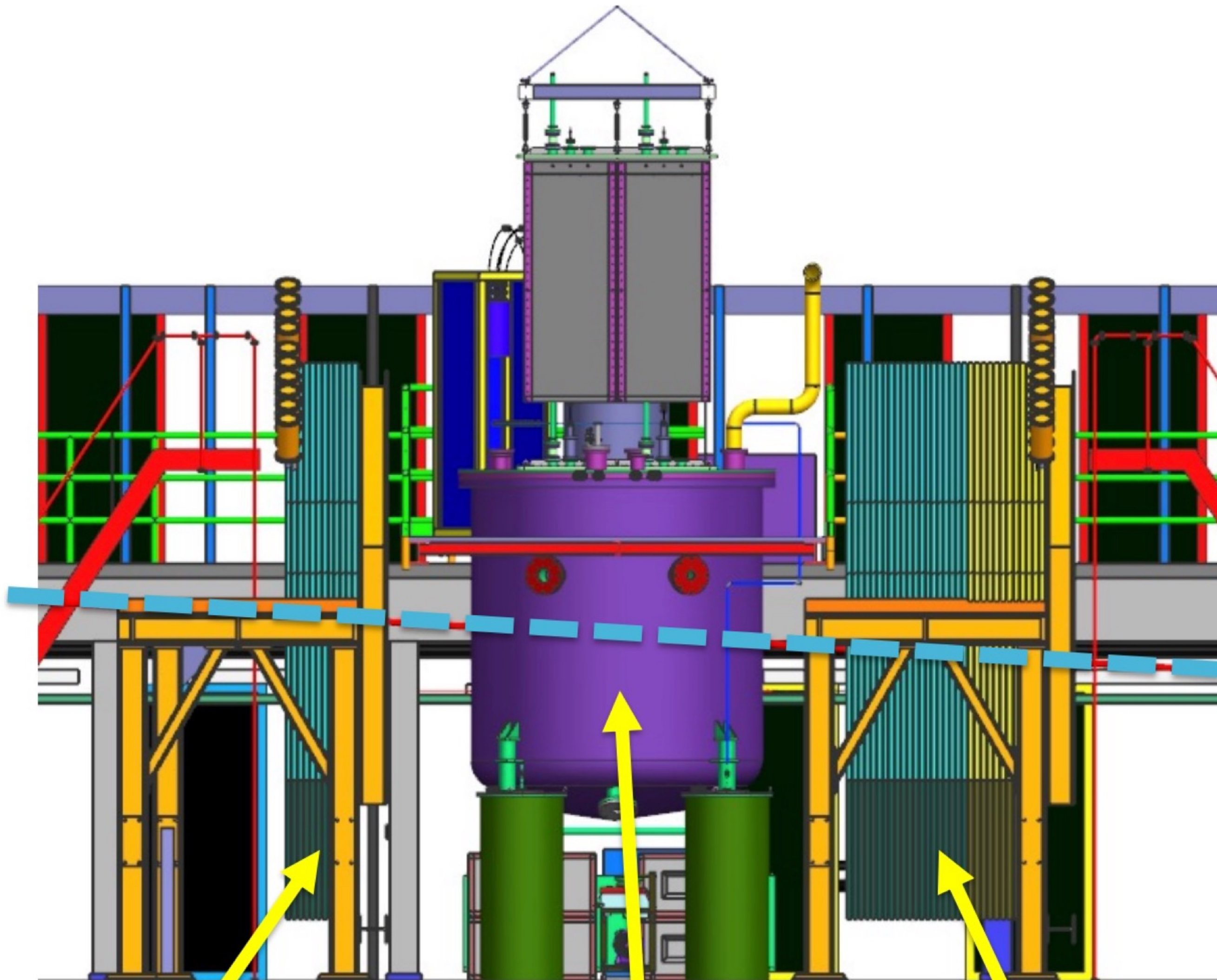
Light Readout spatial resolution simulation for ArgonCube TPC (along beam direction)

Module Performance Summary

	Module-0	Module-1	Module-2
LRS PDE: LCM	0.6%	0.7%	0.7%
LRS PDE: ArCLight	0.06%	0.2%	0.2%
LRS threshold	~ 5 MeV	~ 1.6 MeV	< 1.6 MeV
LRS timing	< 2 ns	1.2 ns	1.2 ns
LRS inactive channels ¹	8.3%	1.0%	0%
CRS threshold	5.8 ke- (~1/4 MIP)	4.5 ke- (~1/5 MIP)	7.5 ke- (~2/5 MIP)
CRS noise	920 e-	920 e-	830 e-
CRS inactive channels ²	7.8%	2.4%	9.0% ³
Electron lifetime	> 2 ms	> 2 ms	> 2 ms
Maximum electric field tested	1 kV/cm	0.5 kV/cm	0.8 kV/cm

By B. Russel, I. Kreslo

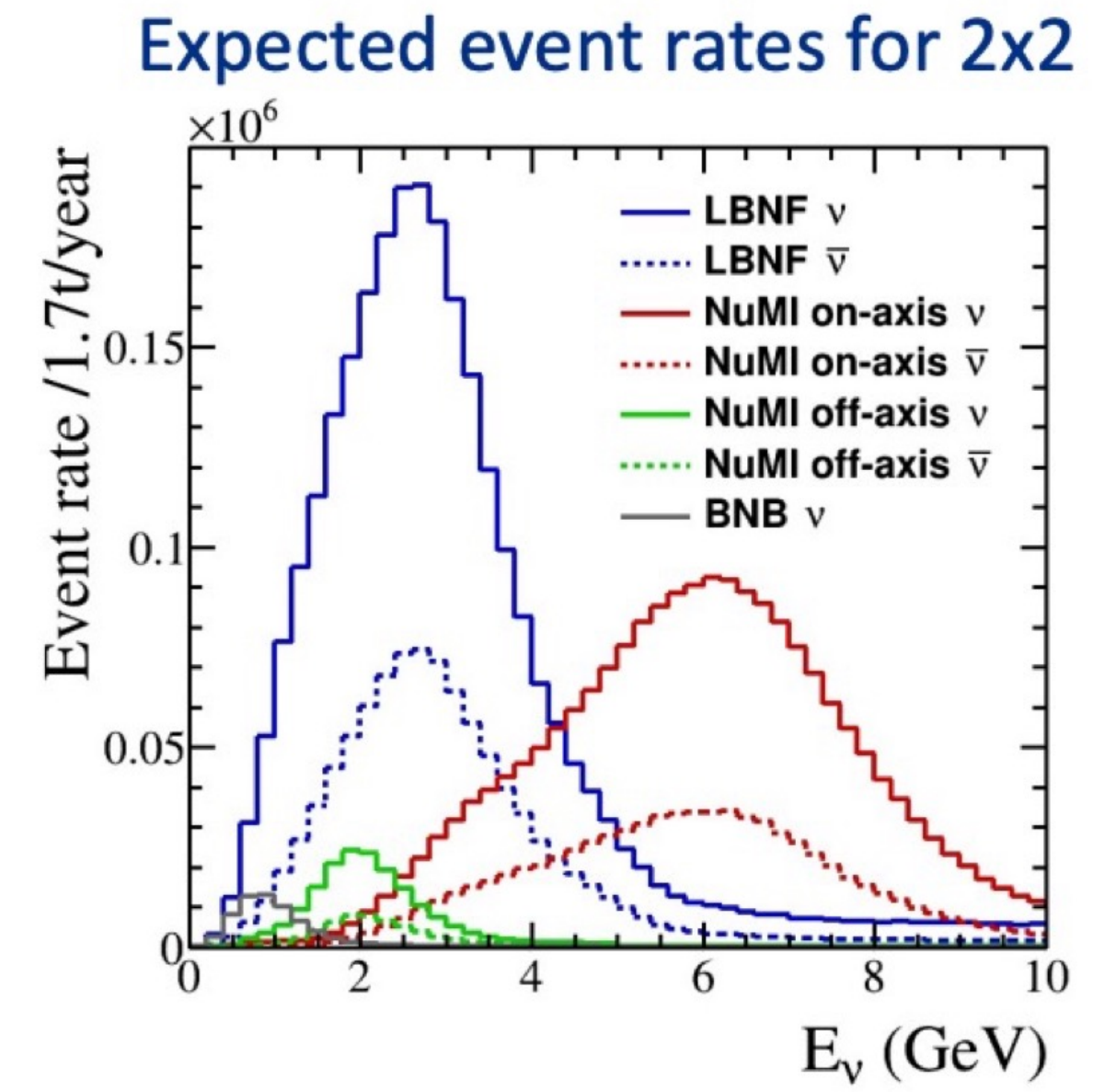
2x2 Demonstrator



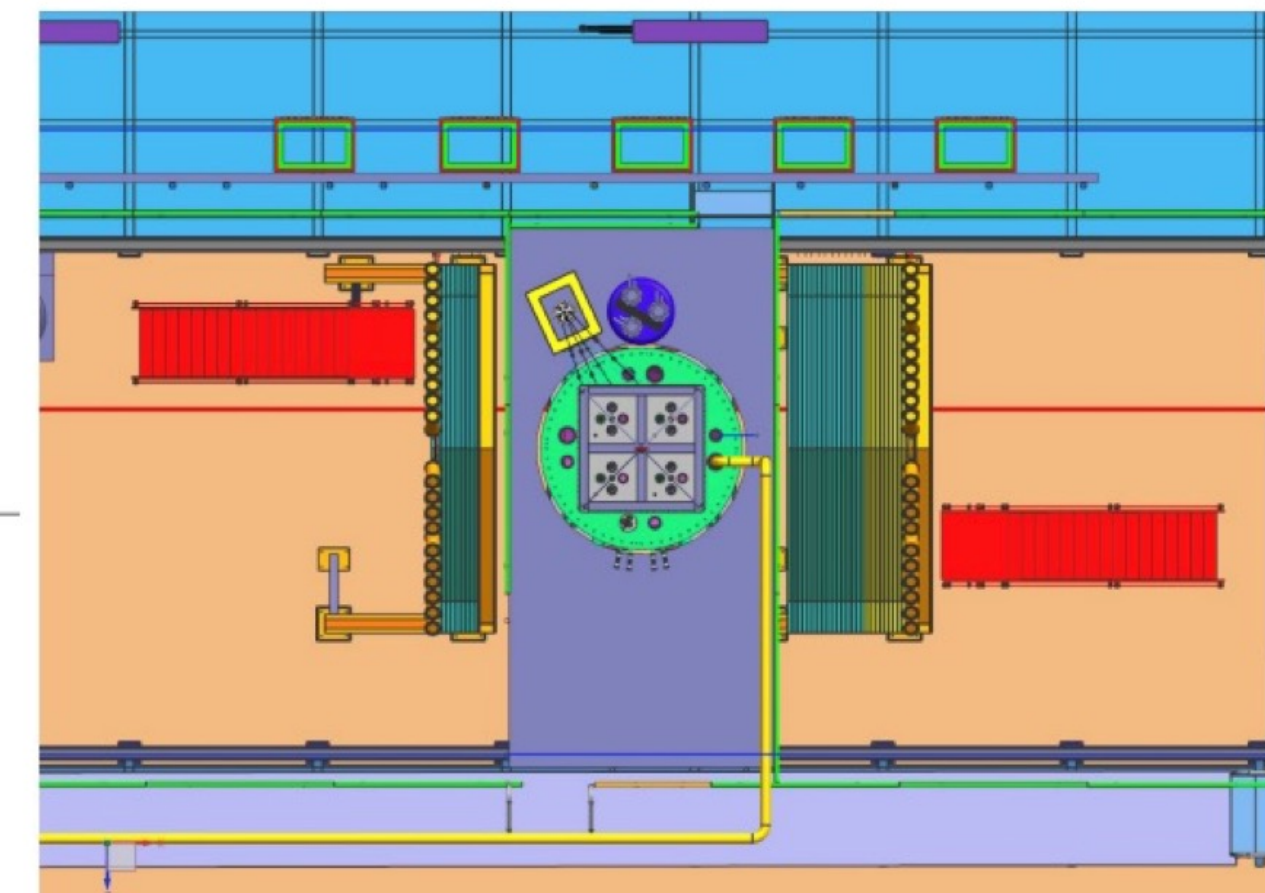
12 MINERvA
Modules

2x2 Cryostat
and 4 TPCs

32 MINERvA
Modules



NuMI Beamline



By J. Raaf

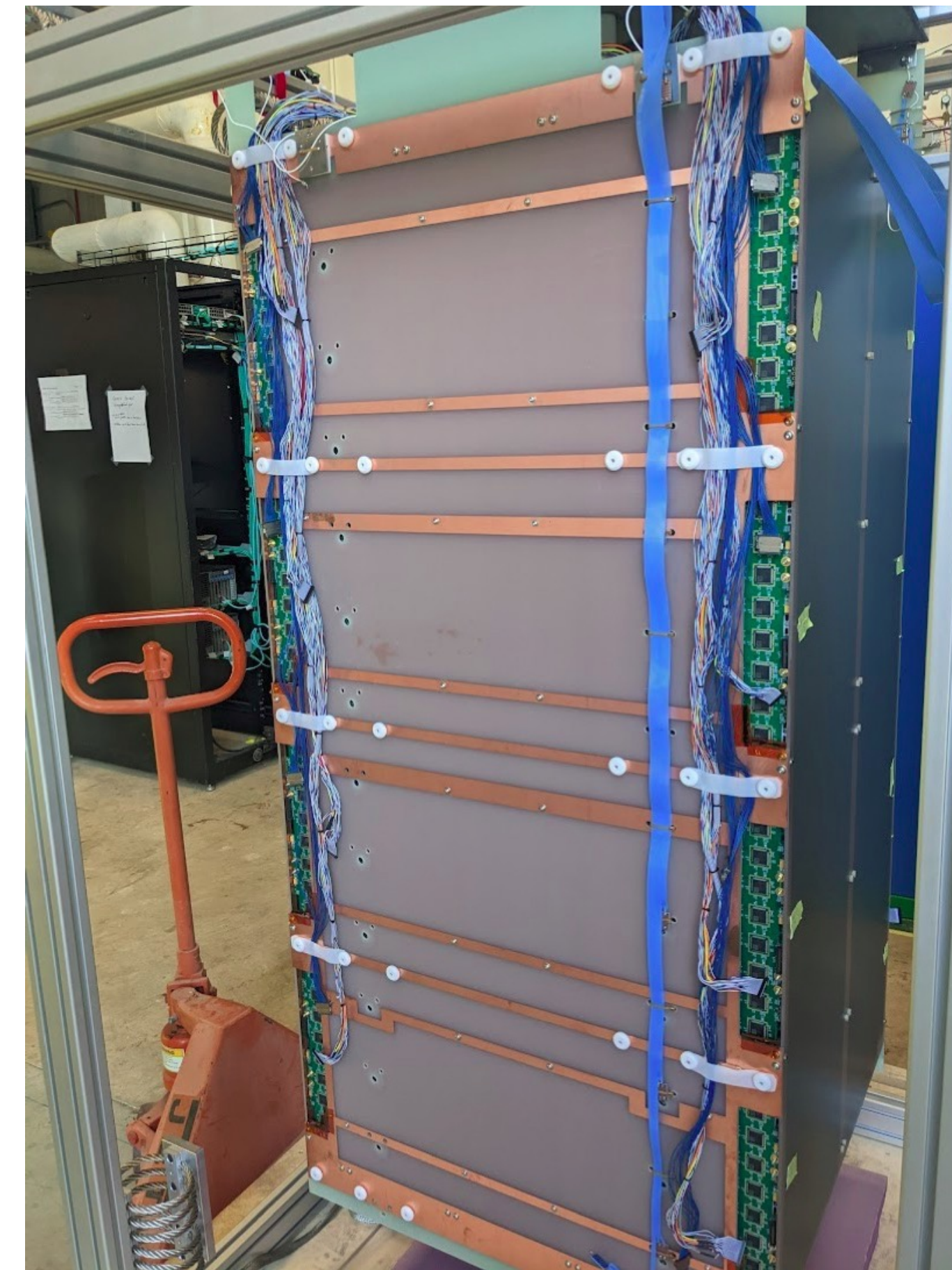
Electronic review at Fermilab 2022



DUNE-doc-#	Title	Author(s)	Topic(s)	Last Updated
25617-v5	Light Readout System DC distribution diagram for ArgonCube 2x2	Alexander Selyunin	ArgonCube2x2	12 Jul 2022
25657-v2	Light Readout System VGA control module ORC	Alexander Selyunin	ArgonCube2x2	09 Jun 2022
25655-v1	Light Readout System SiPM PS PCB ORC	Alexander Selyunin	ArgonCube2x2	08 Jun 2022
25653-v2	Light Readout System Adapter card ORC	Alexander Selyunin	ArgonCube2x2	08 Jun 2022
25650-v1	Light Readout System SiPM PS control board ORC	Alexander Selyunin	ArgonCube2x2	08 Jun 2022
24754-v3	Light System ADC64ve_v3.2	Alexander Selyunin	ArgonCube2x2	02 Jun 2022
24868-v3	Light System VGA board	Alexander Selyunin	ArgonCube2x2	01 Jun 2022

Modules preparation for 2x2 at Fermilab

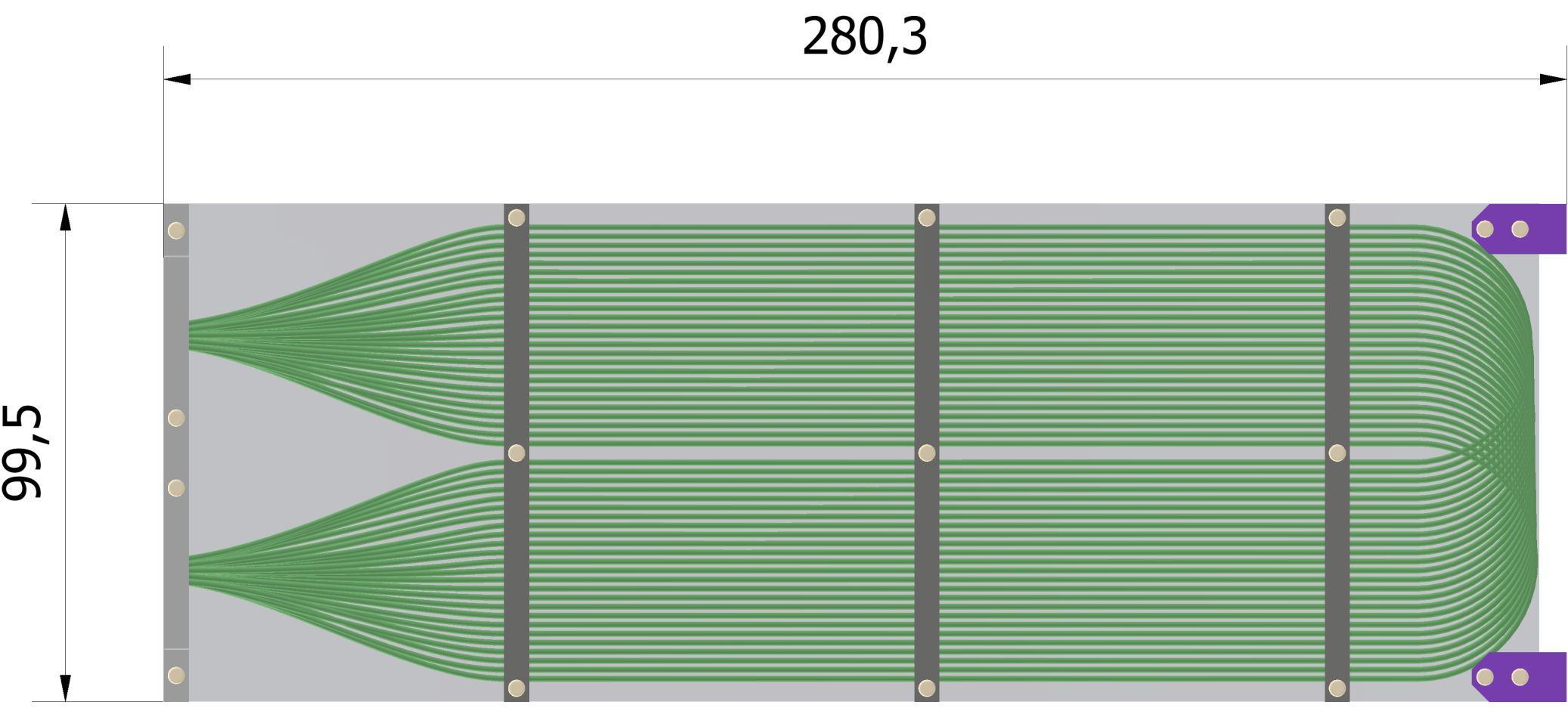
- 3 Modules delivered to FNAL
- QA/QC testing after shipment
- 2x2 cryostat installed



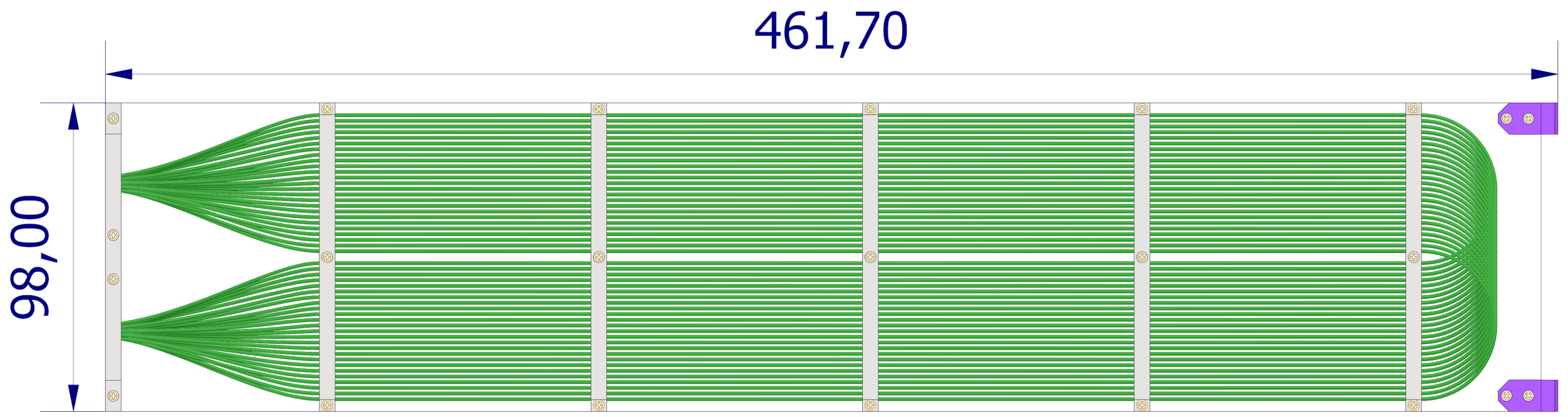
Key Documents for Preliminary Design Review

Light Readout Documentation	Description	EDMS Link
Light Readout Folder	Top level folder for Light Readout documentation	https://edms.cern.ch/project/CERN-0000217529
Requirements	Spreadsheet with all ND-LAr requirements, see sheet "Light Readout (06)"	https://edms.cern.ch/document/2589287
Internal ICDs	Interface control documents (ICDs) internal to the ND-LAr Consortium	https://edms.cern.ch/project/CERN-0000223195
Analyses	Collection of analyses write-up: FEAs, bench testing, 2x2 prototype evaluations	https://edms.cern.ch/project/CERN-0000231222
QAQC Plan	Subsystem QAQC plan with focus on high-level QAQC test plans	https://edms.cern.ch/document/2587876
Manufacturing Plan	Subsystem Manufacturing plan with focus on manufacturing methods of key items	https://edms.cern.ch/document/2605604
Procurement Plan	Subsystem Procurement plan with focus on procurement management of key items	https://edms.cern.ch/document/2605605
Previous Review Tracking	Spreadsheet with previous review recommendations, see "Light Readout"	https://edms.cern.ch/document/2741842
Cost	High-level cost estimate for ND-LAr and subsystems	https://edms.cern.ch/document/2742778
Schedule	High-level "one-pager" schedule for ND-LAr Consortium activities	https://edms.cern.ch/document/2603073
CAD Model (Row Assembly, TPC Assembly)	Solidworks "Pack & Go" and Parasolid exports of CAD models	https://edms.cern.ch/project/CERN-0000230732
Mechanical Component Drawings	Subsystem mechanical component drawings	https://edms.cern.ch/project/CERN-0000218197
Mechanical Assembly Drawings	Subsystem assembly drawing	https://edms.cern.ch/project/CERN-0000218198
Parts List	Subsystem parts list	https://edms.cern.ch/project/CERN-0000220723
Electrical Schematics and Board Layouts	Subsystem electrical schematics and board layouts	https://edms.cern.ch/project/CERN-0000218199
Electrical Cabling and Wiring Specification	Specification of electrical cables/wiring	https://edms.cern.ch/project/CERN-0000217668

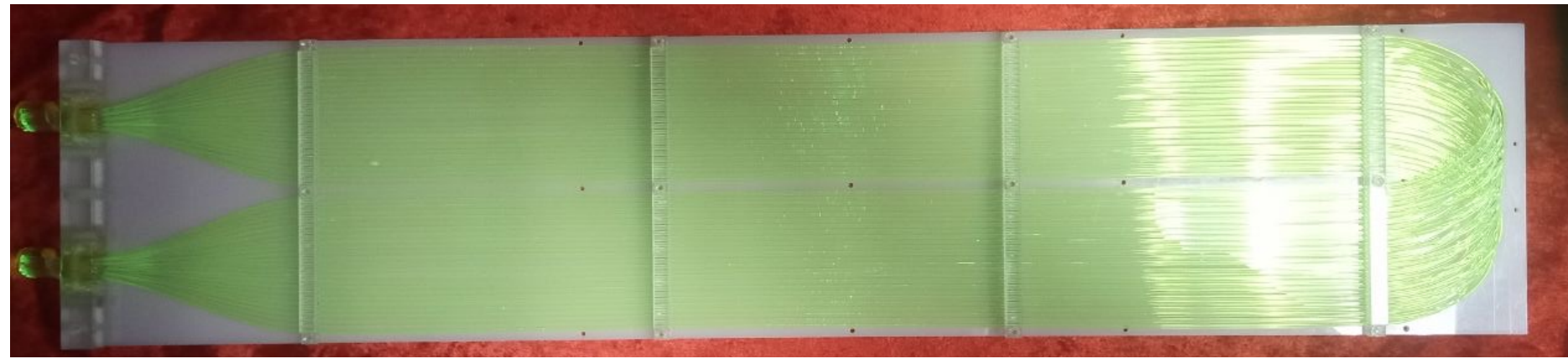
LCM for Full Scale Demonstrator (FSD)



2x2 Version ~ 20 m of WLS fiber

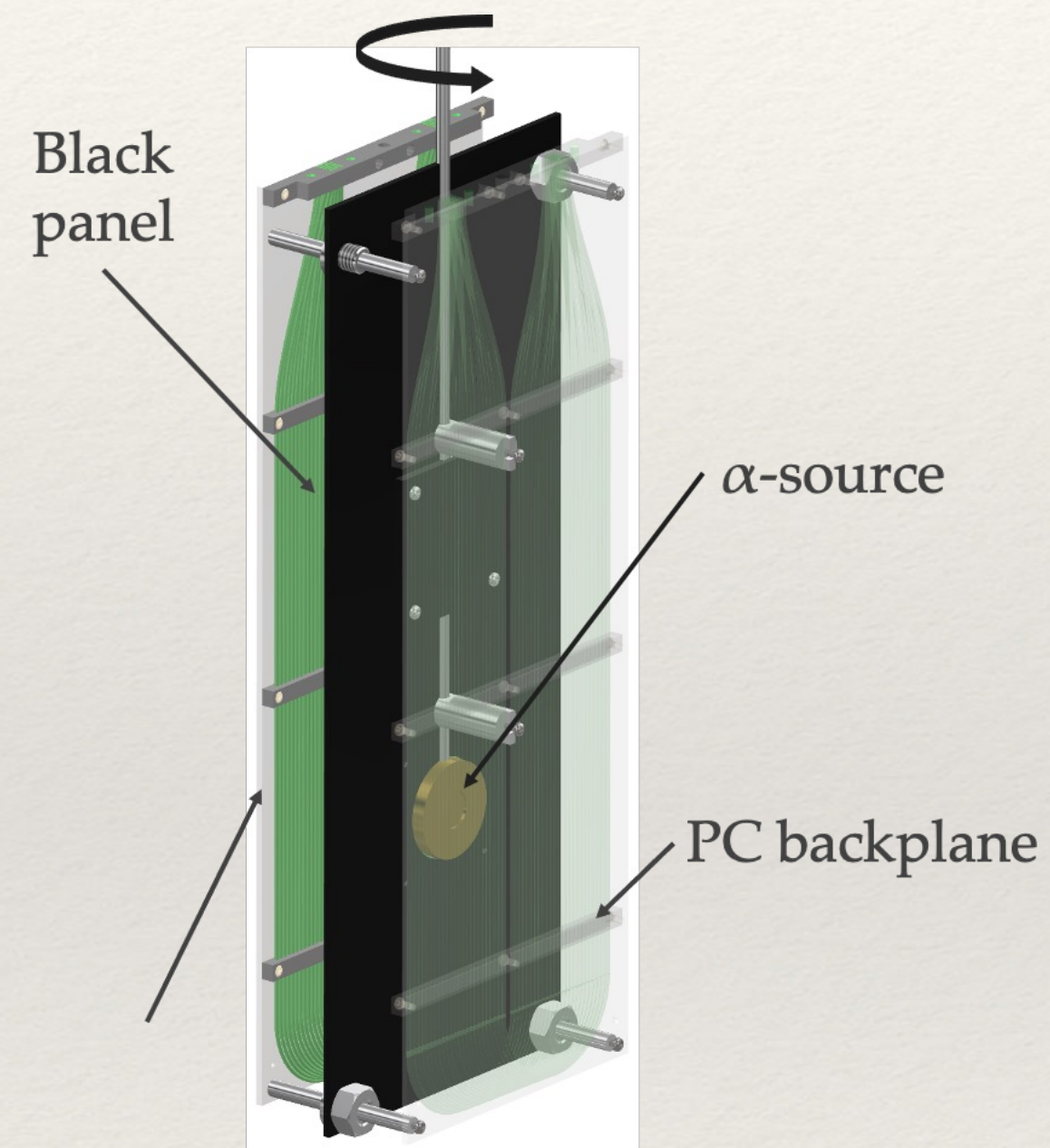
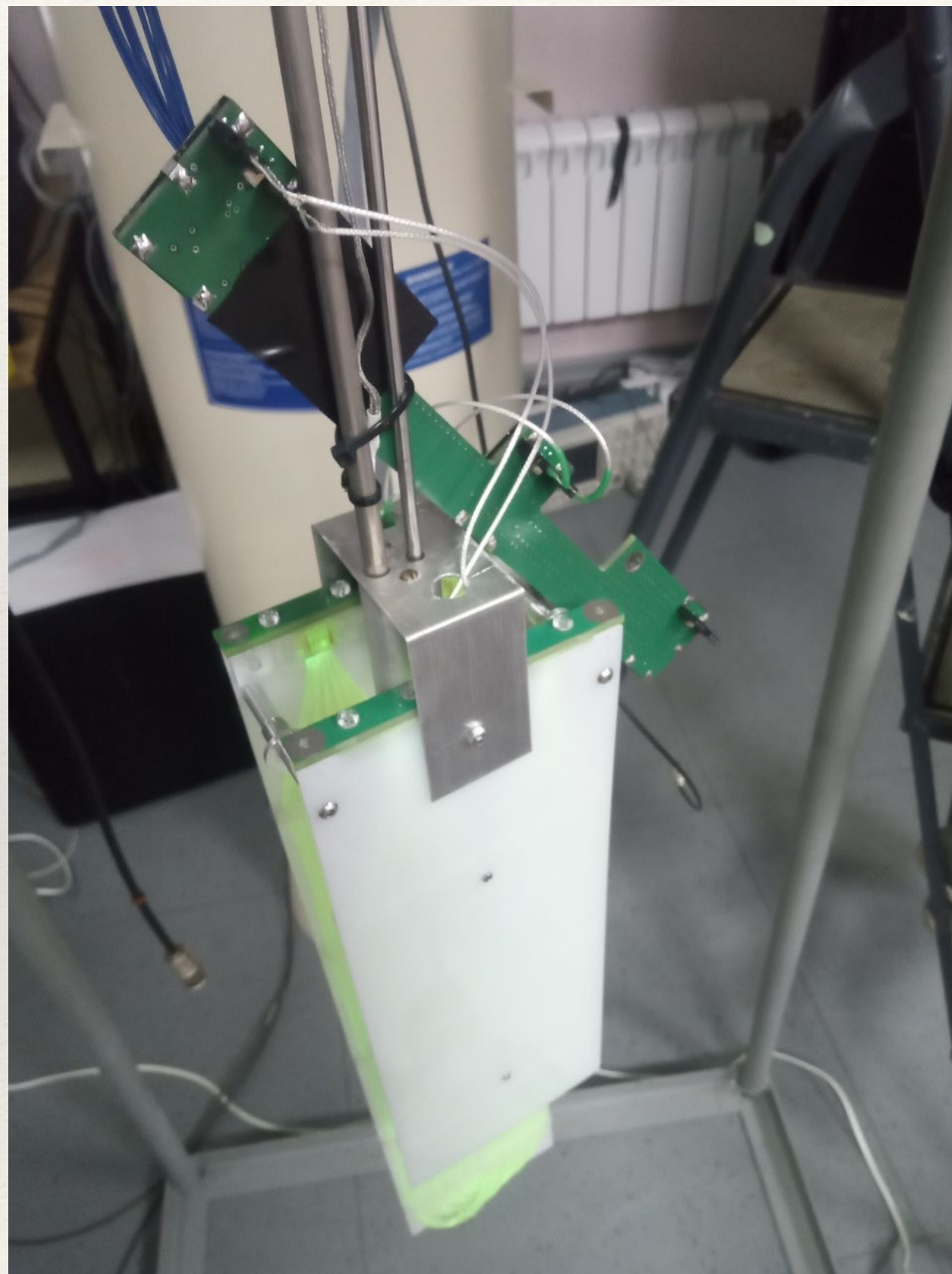


FSD Version ~ 30 m of WLS fiber



Cryogenic stand at JINR

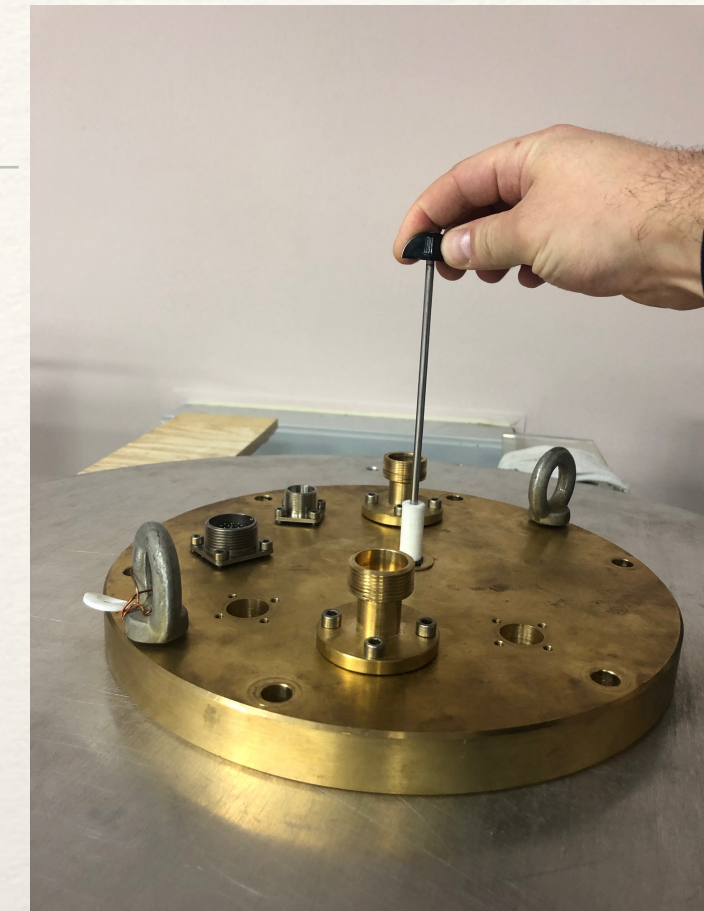
Studies with real LAr signal -> pre-test of the readout chain in LAr



3D model prototype



We use ^{241}Am α -source

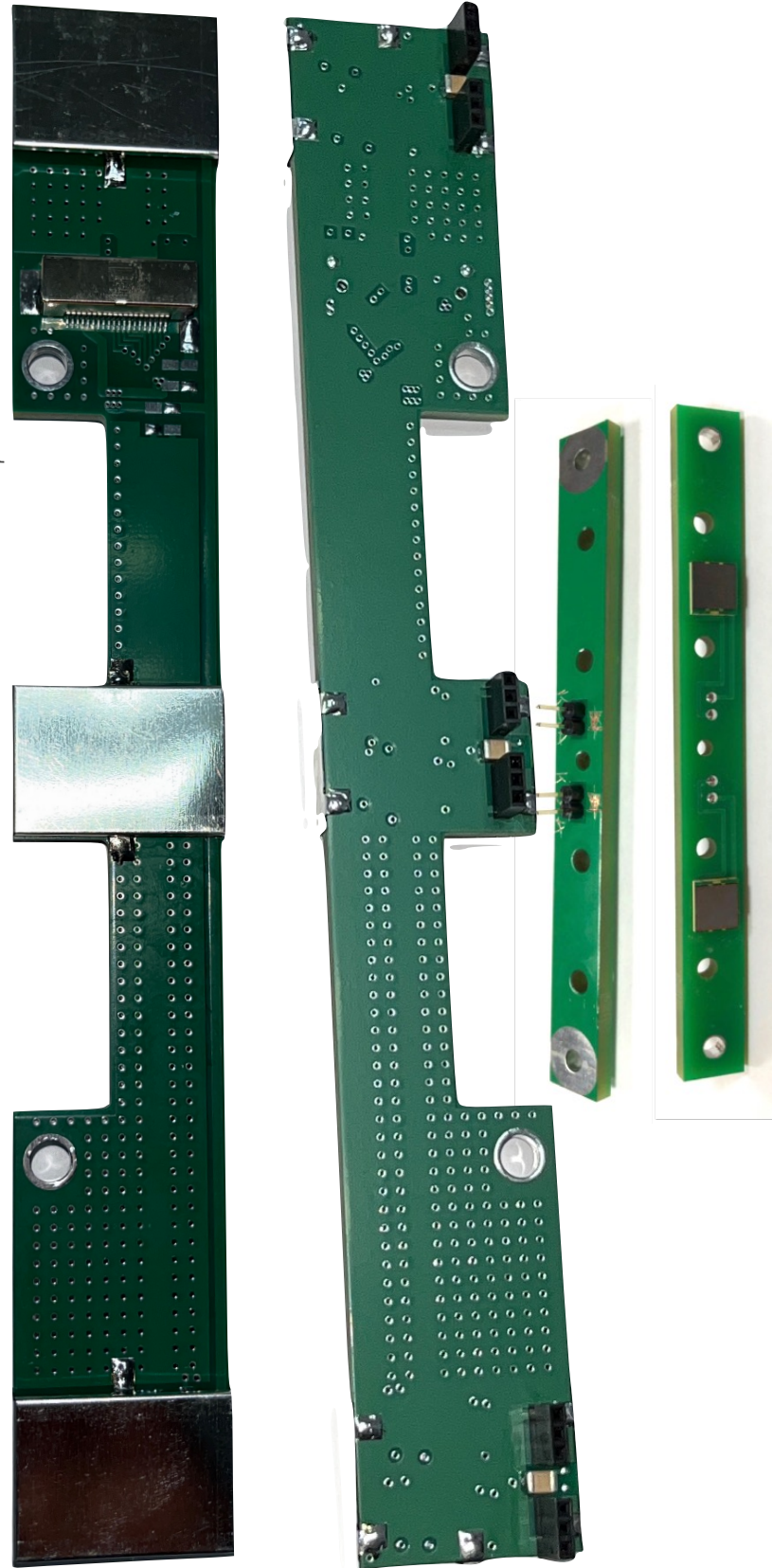


Purchase LAr from Kurchatov's Institute
Purity of LAr at level 10^{-5} - 10^{-6}

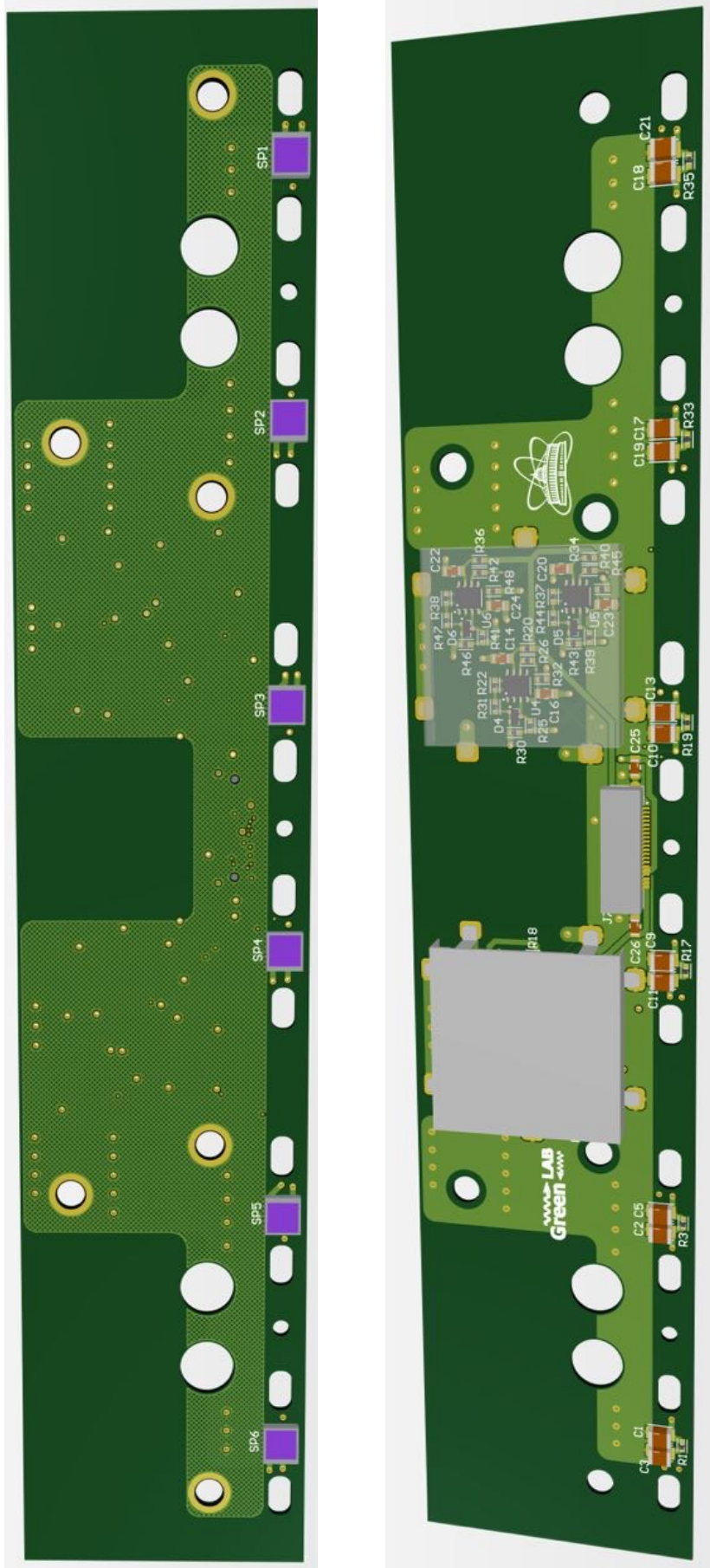
Cold PCB for FSD

2x2 Version

- E-PCB carrying 6 preamps
- Cold preamps (LMH6624) Gain ~ 5
- Power ~ 30-40~mW each @ BW of ~ 30MHZ (~10 ns rise time).
- Interface to 3 SiPM boards (3 LCMs or 1 ArCLight)
- Metal screens use to cancel clock pick up from Charge readout.
- Samtec connectors
- Left and right boards



FSD Version

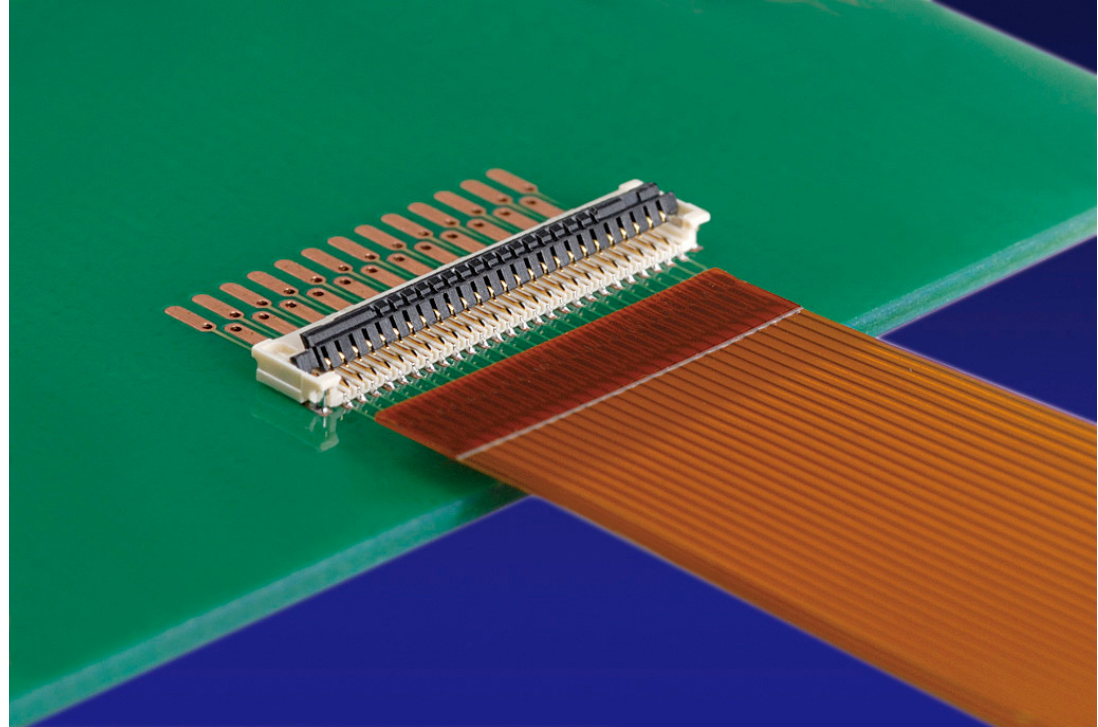


- FSD PCB carrying 6 preamps + 6 SiPM
- 6 SiPM are integrated onto the board
- Cold preamps (LMH6624) Gain ~ 5
- Power ~ 30-40~mW each @ BW of ~ 30MHZ (~10 ns rise time).
- Metal Screens
- **Interface to 3 LCMs or 1 ArCLight**
- SiPM number can be doubled (?)
- **Samtec or flex cable (?) connector**

Samtec microcoax cable



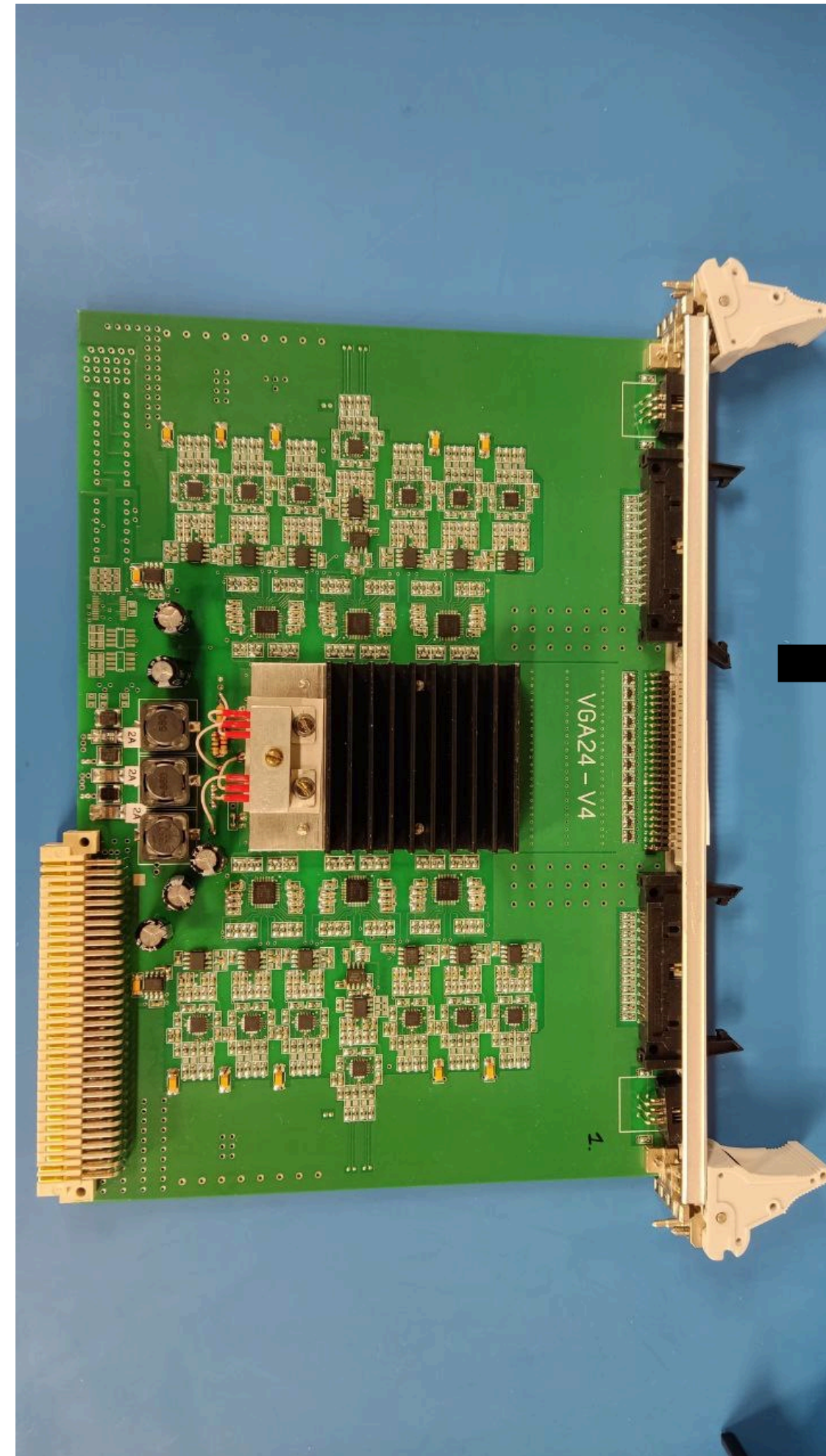
Flexible PCB



VGA for FSD

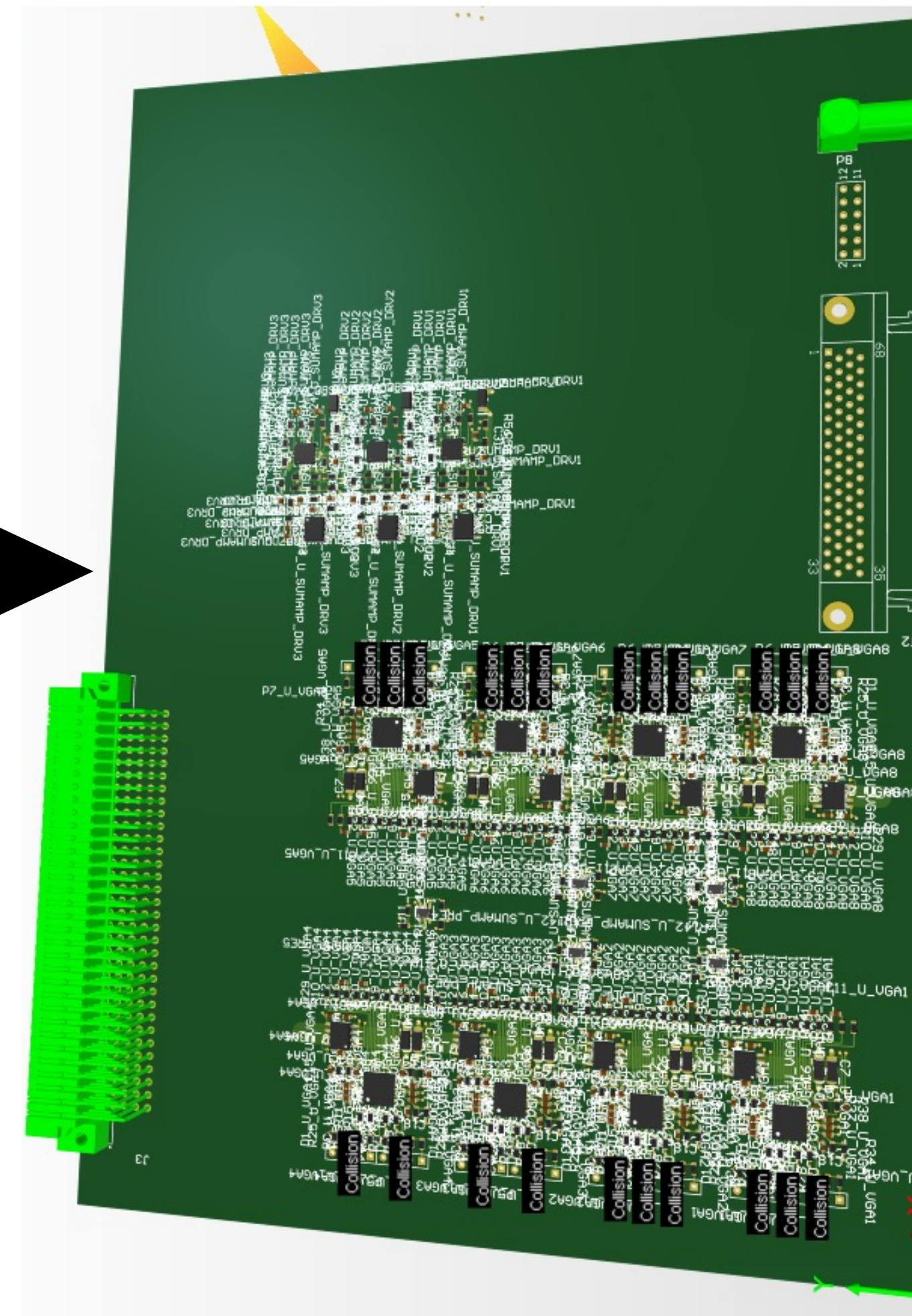
2x2 Version

- VME module
- 24 channels
- Needs adapter board for Power and Signal decoupling
- External E-PCB power
- External gain controller



FSD Version

- VME module
- 30 channels
- Onboard Power and Signal decoupling
- Onboard Cold-PCB power
- Onboard gain controller CAN-open

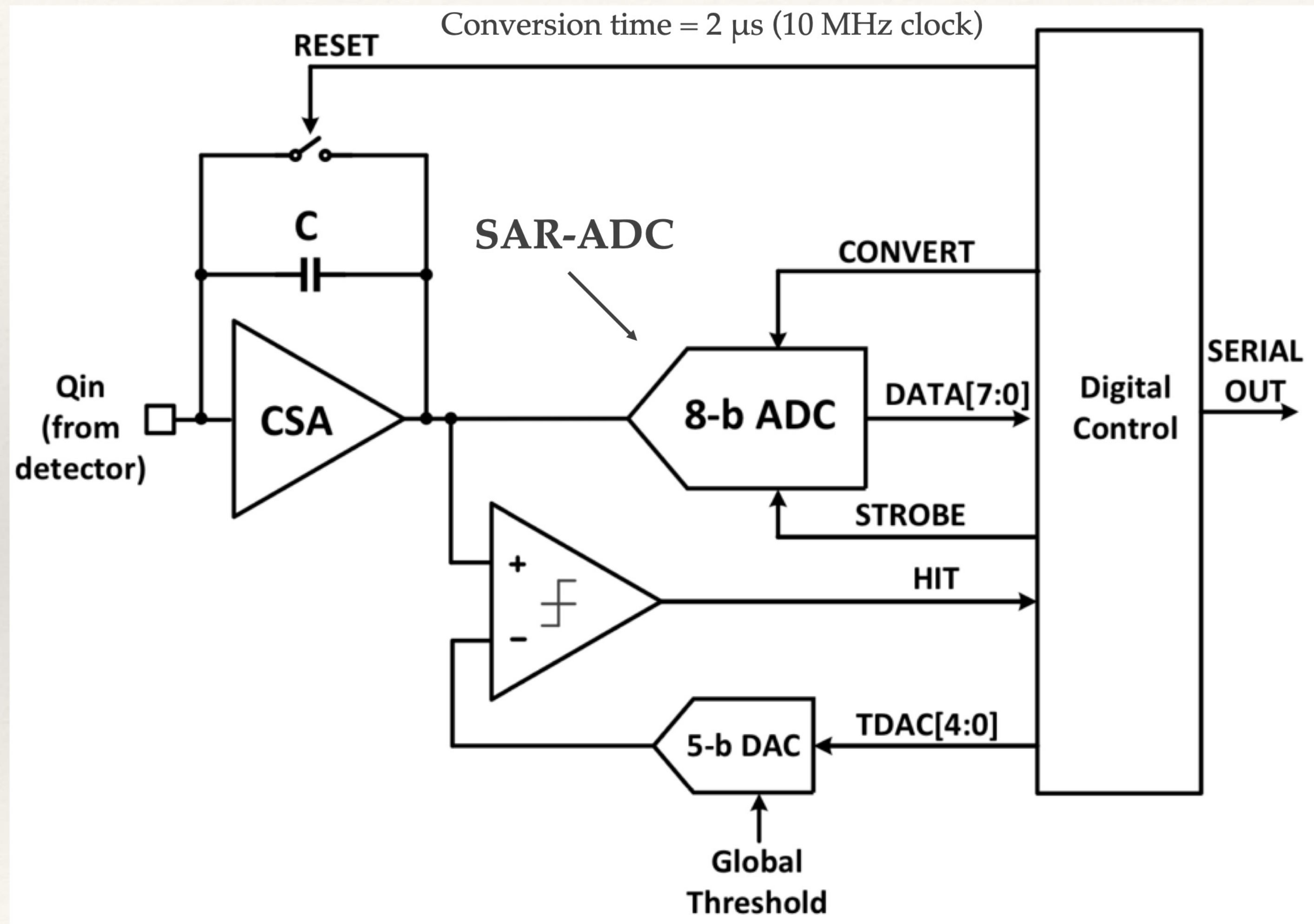


Планы на 2024-2026 гг.

- Производство компонент световой системы для прототипа 5-го модуля - модуль-Х. Будут отрабатываться новые решения в криогенных тестах в Берне. 2024-2026 гг.
- Тесты матрицы модулей 2x2 на нейтринном пучке в Фермилабе - 2023-2024 гг.
- Производство компонент световой системы для полноразмерного модуля ближнего детектора: электроника, детекторы, система калибровки, кабели. Испытания компонент. 2024 г.
- Тесты полноразмерного модуля в Берне. 2024-2025 гг.
- Подготовка документации по итогам испытаний полноразмерного модуля ближнего детектора для прохождения FDR (final design review). 2025-2026 гг.
- НИОКР новых типов волокон с добавкой TPВ и тесты. 2024-2025 гг.
- Подготовка к массовому производству компонент световой системы для Ближнего детектора DUNE. 2026 г.

Backup

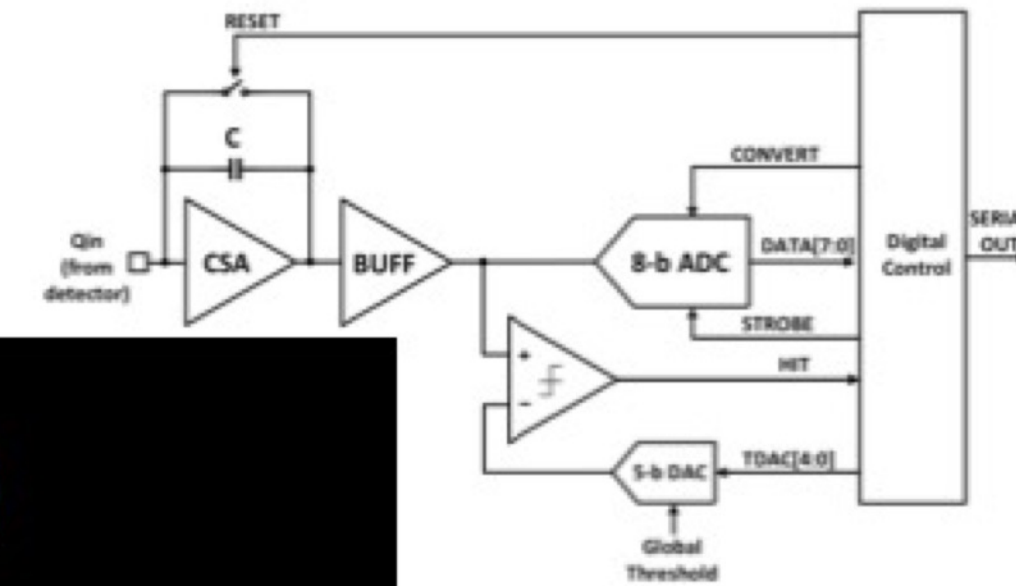
Charge readout ASIC



Analog and digital parts in the same chip!

Charge readout timing

LArPix Self-trigger Cycle



1. Drifting charge induces current on pixel.

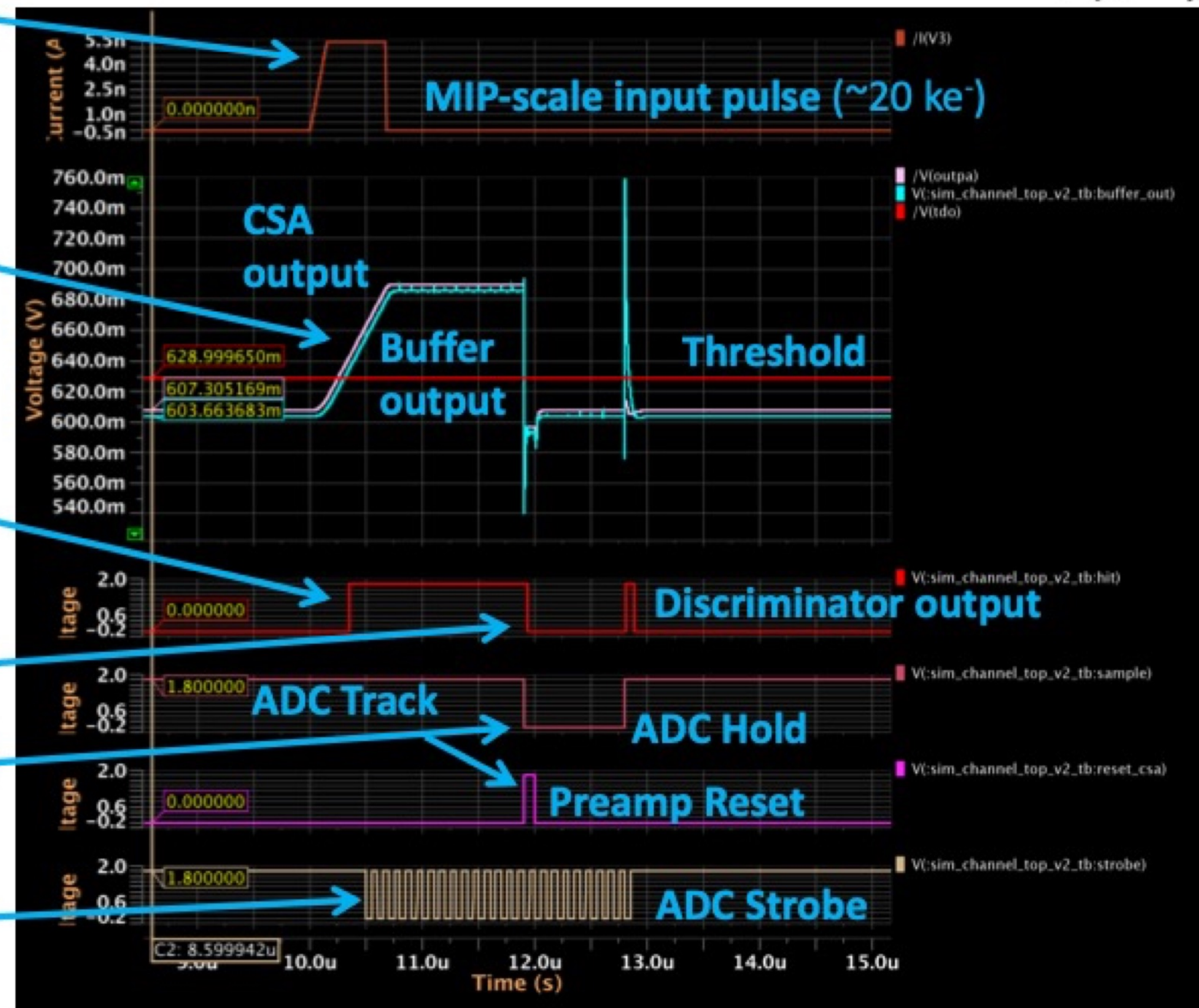
2. CSA integrates current, buffer drives current to discriminator and ADC.

3. Signal exceeds discriminator threshold, hit cycle begins.

4. Channel 'waits' a tunable delay (typically 1.8 us) for full drift signal integration.

5. If discriminator still high after wait, ADC 'holds' signal and front-end is reset to discard charge on pixel. Channel ready for next signal.

6. ADC 'strokes', converting held signal to digital value. Sends ADC value, timestamp, and chip/channel ID to serial out.



Optional Burst Modes:

'Fixed' Burst:
Process 'n' hit cycles for each self trigger

'Dynamic' Burst:
Continue to process hit cycles until change in ADC value is below set value.

Note:
CSA does not reset until end of burst.