Status of ECal PCB Production

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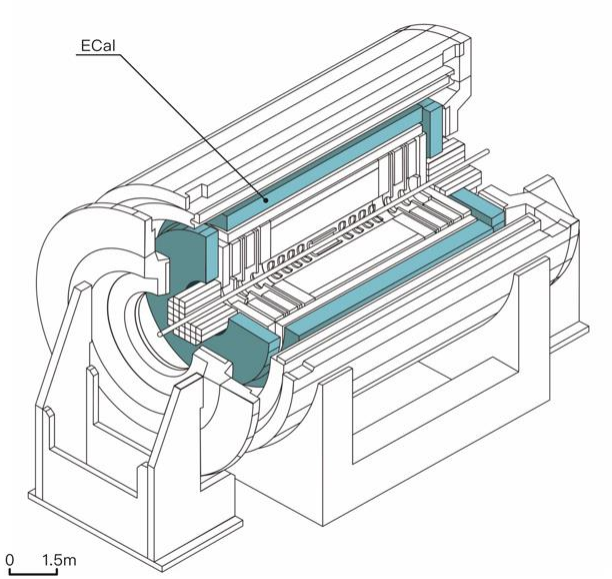
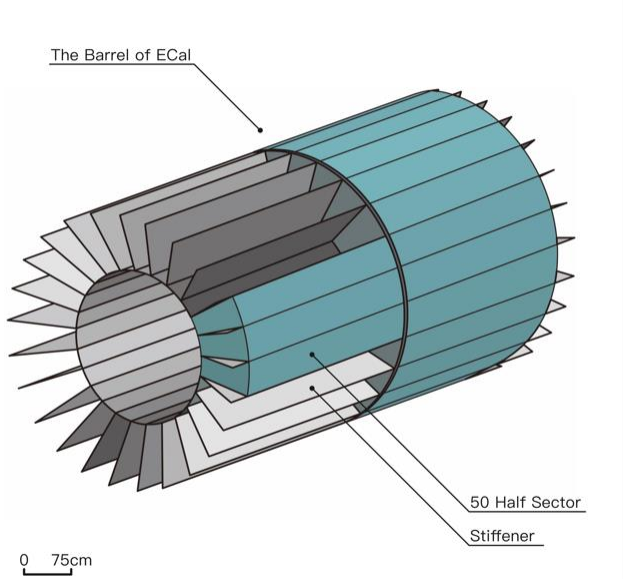
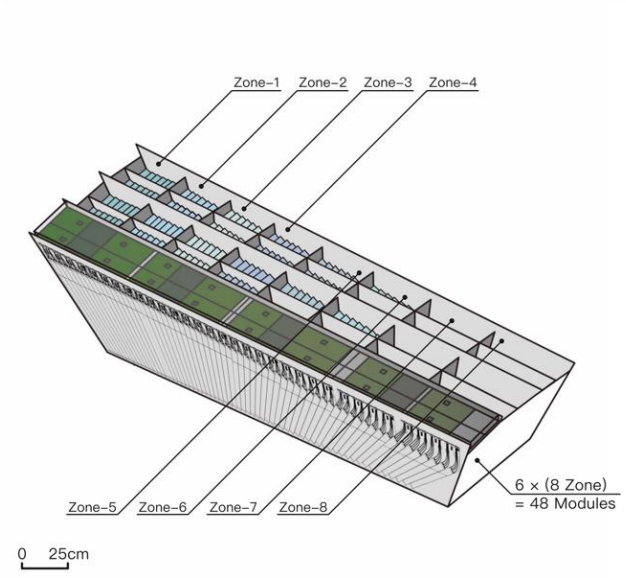
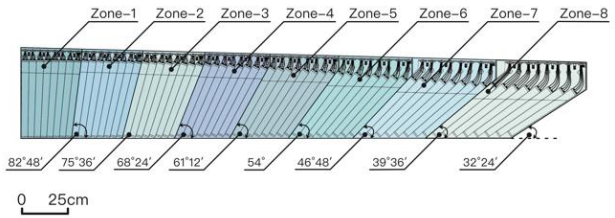
01 Background

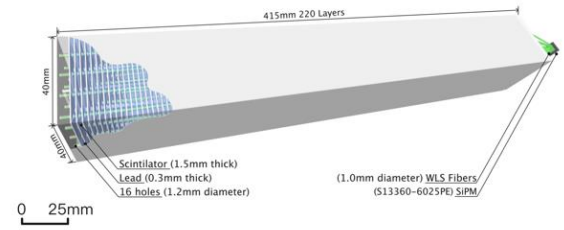
Background











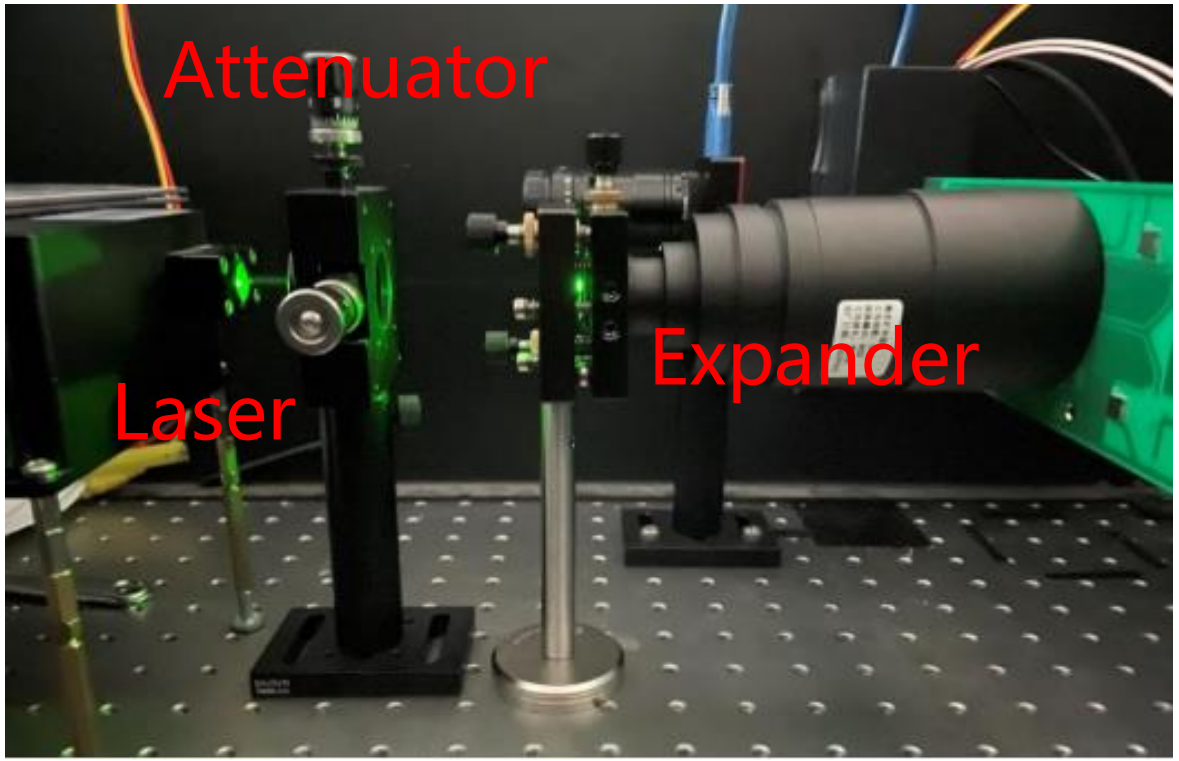
MPD ECal:

- 50 Half Sectors
- 2400 Modules
- 38400 Towers

Produced in China:

- 800 Modules (Completed)

Fast Preamplifier for module cosmic test in China



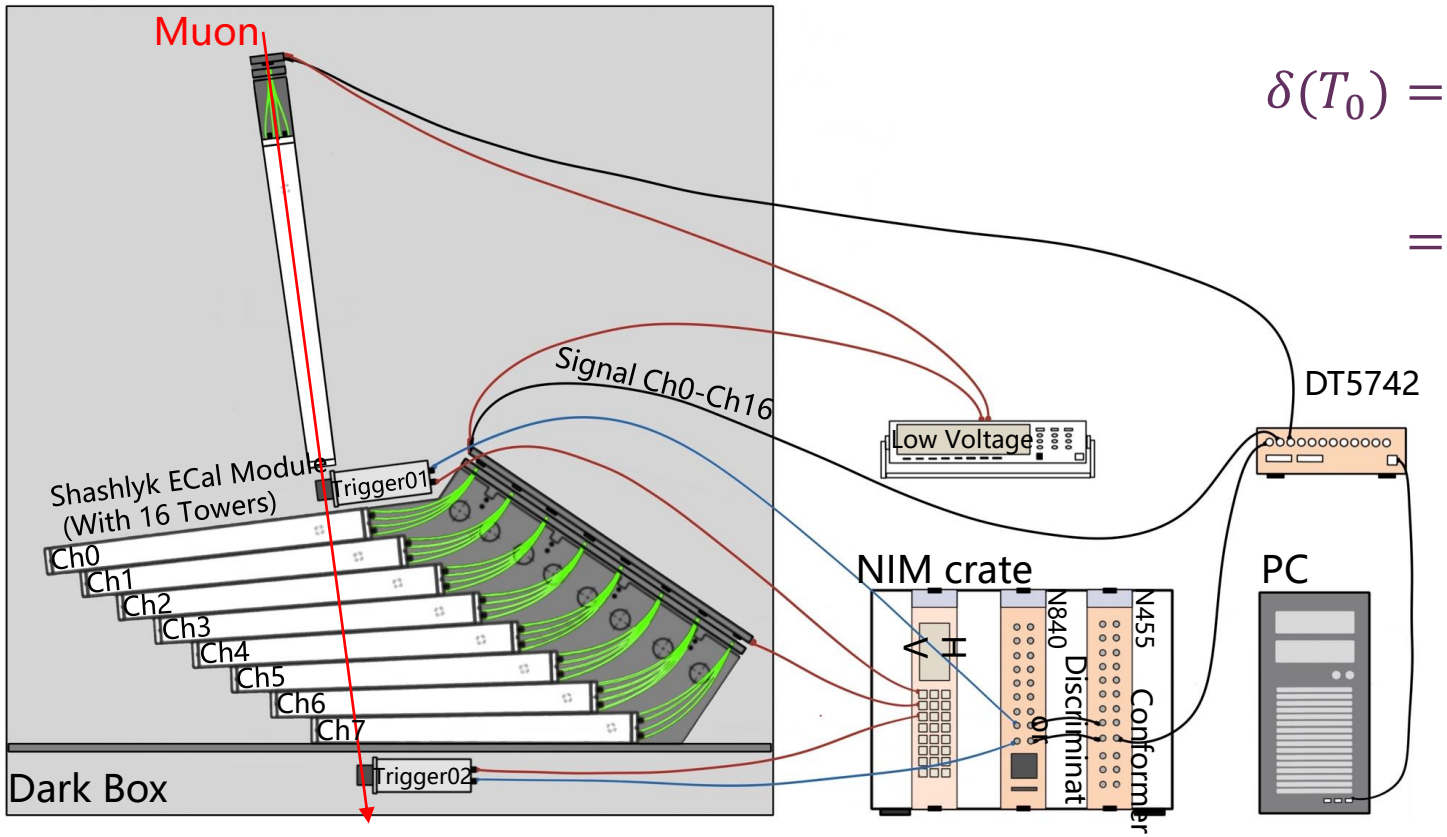
	Amp	Rise Time	Time Resolution
	MPV/mV	MPV/ns	single CH/ps
1	62.92	1.565	17.49
2	111.53	1.509	12.03
3	230.66	1.433	9.57
4	305.55	1.473	7.47
5	444.92	1.500	8.61
6	608.20	1.494	6.72
7	767.80	1.529	12.20

Bandwidth: 250MHz

Single CH Time resolution: <18ps (Tested with oscilloscope)

Fast Preamplifier for module cosmic test in China

T	Before Slewing	After Slewing
Ch7531-Ch6420	505.8	252.5
Tower-Ch76543210	1767	549.1



$$\delta(T_0) = \delta\left(\frac{\sum_{i=0}^{i=7} T_i}{8}\right) = \delta\left(\frac{\sum_{i=0}^{i=3} T_i - \sum_{i=4}^{i=7} T_i}{8}\right)$$
$$= \delta\frac{(T_1+T_3+T_5+T_7)-(T_0+T_2+T_4+T_6)}{8}$$

$$\delta(T_{tower}) = \delta(T_{tower} - \frac{\sum_{i=0}^{i=7} T_i}{8}) \ominus \delta(T_0)$$
$$= 487.7\ ps$$

Background

Plan for the next stage of production:

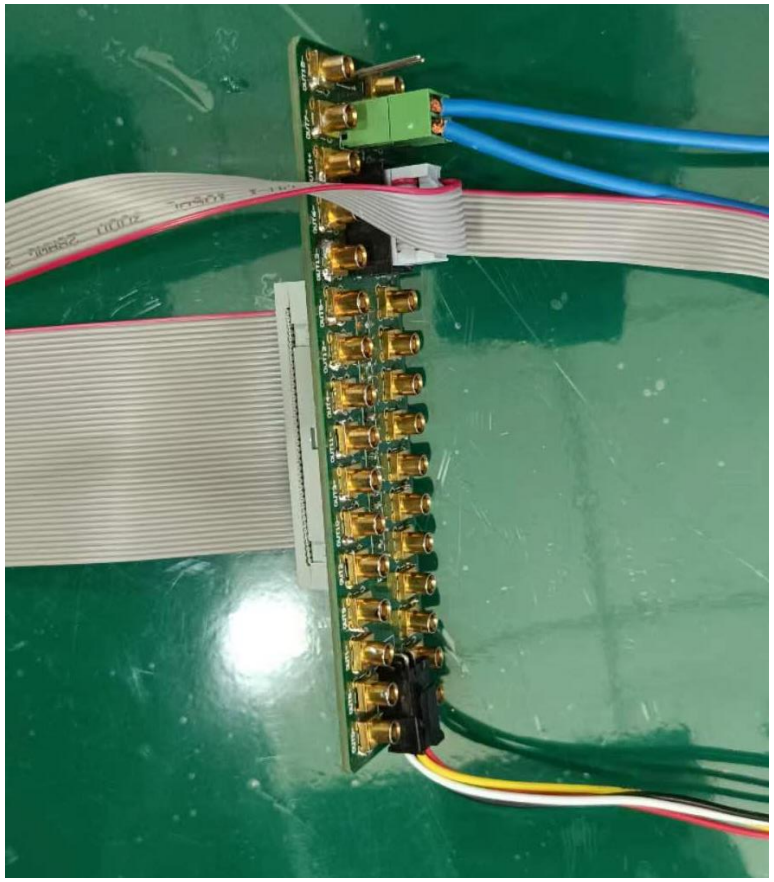
400 ECal Modules

1200 MPD ECal PCBs (150 for each zone) without SiPMs

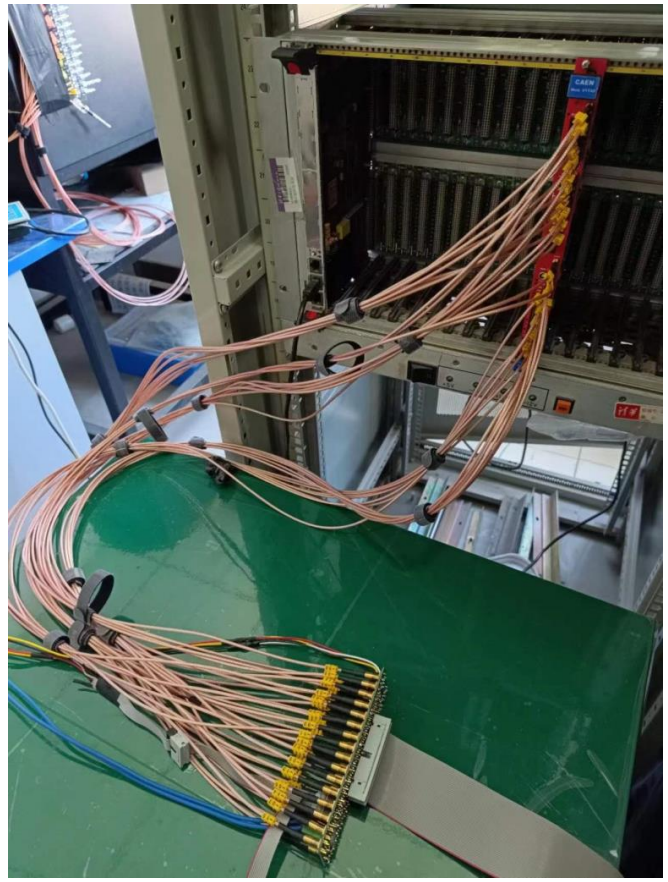
02 Verification of PCBs made in China

Setups

ECal module in darkroom

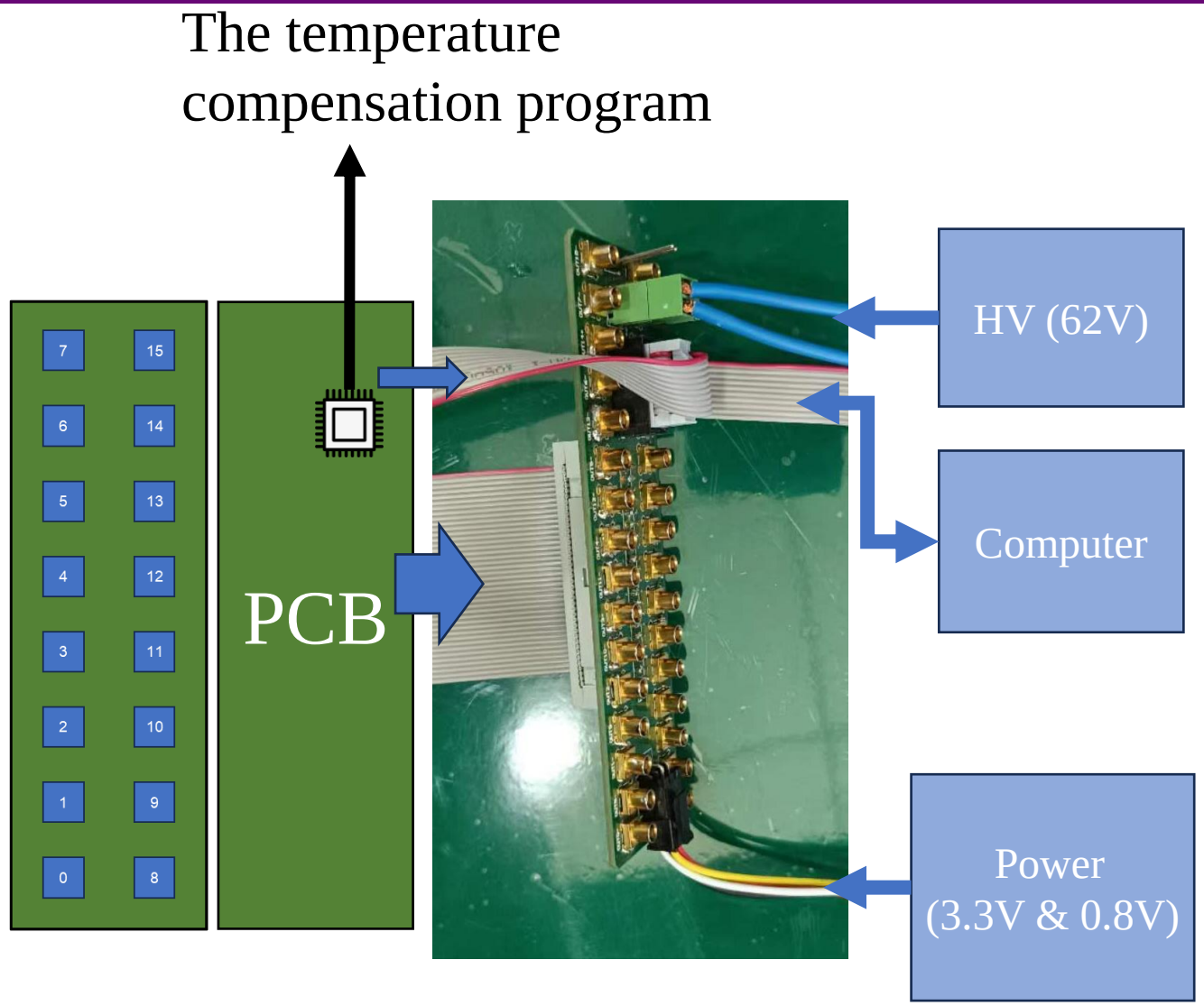


Adapter



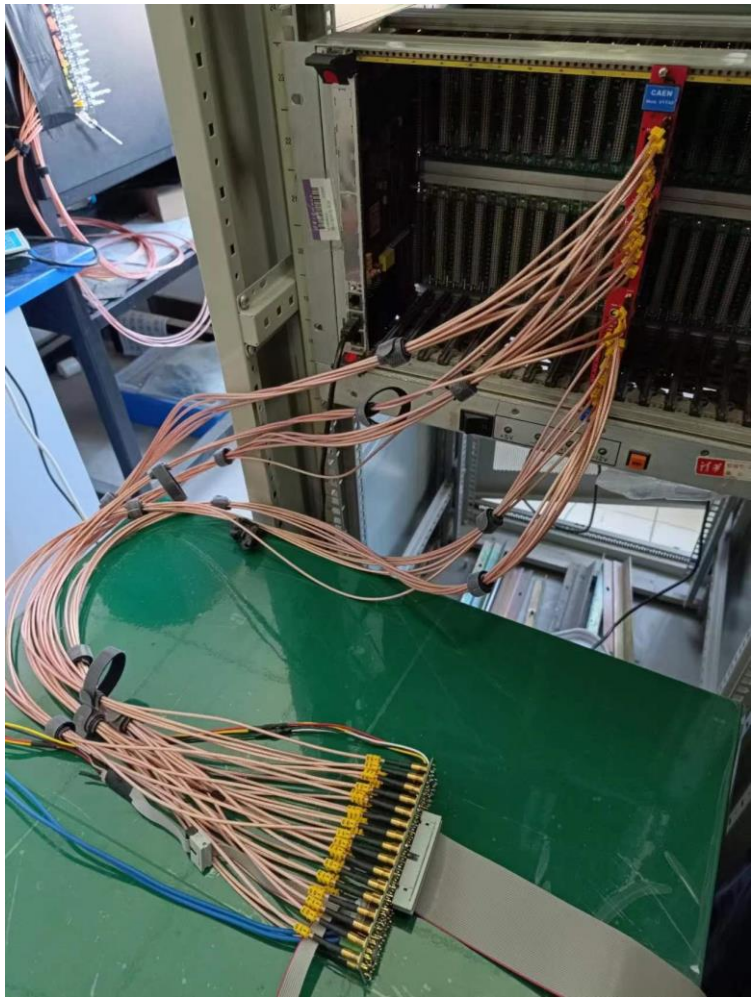
Read out by V1742 waveform digitizer

Adapter from flat cable to coaxial cable



- The temperature compensation program is written into the chip on the PCB.
- The base bias voltages at 25 ℃ are written in the code (59V for all SiPMs in this experiment).
- The computer can communicate with the chip to get some information and change the base bias voltages.
- The HV source only needs to provide a voltage high enough.

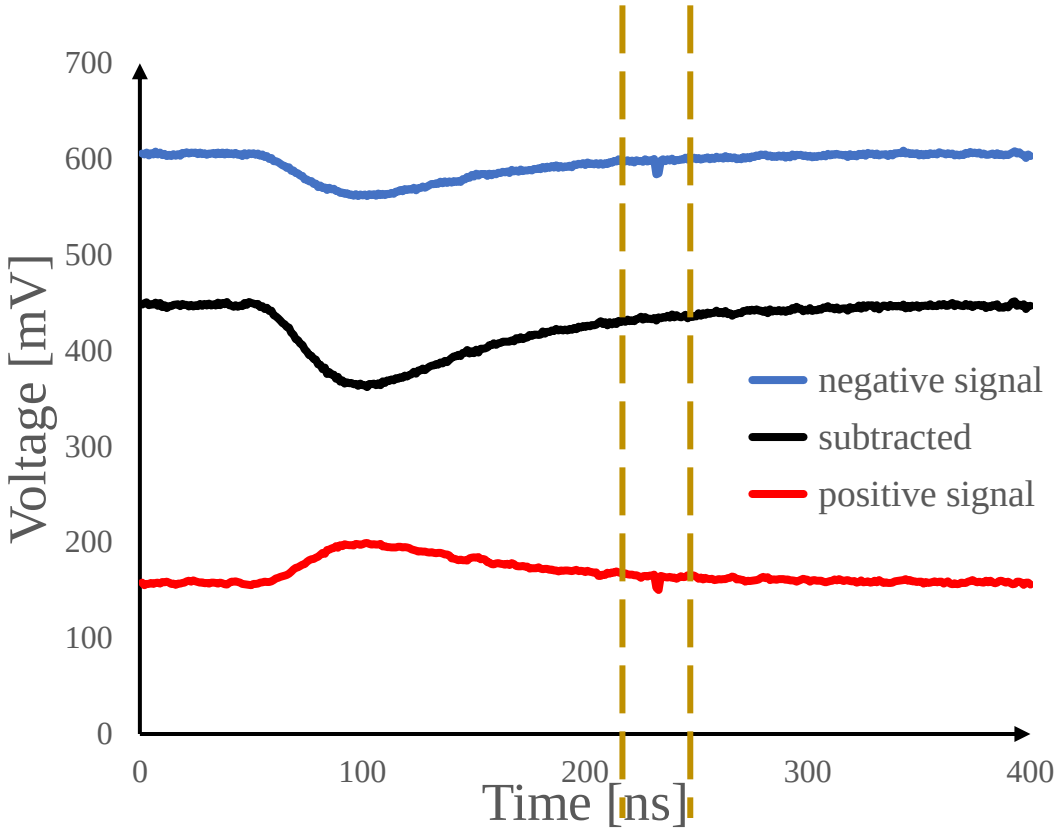
Adapter from flat cable to coaxial cable



- The differential output signal of each SiPM is transformed into 2 single-ended signals (one positive signal and one negative signal), then read out by V1742 waveform digitizer.

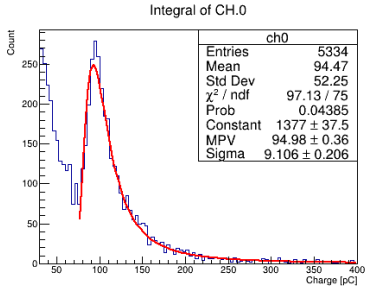
- The V1742 works in Self-Trigger Mode. The positive signals participate in the trigger generation

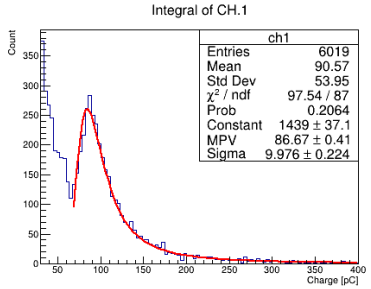
Data processing

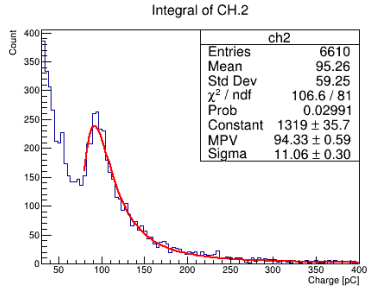


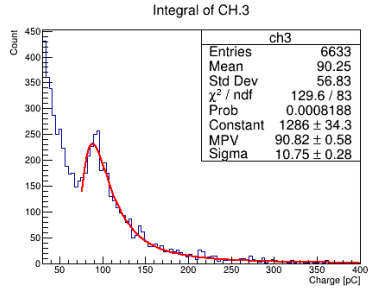
- The 2 single-ended signals of each SiPM are subtracted to eliminate the common-mode noise.
- Calculate the integral charge of each signal and fill the histograms

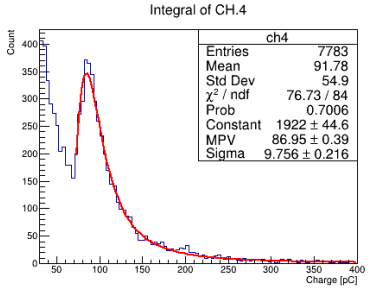
PCB from JINR

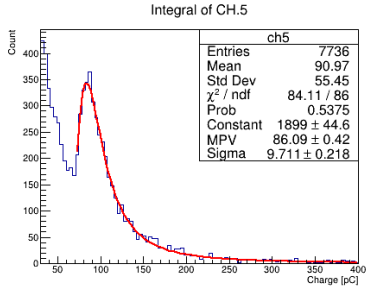


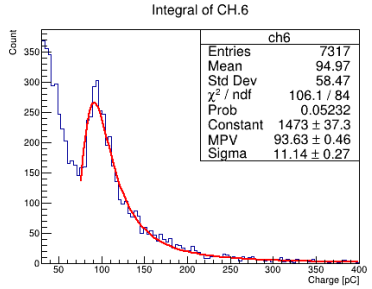


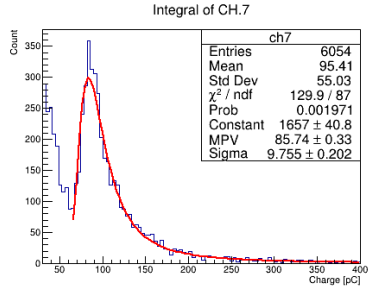


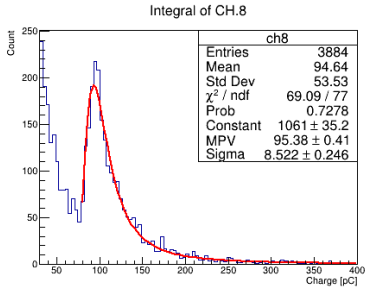


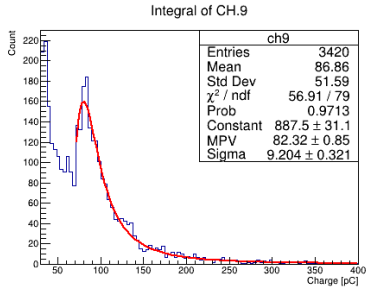


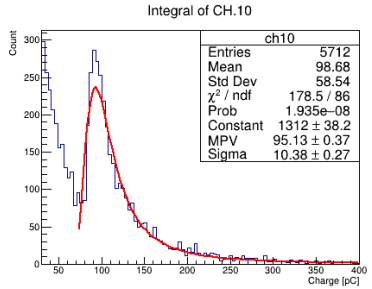


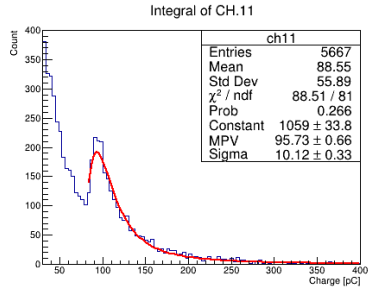


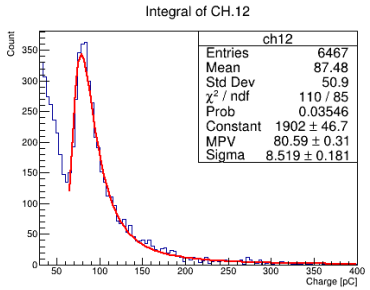


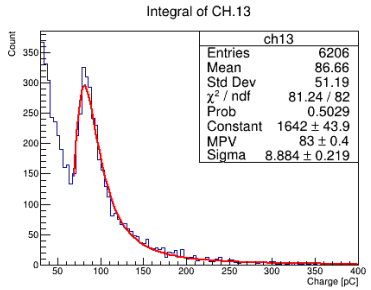


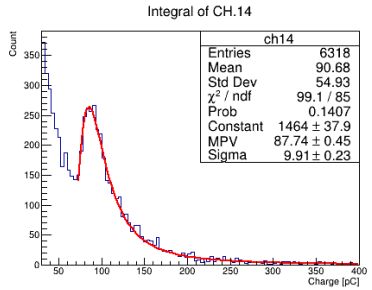


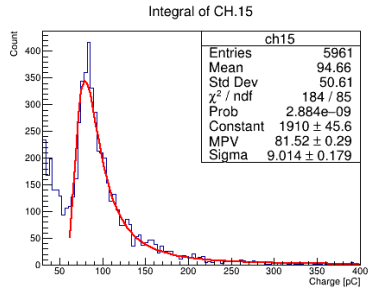






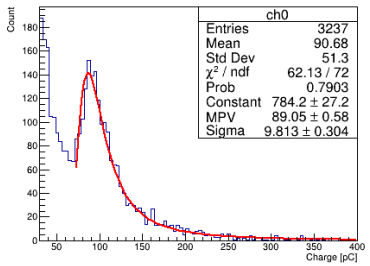




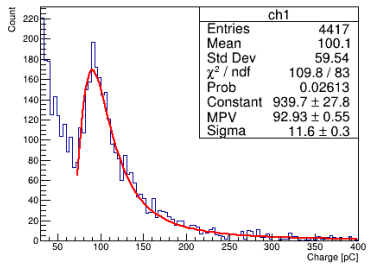


PCB from Tsinghua

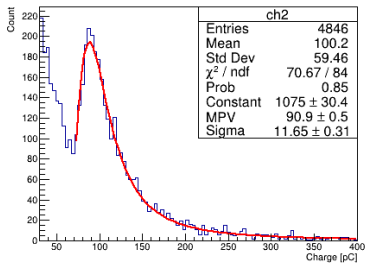
Integral of CH.0



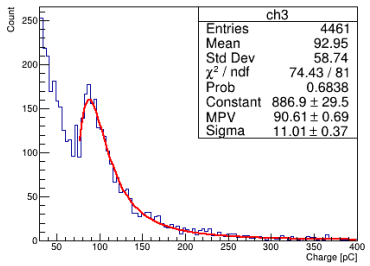
Integral of CH.1



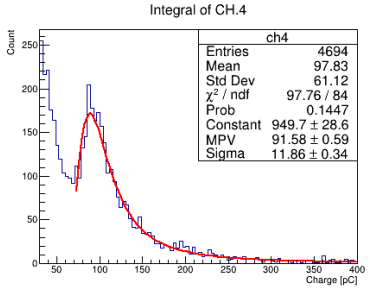
Integral of CH.2



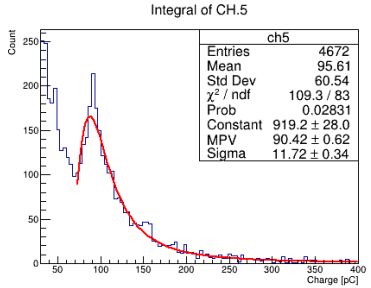
Integral of CH.3



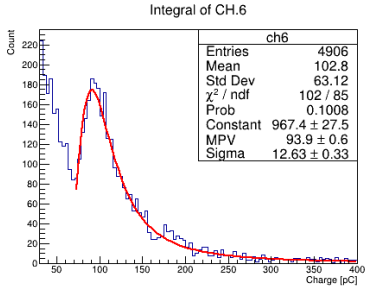
Integral of CH.4



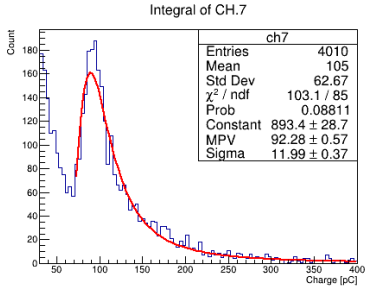
Integral of CH.5



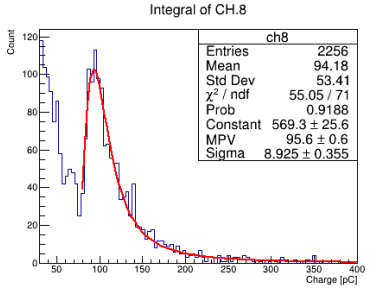
Integral of CH.6



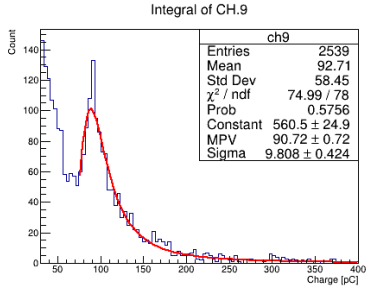
Integral of CH.7



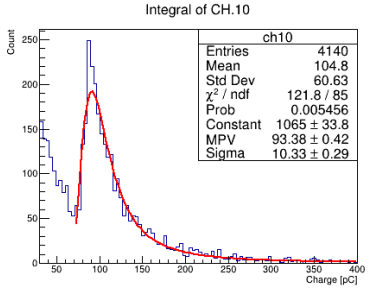
Integral of CH.8



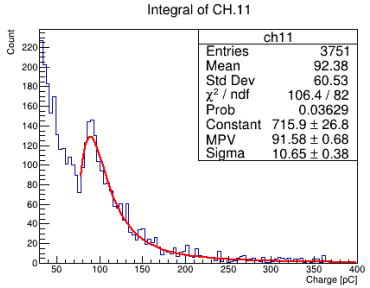
Integral of CH.9



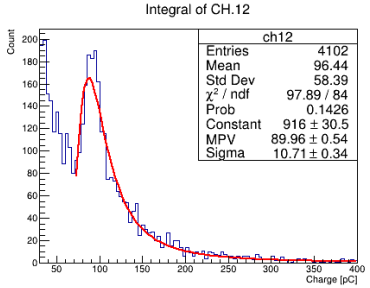
Integral of CH.10



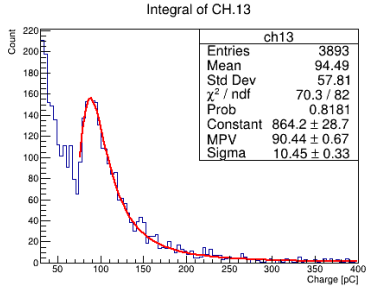
Integral of CH.11



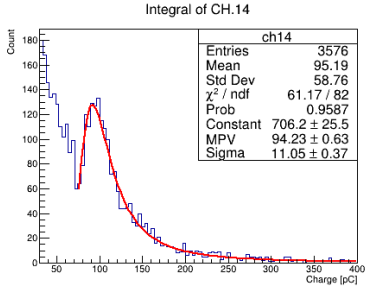
Integral of CH.12



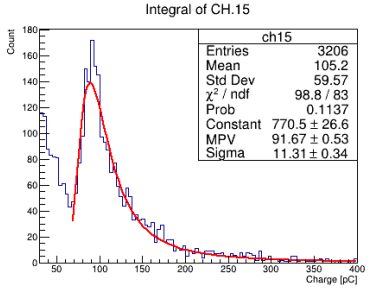
Integral of CH.13



Integral of CH.14



Integral of CH.15



Result

channel	Integral Charge [pC]	
	PCB from JINR	PCB from Tsinghua
ch0	94.99	89.05
ch1	86.67	92.93
ch2	94.33	90.90
ch3	90.82	90.61
ch4	86.95	91.58
ch5	86.09	90.42
ch6	93.63	93.90
ch7	85.74	92.28
ch8	95.38	95.60
ch9	82.32	90.72
ch10	95.14	93.38
ch11	95.73	91.58
ch12	80.59	89.96
ch13	83.00	90.44
ch14	87.74	94.23
ch15	81.52	91.67

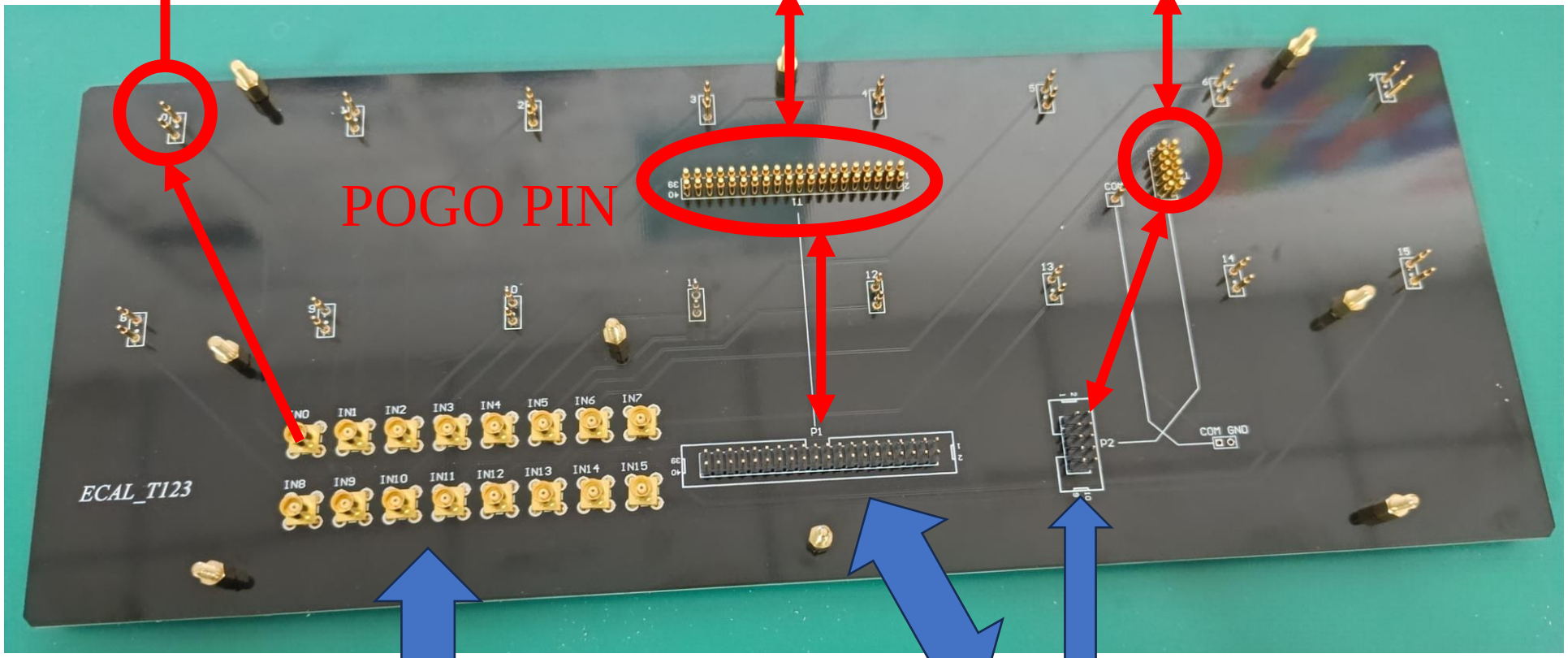
03 The method of testing PCBs without SiPMs

The design of backplane

The pads for SiPM

40P Header

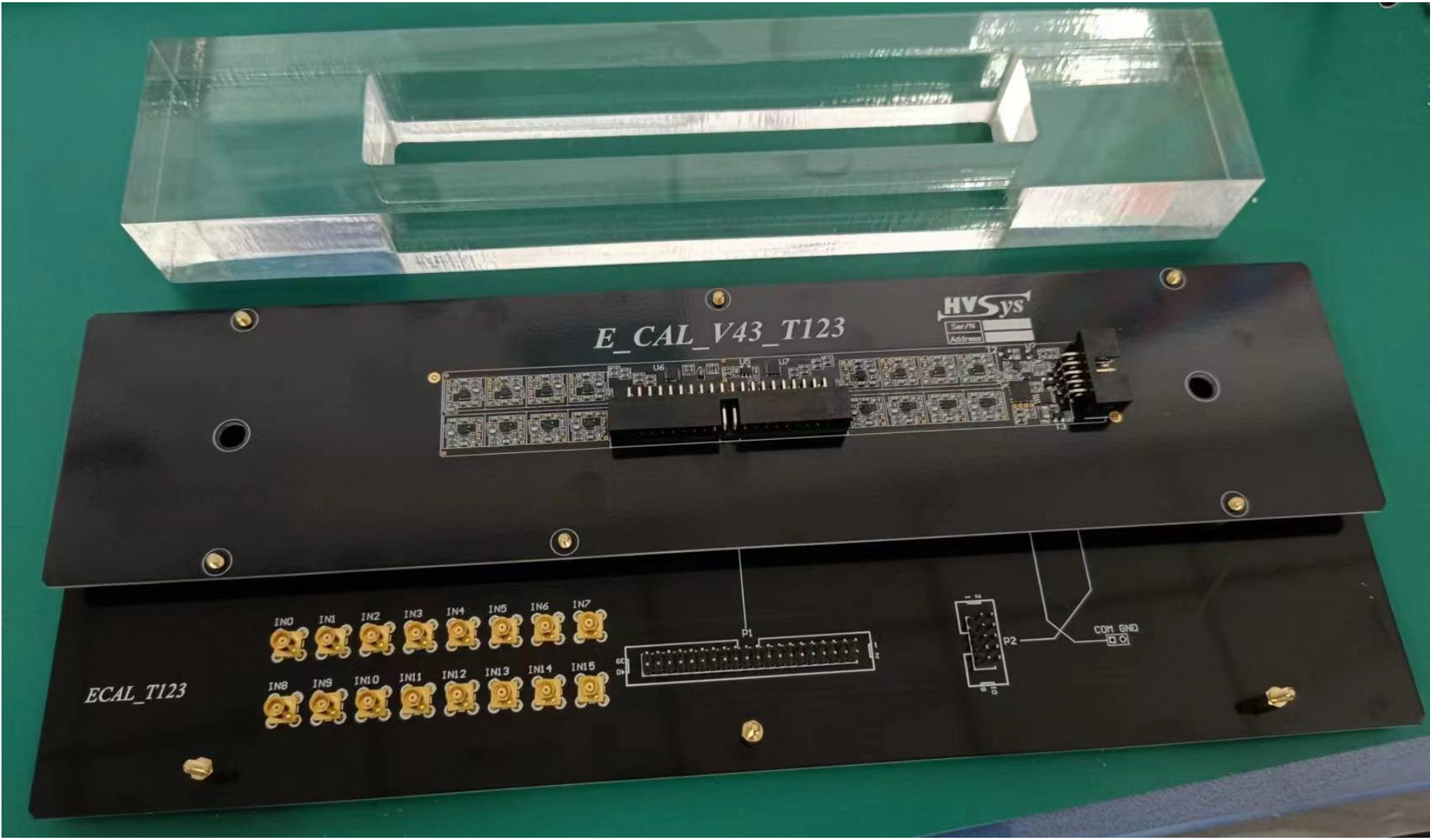
10P Header



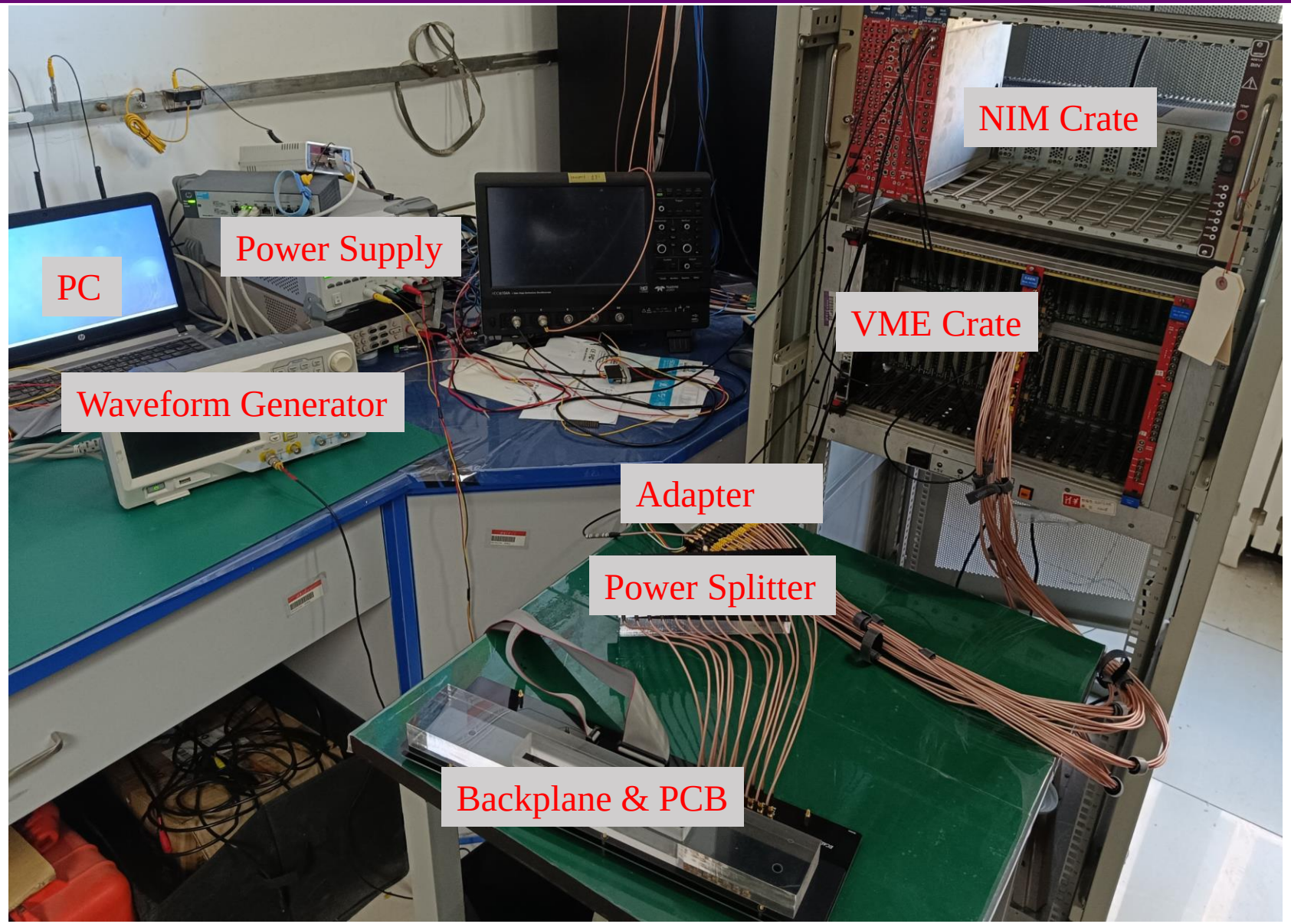
Input Signal

Adaptor

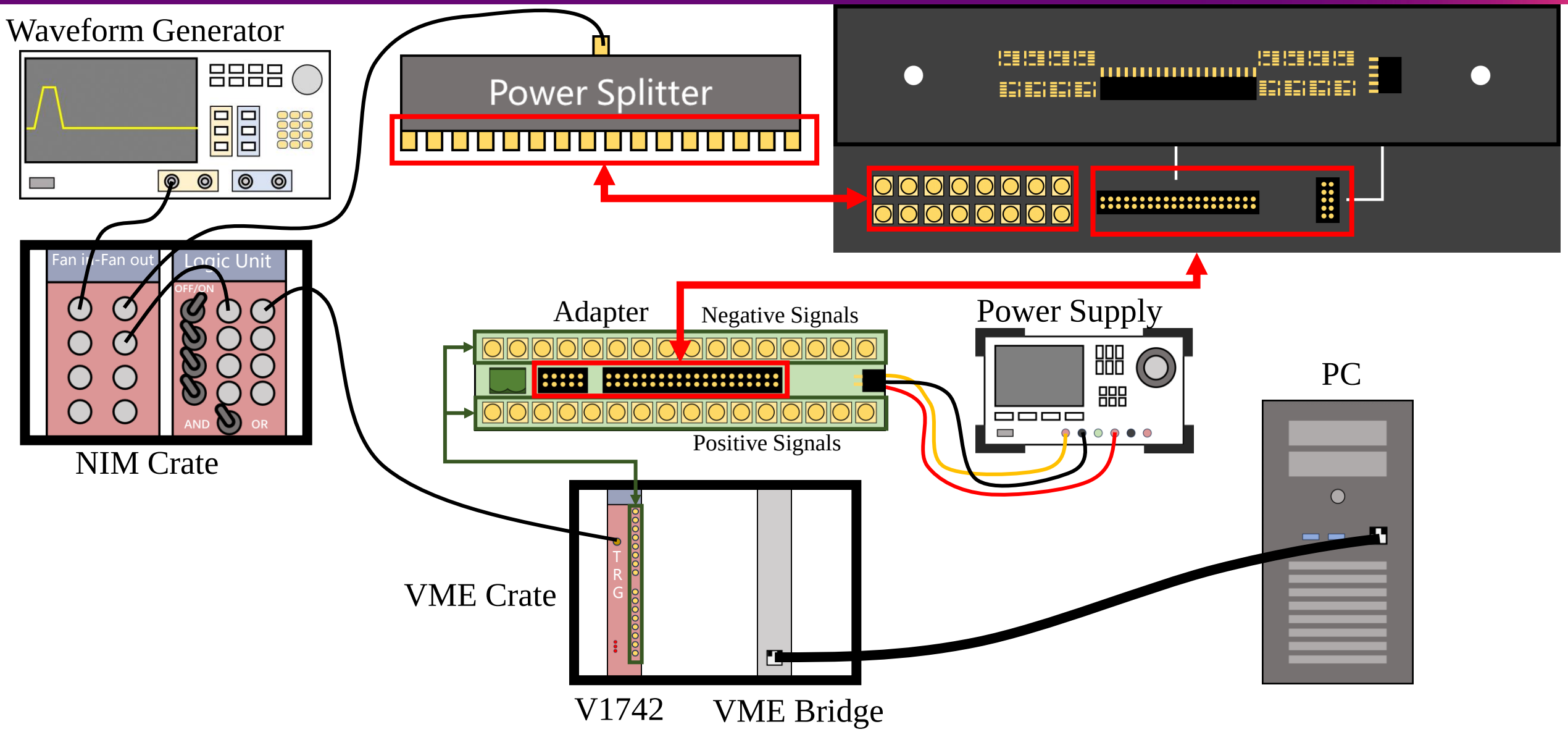
The design of backplane



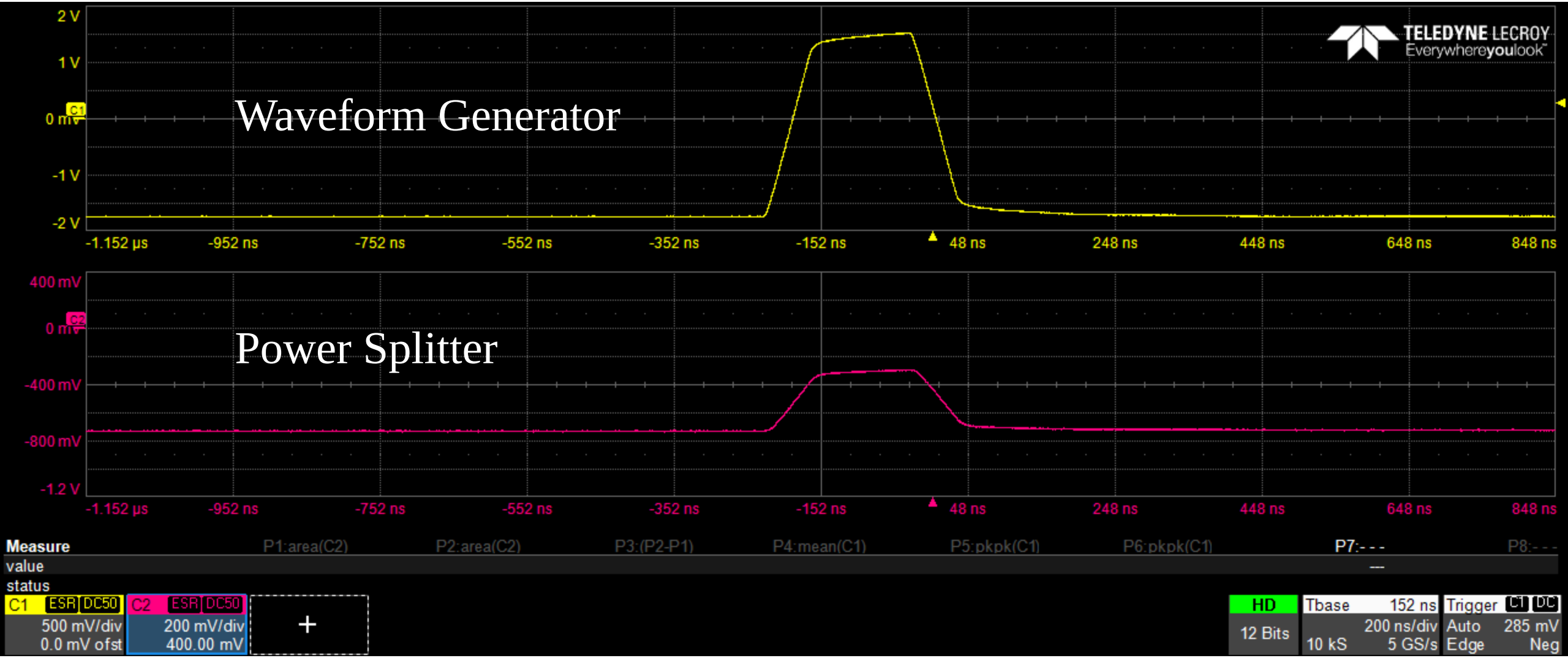
Setups


NIM Crate
Power Supply
PC
VME Crate
Waveform Generator
Adapter
Power Splitter
Backplane & PCB

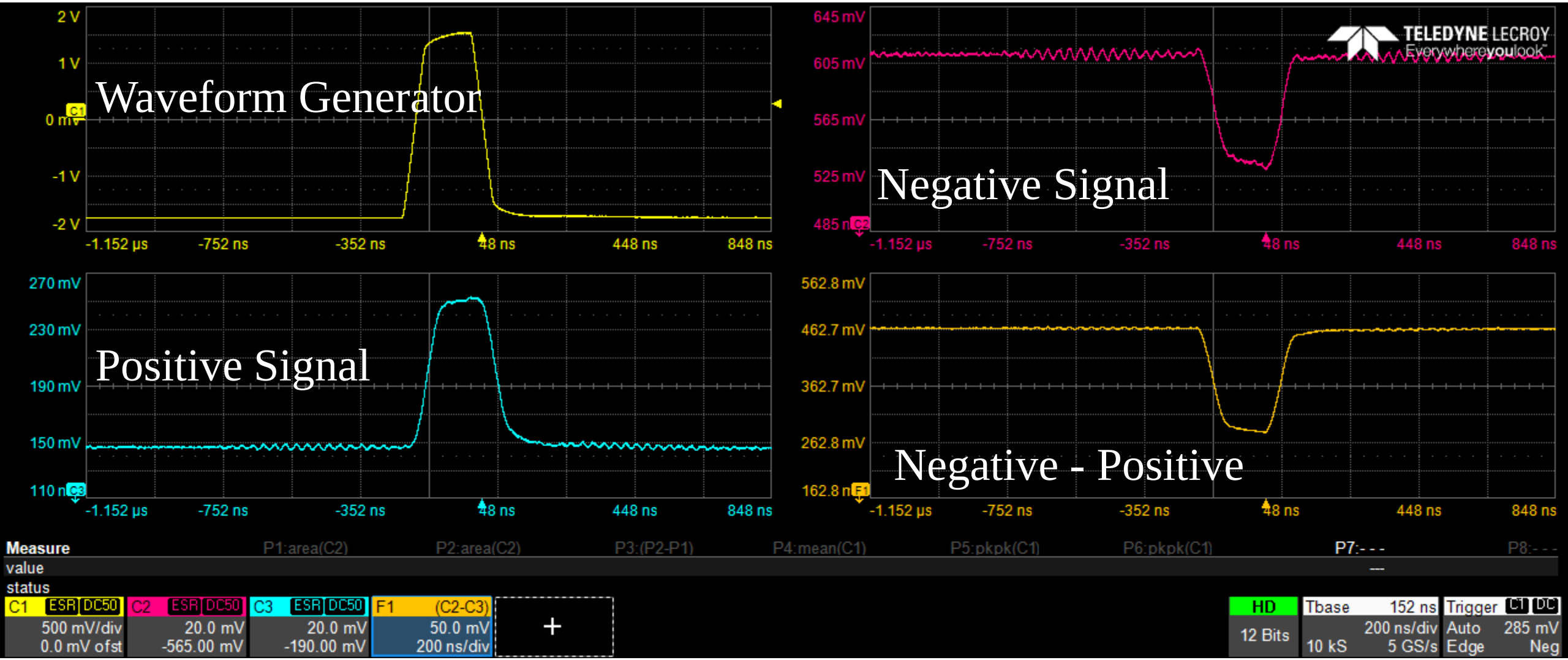
Setups


Waveform Generator
Power Splitter
Fan in-Fan out
Logic Unit
OFF/ON
AND
OR
NIM Crate
Adapter
Negative Signals
Positive Signals
Power Supply
PC
VME Crate
T
R
G
V1742
VME Bridge

Waveforms


TELEDYNE LECROY
Everywhereyoulook
Waveform Generator
2 V
1 V
0 mV
C1
-1 V
-2 V
-1.152 µs
-952 ns
-752 ns
-552 ns
-352 ns
-152 ns
48 ns
248 ns
448 ns
648 ns
848 ns
Power Splitter
400 mV
0 mV
C2
-400 mV
-800 mV
-1.2 V
Measure
P1:area(C2)
P2:area(C2)
P3:(P2-P1)
P4:mean(C1)
P5:pkpk(C1)
P6:pkpk(C1)
P7:- - -
P8:- - -
value
---
status
C1 ESR DC50
500 mV/div
0.0 mV ofst
C2 ESR DC50
200 mV/div
400.00 mV
HD
12 Bits
Tbase 152 ns
200 ns/div
10 kS 5 GS/s
Trigger C1 DC
Auto 285 mV
Edge Neg

Waveforms


Waveform Generator
Negative Signal
Positive Signal
Negative - Positive
TELEDYNE LECROY
Everywhereyoulook™
2 V
1 V
0 mV
-1 V
-2 V
645 mV
605 mV
565 mV
525 mV
485 mV
270 mV
230 mV
190 mV
150 mV
110 mV
562.8 mV
462.7 mV
362.7 mV
262.8 mV
162.8 mV
-1.152 µs
-752 ns
-352 ns
48 ns
448 ns
848 ns
Measure
P1:area(C2)
P2:area(C2)
P3:(P2-P1)
P4:mean(C1)
P5:pkpk(C1)
P6:pkpk(C1)
P7:- - -
P8:- - -
value
status
C1 ESR DC50
500 mV/div
0.0 mV ofst
C2 ESR DC50
20.0 mV
-565.00 mV
C3 ESR DC50
20.0 mV
-190.00 mV
F1 (C2-C3)
50.0 mV
200 ns/div
HD
12 Bits
Tbase 152 ns
200 ns/div
10 kS 5 GS/s
Trigger C1 DC
Auto 285 mV
Edge Neg

04 Schedules

Schedules

1200 MPD ECal PCBs:

The production and test of PCBs will be finished before Feb. 2024.

400 ECal Modules:

We are trying to get budget to finish the production.

Thank you!

清華大學
Tsinghua University