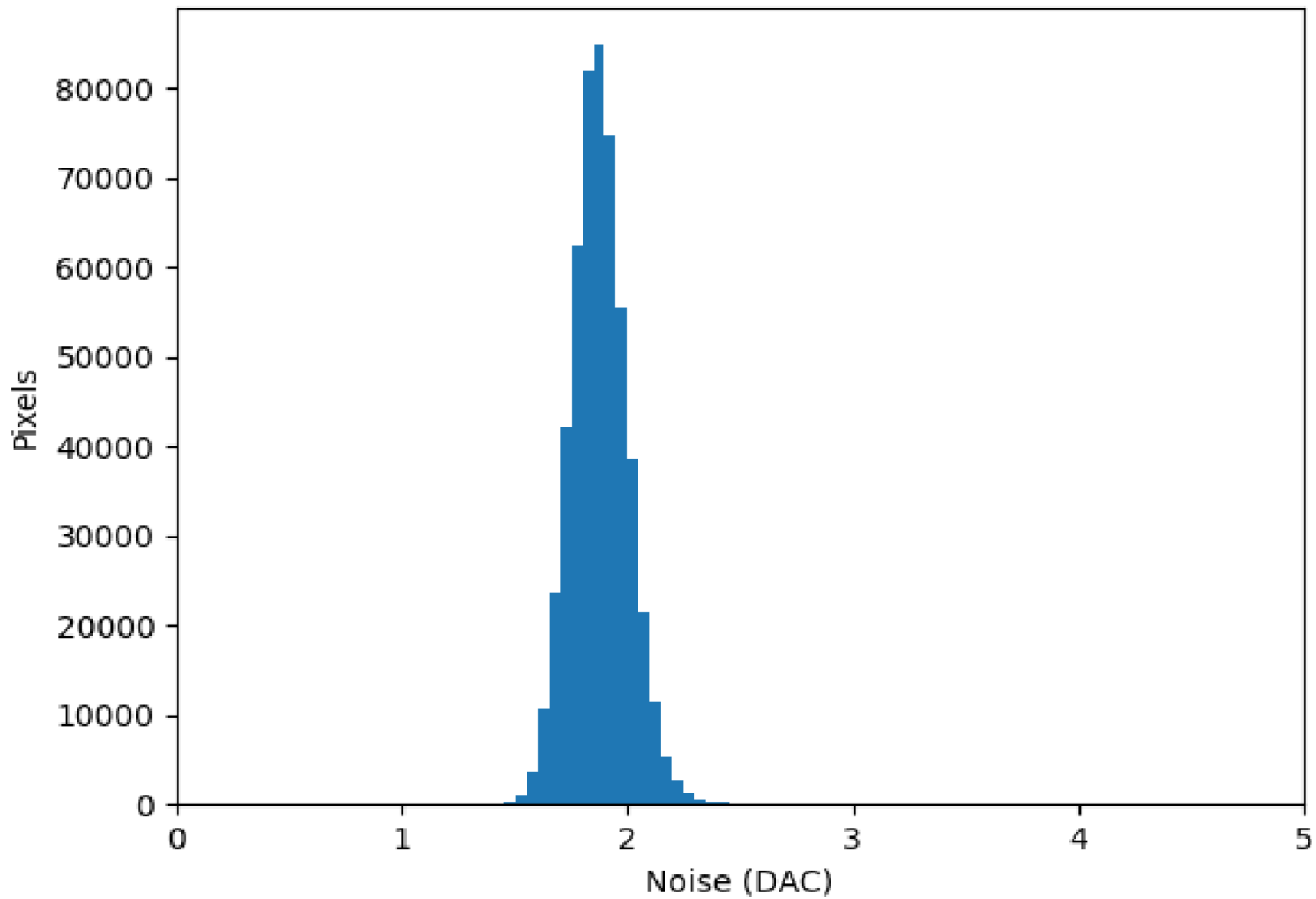


JINR DAQ board at SPbU, latest firmware

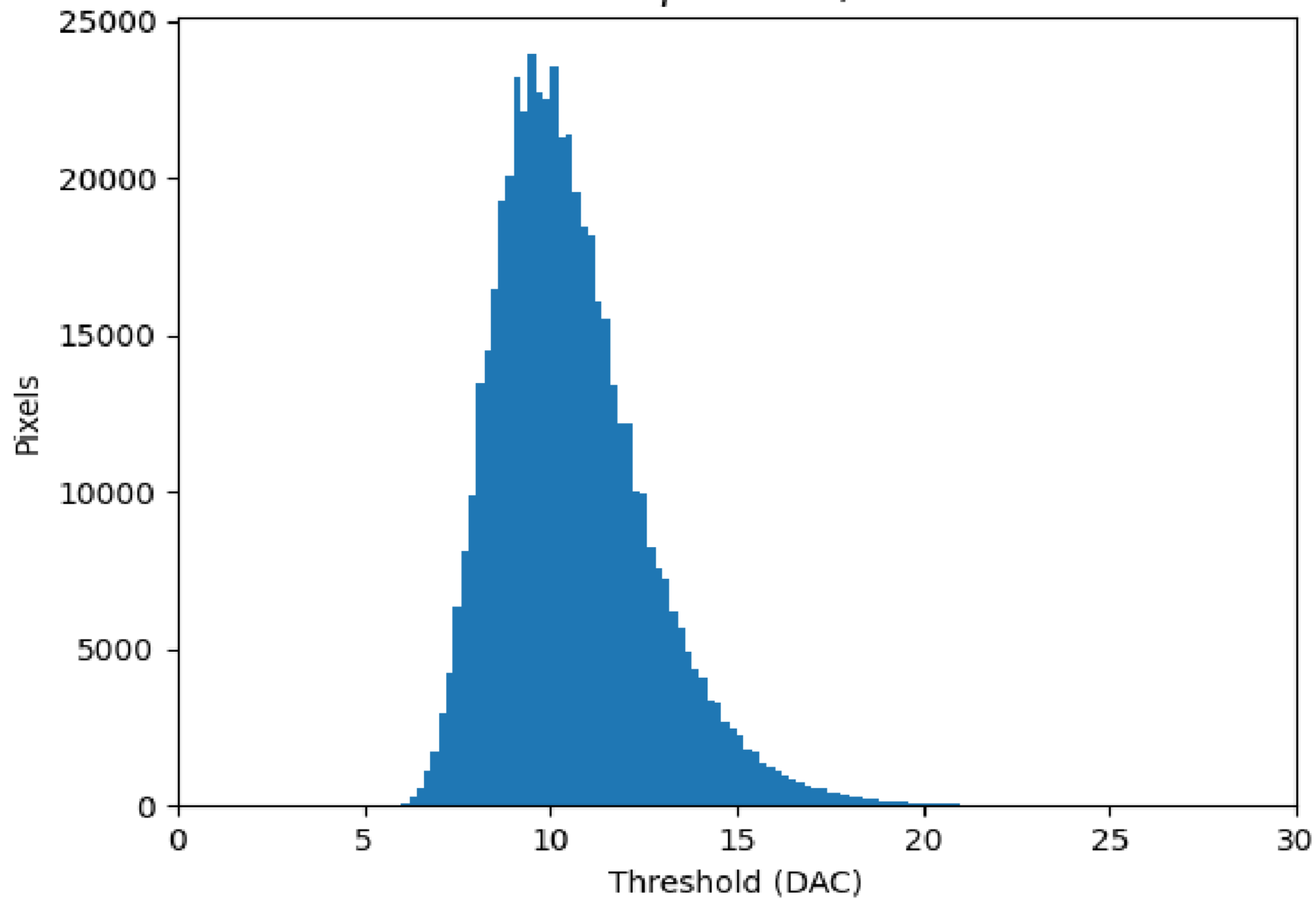
JINR DAQ board at CERN, latest firmware

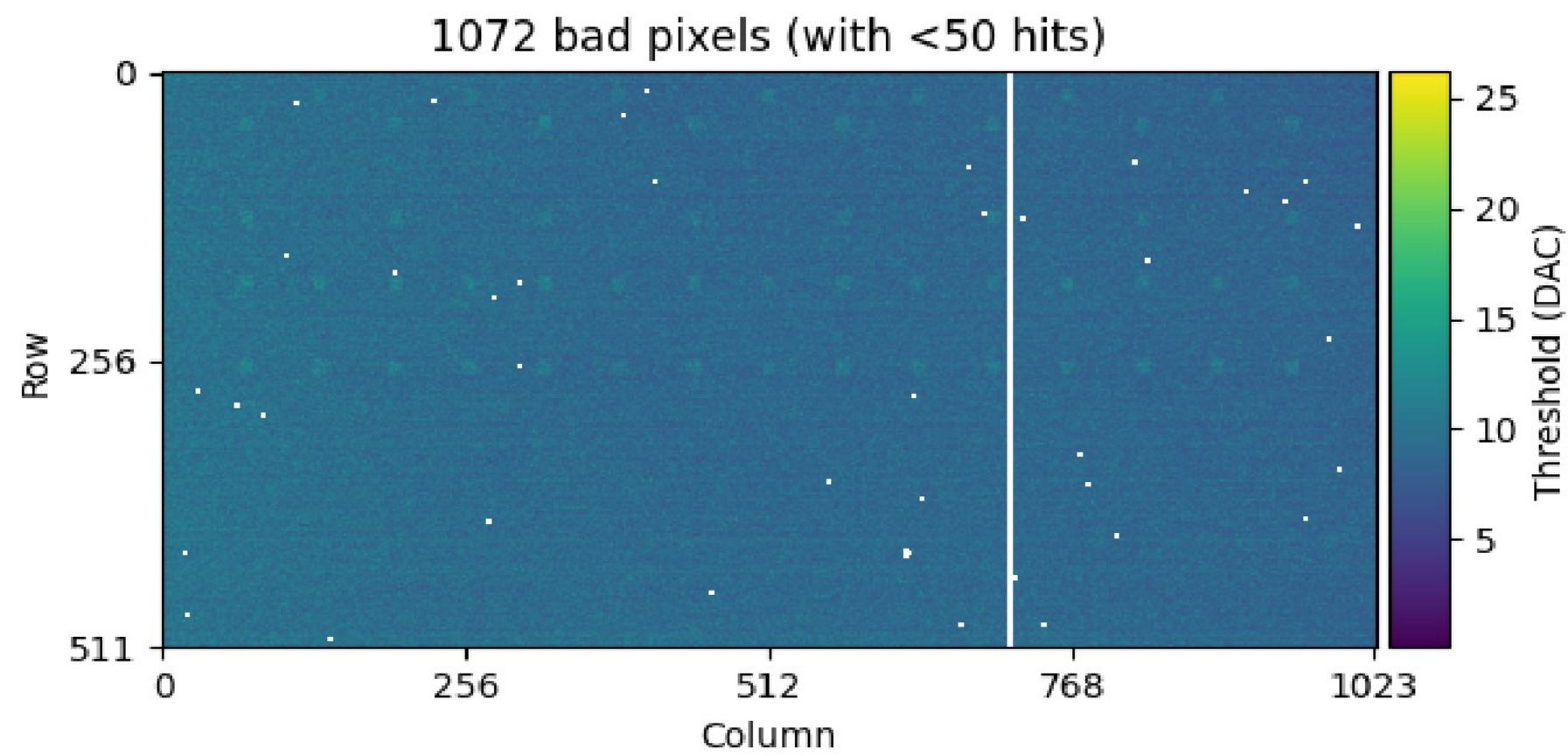


Noise: $\mu = 1.88$, $\sigma = 0.13$

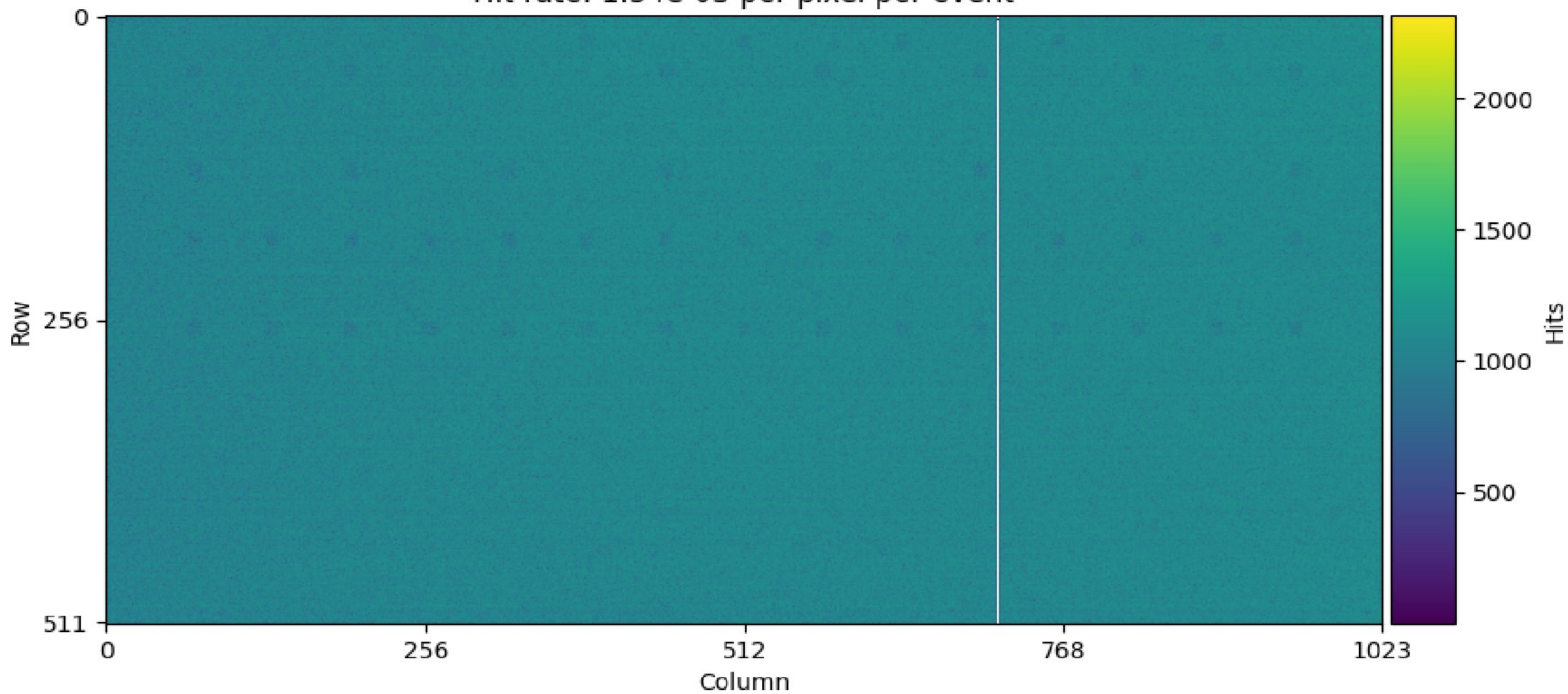


Threshold: $\mu = 10.56, \sigma = 2.05$





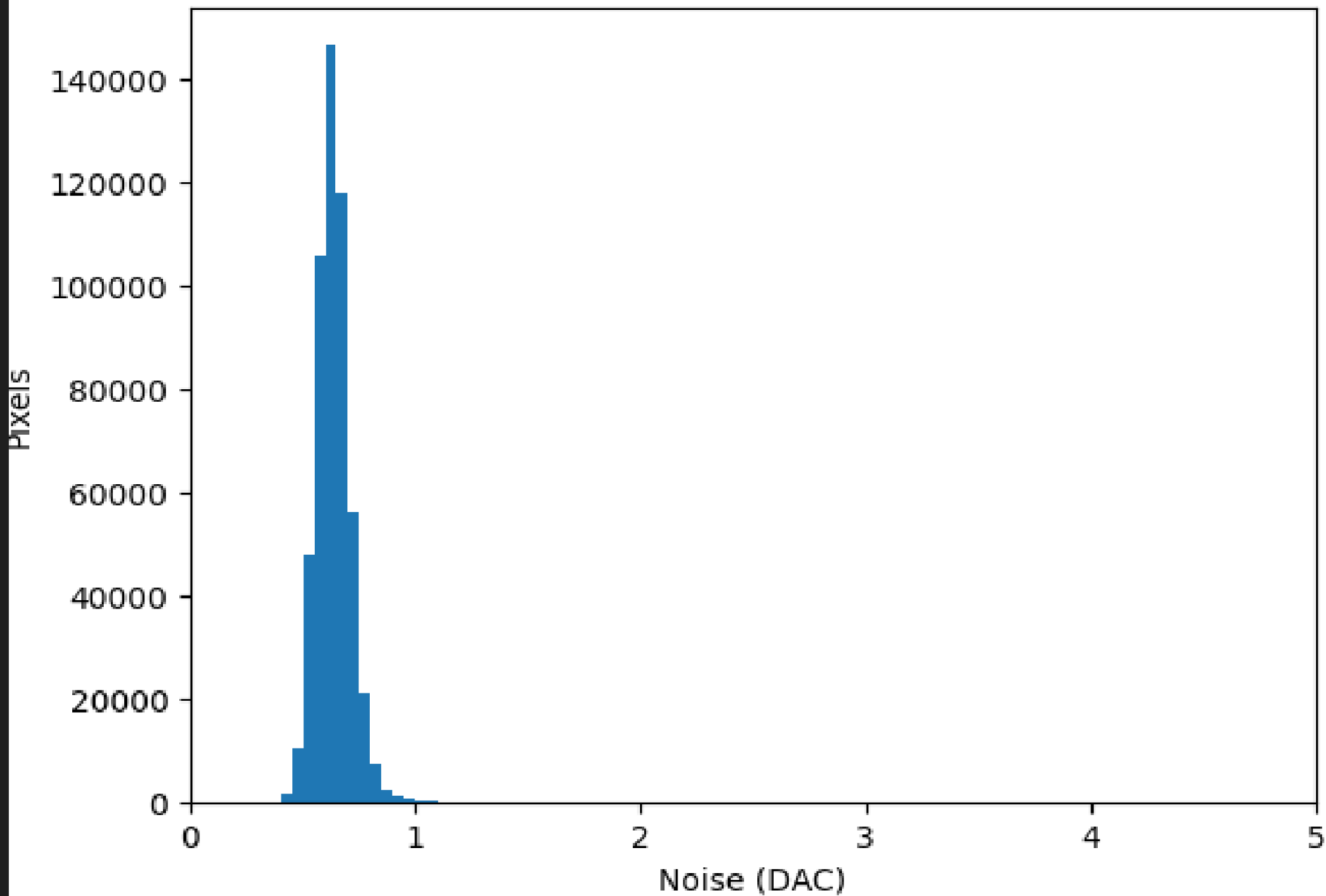
Hit rate: 1.34×10^{-3} per pixel per event



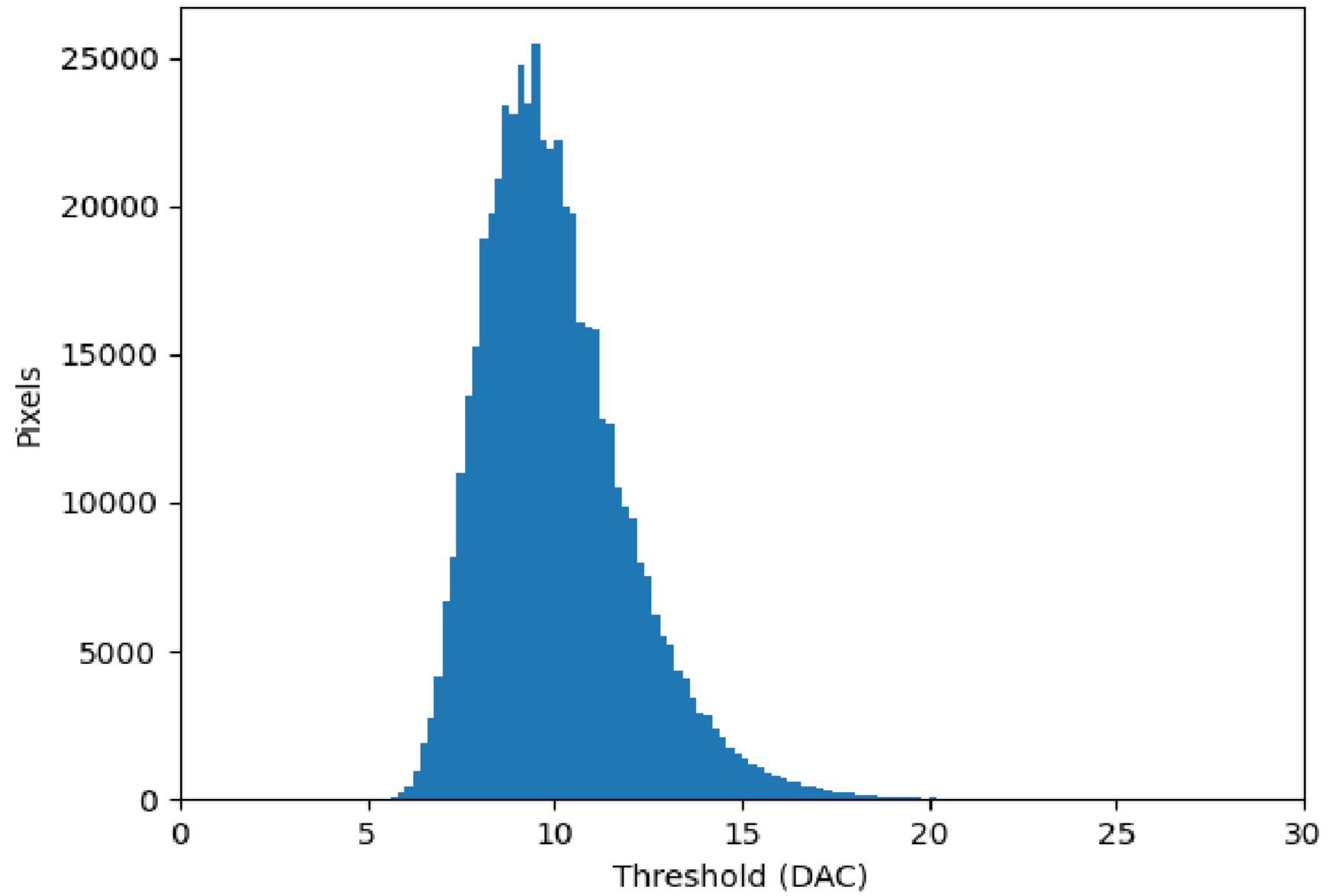
CERN DAQ board, latest official firmware

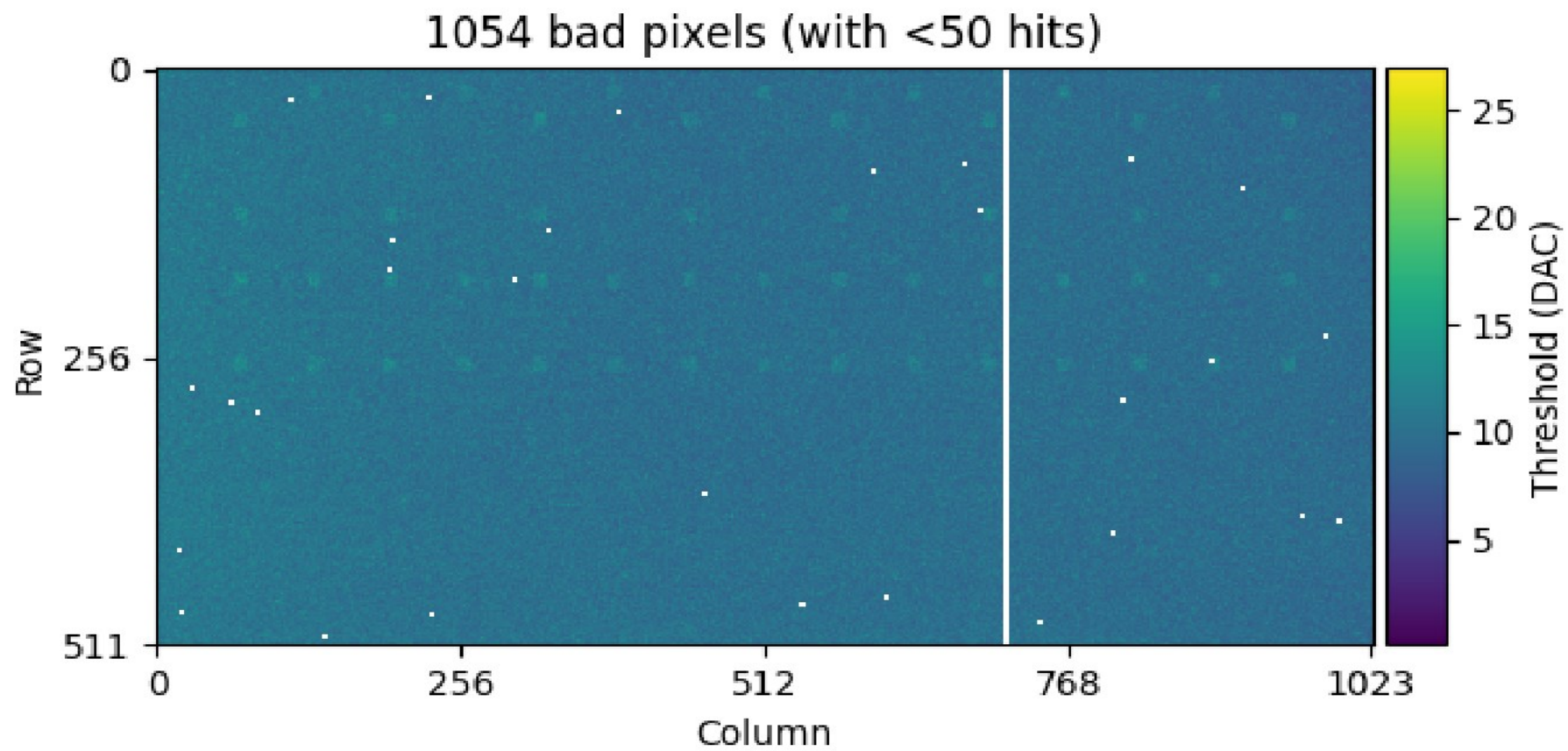


Noise: $\mu = 0.64$, $\sigma = 0.09$



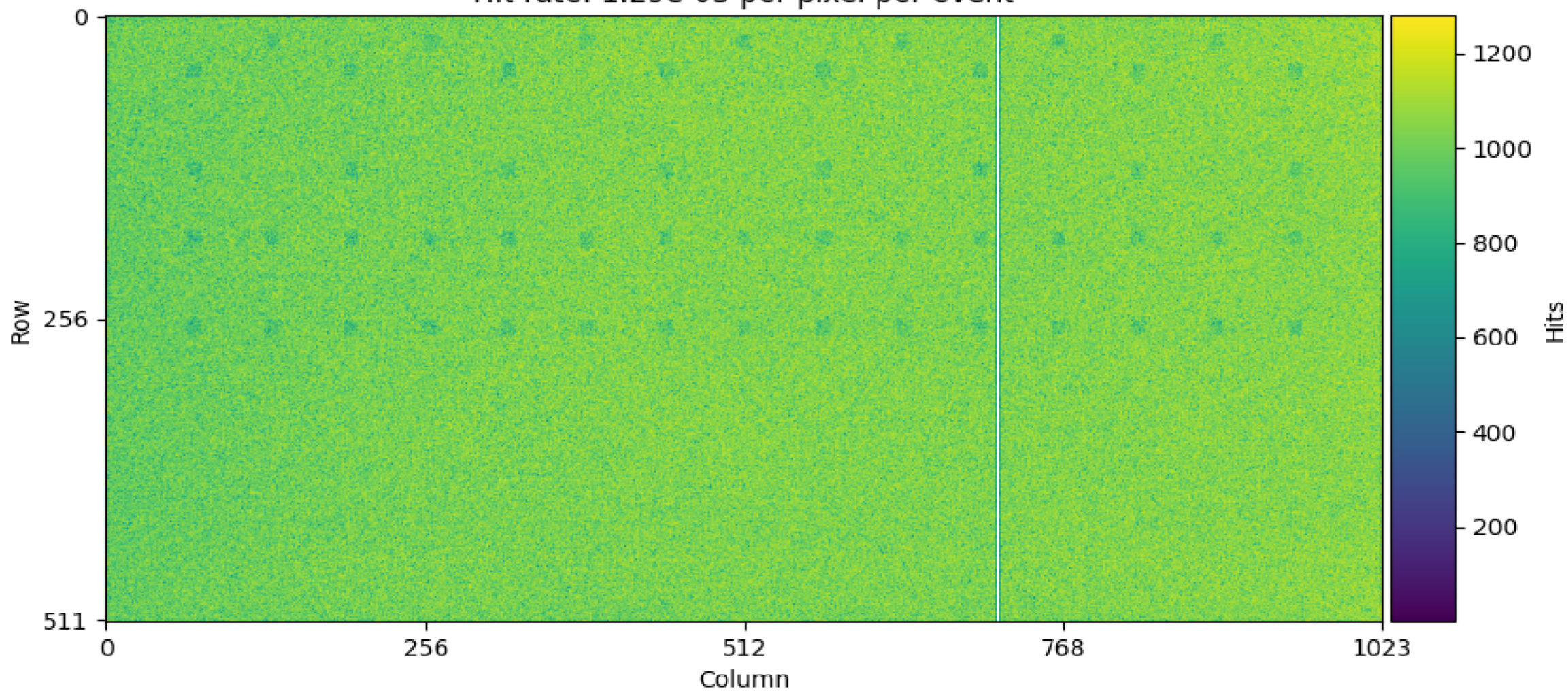
Threshold: $\mu = 10.04$, $\sigma = 1.97$





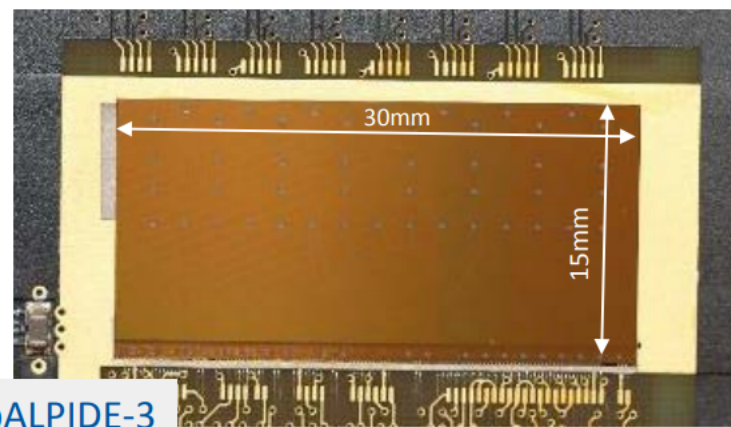
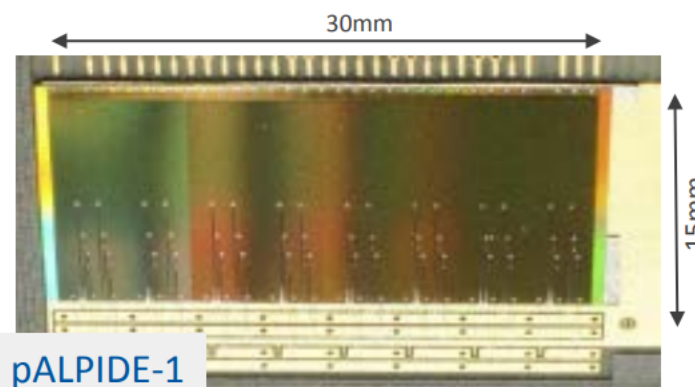
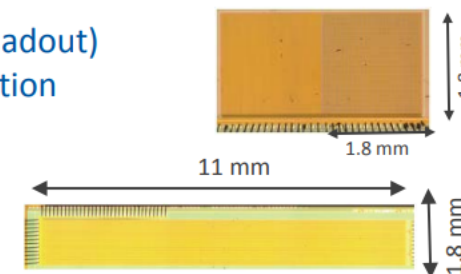
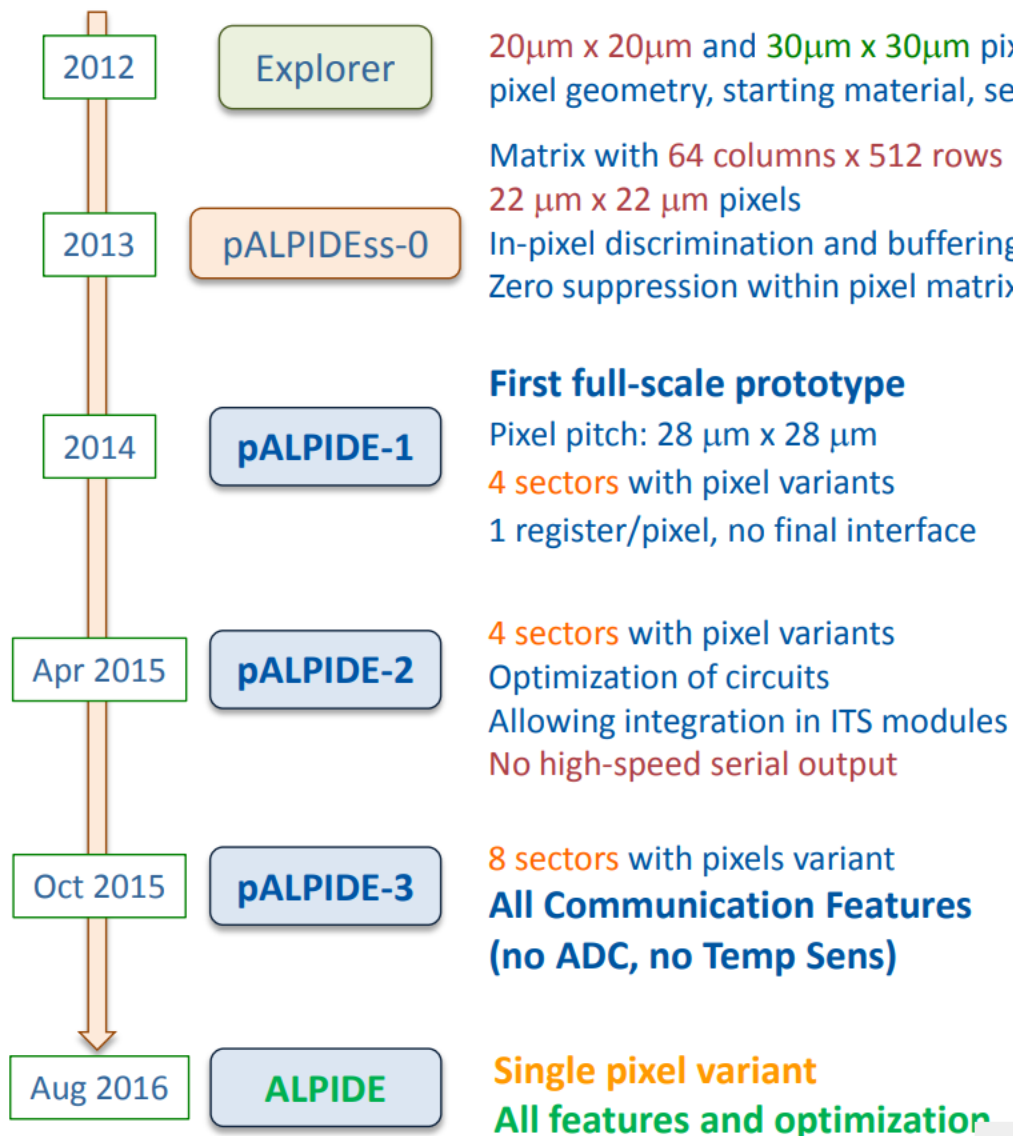


Hit rate: $1.29e-03$ per pixel per event



Development Roadmap

Press Esc to exit full screen



From pALPIDE-3 to ALPIDE, main design changes

1. Select and integrate **final pixel sensing diode and**
2. Improve routing of **pixels configuration control wires** under Pads Over Active Circuits
Solve weakness of wiring (row select lines in M5) under pads over circuits identified in pALPIDE-3

3. Optimize distribution of **global signals** from periphery

STROBE, MEMSEL, FLUSH, PULSE

Option to phase shift global pulses in time: mitigate risk of noise, optimize supply current time profile

Automatic rotation of PULSE: support **acceleration of pixel tests** with analog scans and charge injection

← EDR recommendation

4. Improve management of **pixel configuration signals** from periphery

Enable **fast reload of pixels mask** even during readout. Support active forcing of the mask bits from periphery

Mitigate potential impact of SEUs in pixel mask registers

← EDR recommendation

From pALPIDE-3 to ALPIDE, main design changes (2/2)



5. Optimize CMOS IO drivers

Improve series termination. Increase timing margins on OB Module Local Bus. Verify adequate on-chip decoupling with more detailed analog sims.

← EDR recommendation

6. Separation of on-chip PLL power distribution network

Mitigation of excess jitter induced by noise on power supply

7. Full triplication of global asynchronous RESET signals in Digital Periphery, DTU-PLL, DTU-Serializer

Improve resilience to SEUs and SETs

← EDR recommendation

8. Clock gating of digital periphery modules

Optimization of digital power consumption

9. Add **new ADC module, Temperature Sensor** and related digital features for analog monitoring