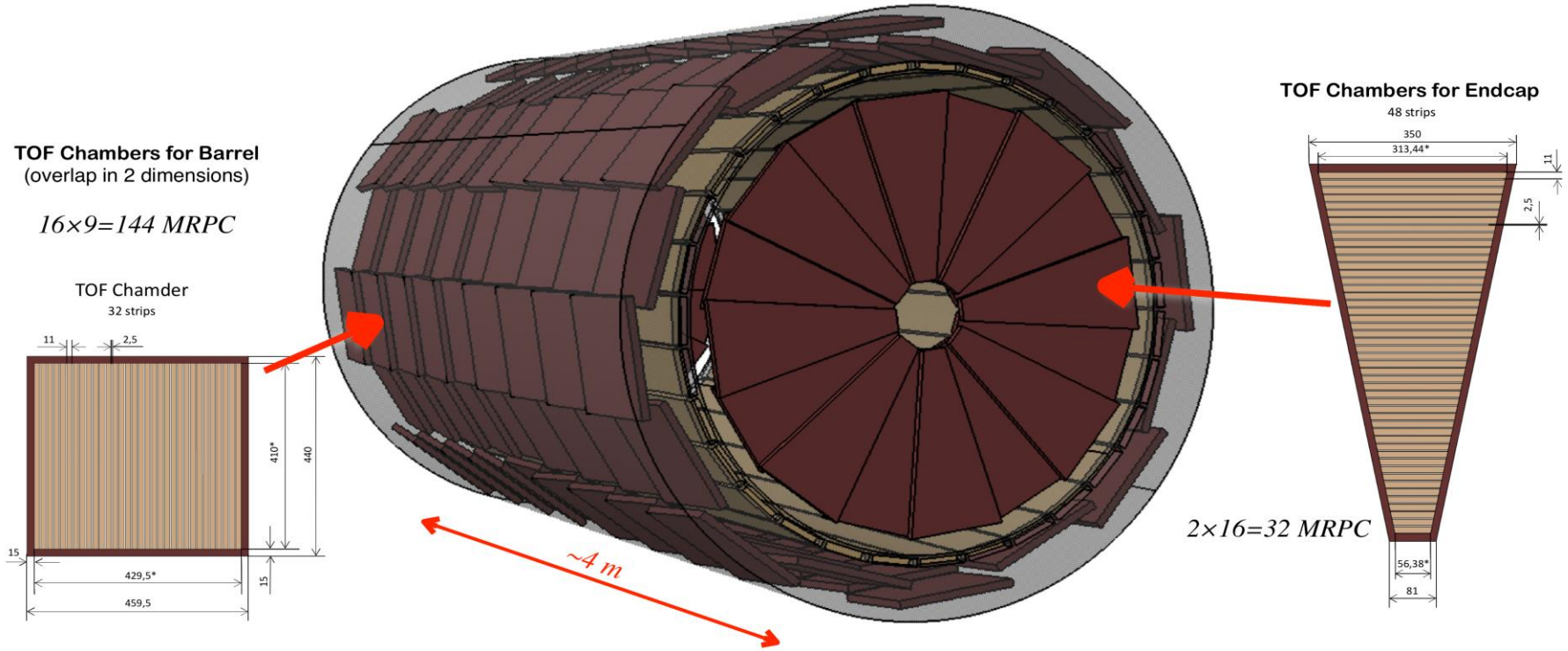
Time of Flight Detector
Status Report

Valery Chmill

Time of Flight (TOF) the last version



- π/K/p discrimination for momenta ≲2 GeV
- Determination of t0
- Time resolution requirement <60 ps.
- Sealed (MRPC) are the base option. B.Wang et al, JINST 15 (2020) 08, C08022

- Number of readout for Barrel is 144x2x32=9216 channels.
- Number of readout for Endcap is 32x2x48=3072 channels.
- Total amount is 12288 channels

PID for m^2 vs. p

- π/K/p/d discrimination for momenta <2 GeV
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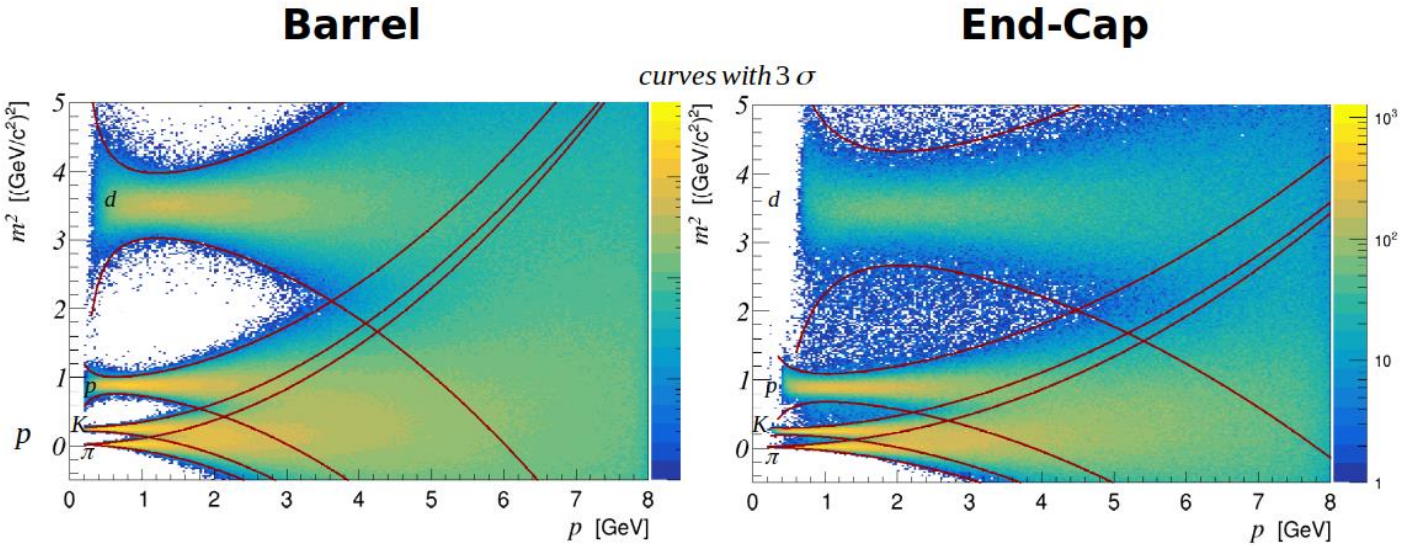
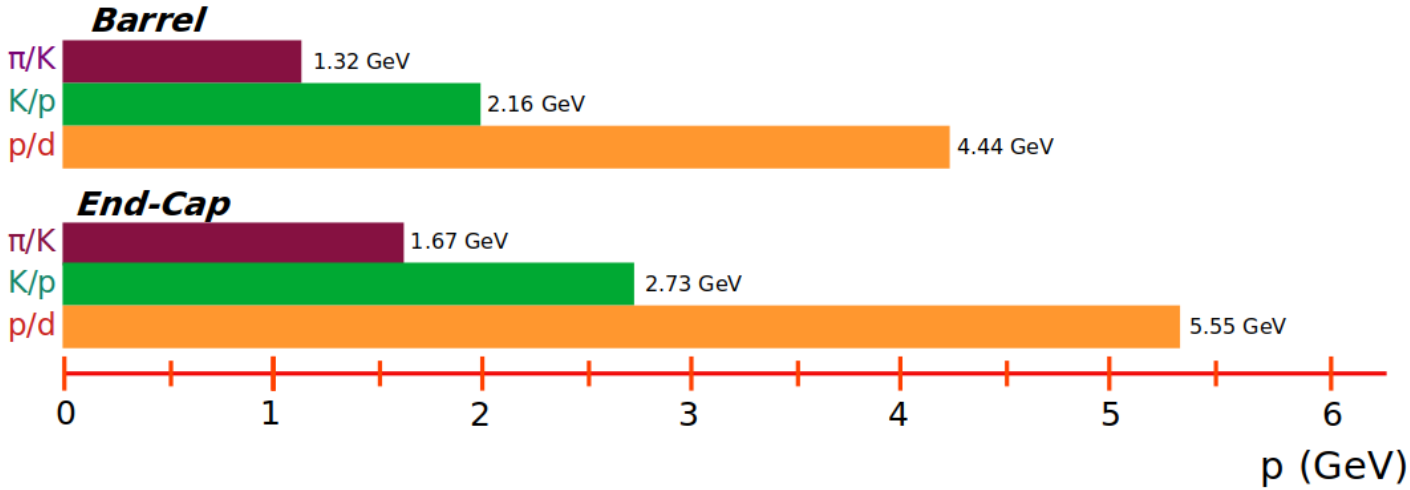
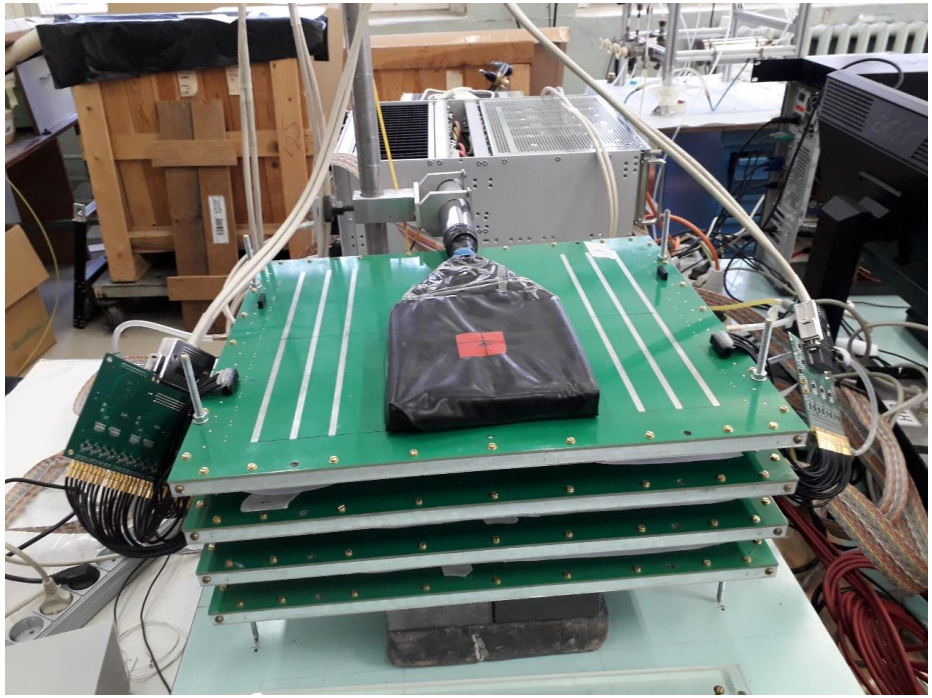
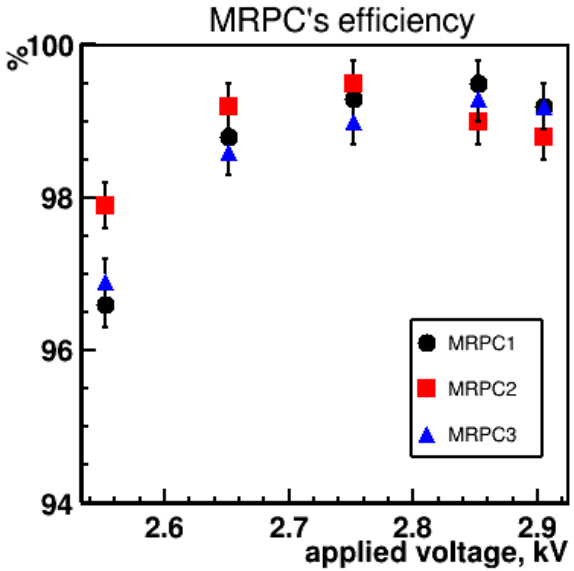
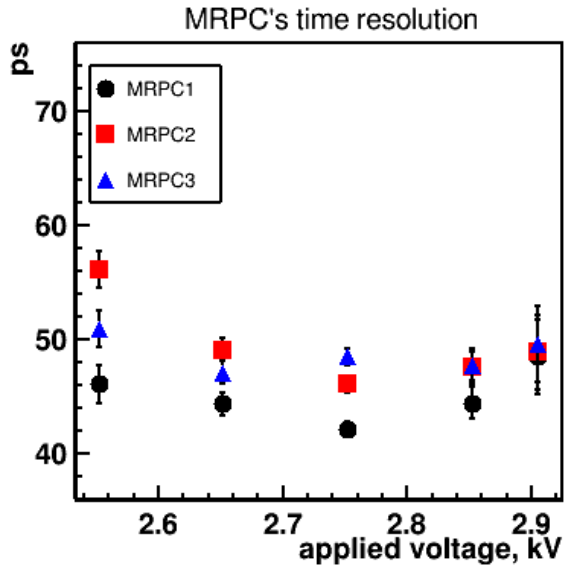




Protvino MRPC prototype for SPD project at NICA

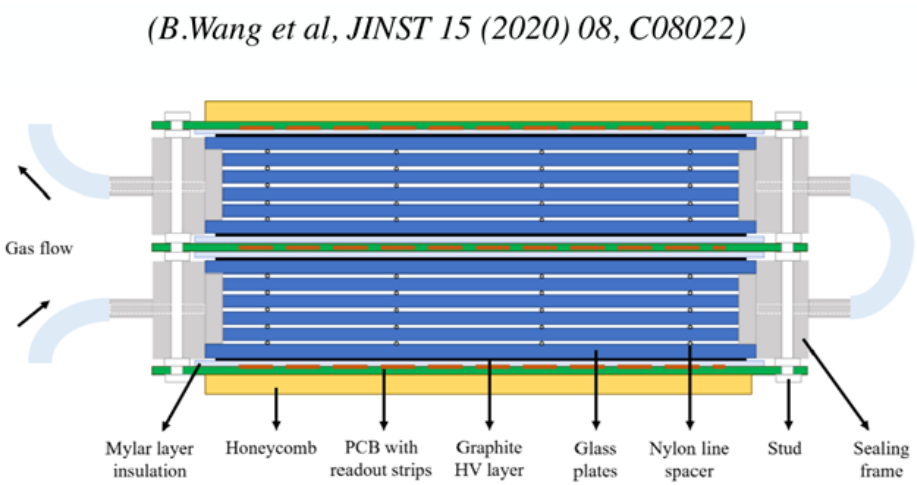


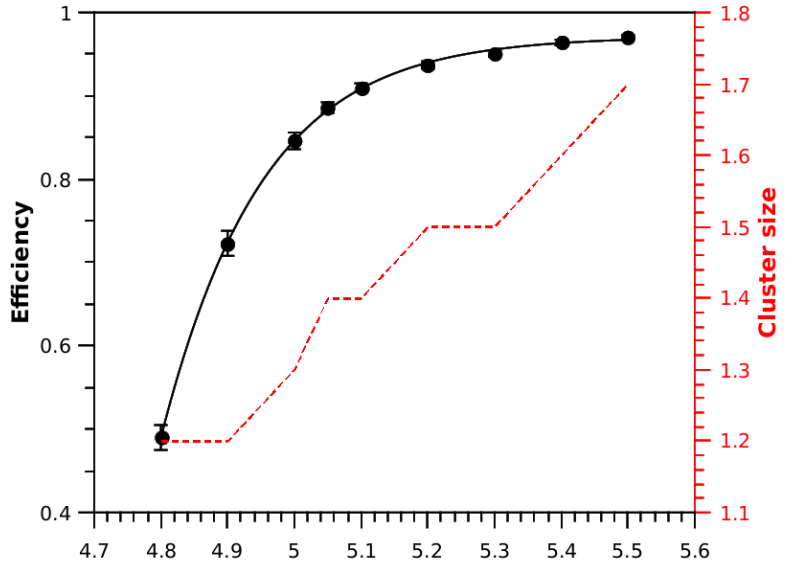




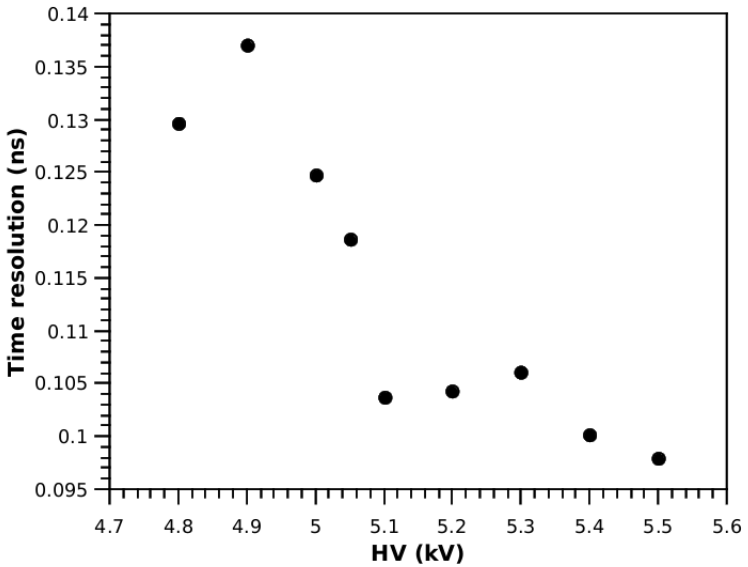
- To start MRPC and check functionality
- To obtain detection efficiency and time resolution on a new DAQ
- Preparation for using 3 MRPC as a servicing system at TEST AREA (Anton Baldin).

Sealed (MRPC) are the base option of today

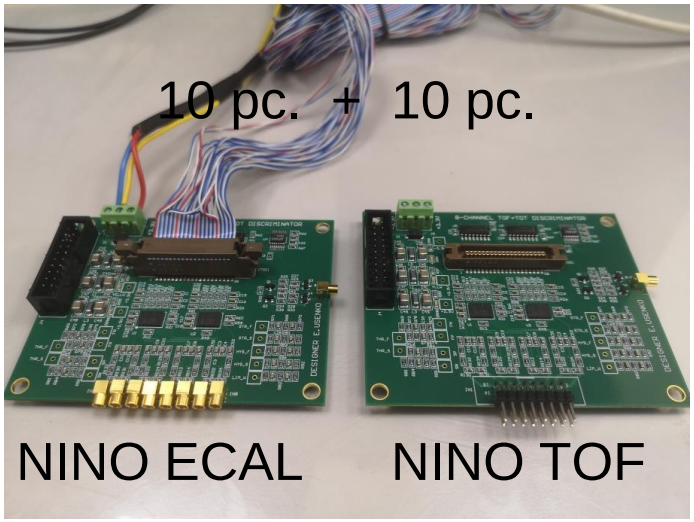




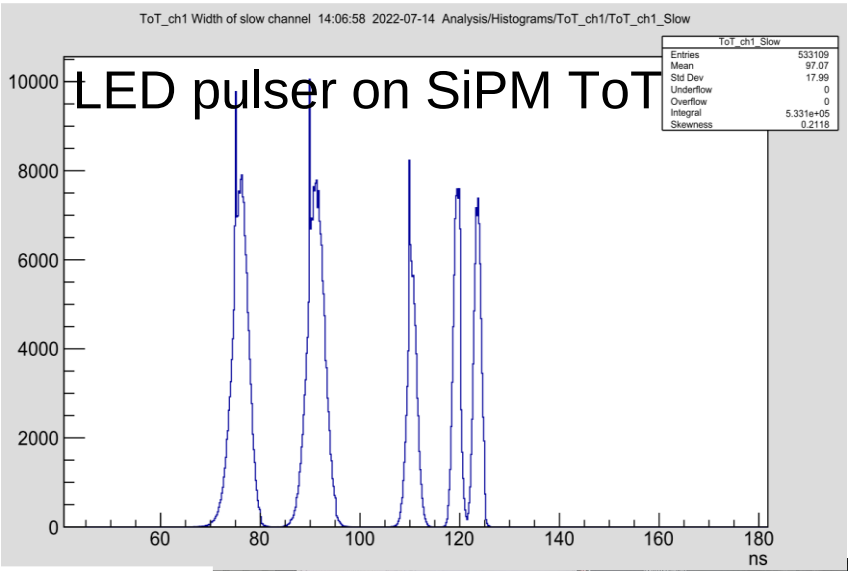
- The prototype was tested in cosmic rays along with 2 MRPC2 counters in the TRBv3 test stand.
- The plateau efficiency is 97%, with a 1.6 cluster size and a 100 ps flight-time resolution.
- The systematic time resolution of the prototype is about 60 ps. if we reasonably expect the same timing precision between two MRPCs.
- The prototype has the same working point at ±5.4 kV with standard gas flow (Freon/iC_4H_{10} = 90/5/5

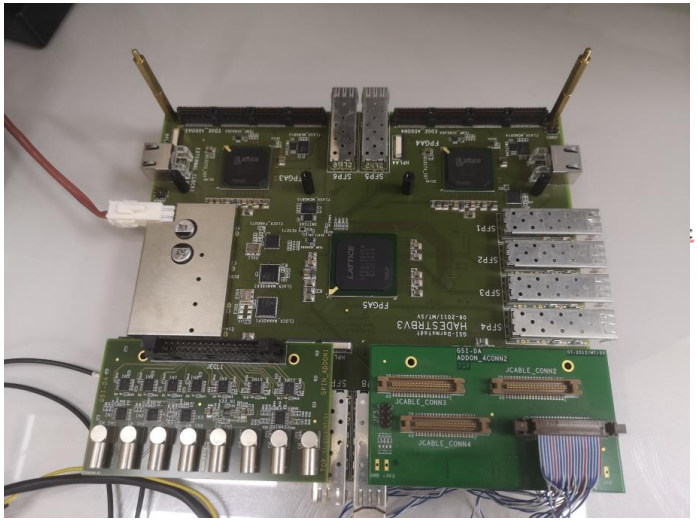


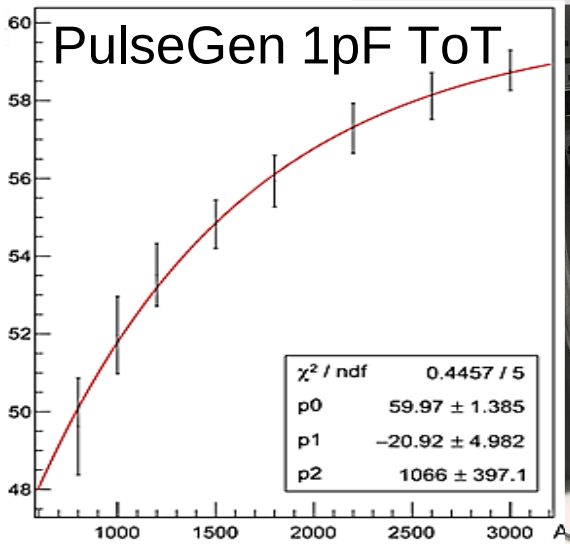
TRBv3 and FEE preliminary test

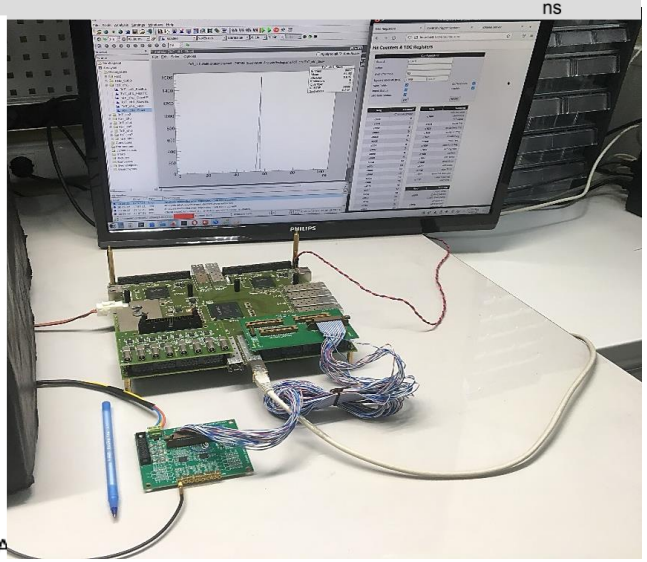


10ps bin weight in TDC mode ShortUsersGuide to the TRBv3 contains 139pp.









TDC-Readout-Board, Triggered/Triggerless-Readout-Board

Item	Value
Supply Voltage	48 V (40-50V), galvanically isolated on board
Power Supply Current	0.5A minimum without AddOns
GbE-connectivity	max. 95 MBytes/s transfer per link
GbE-slow-control	up to 400 registers/transfer, speed depends on GbE latency
Connectivity	Max. 8 SFPs, each 2GBit/s on board. With hub-addon: max. 32 SFP
	4 AddONs on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate	about 300 KHz (depending on configuration and network size)
Max Hit Rate	50 MHz (burst of 63 hits)
TDC Channels	260 (Single edge detection)
Time Precision	<20 ps
Minimum pulse width	<500 ps

TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

Possible FEE and Digitization

https://www.caen.it/subfamilies/fers-5200/

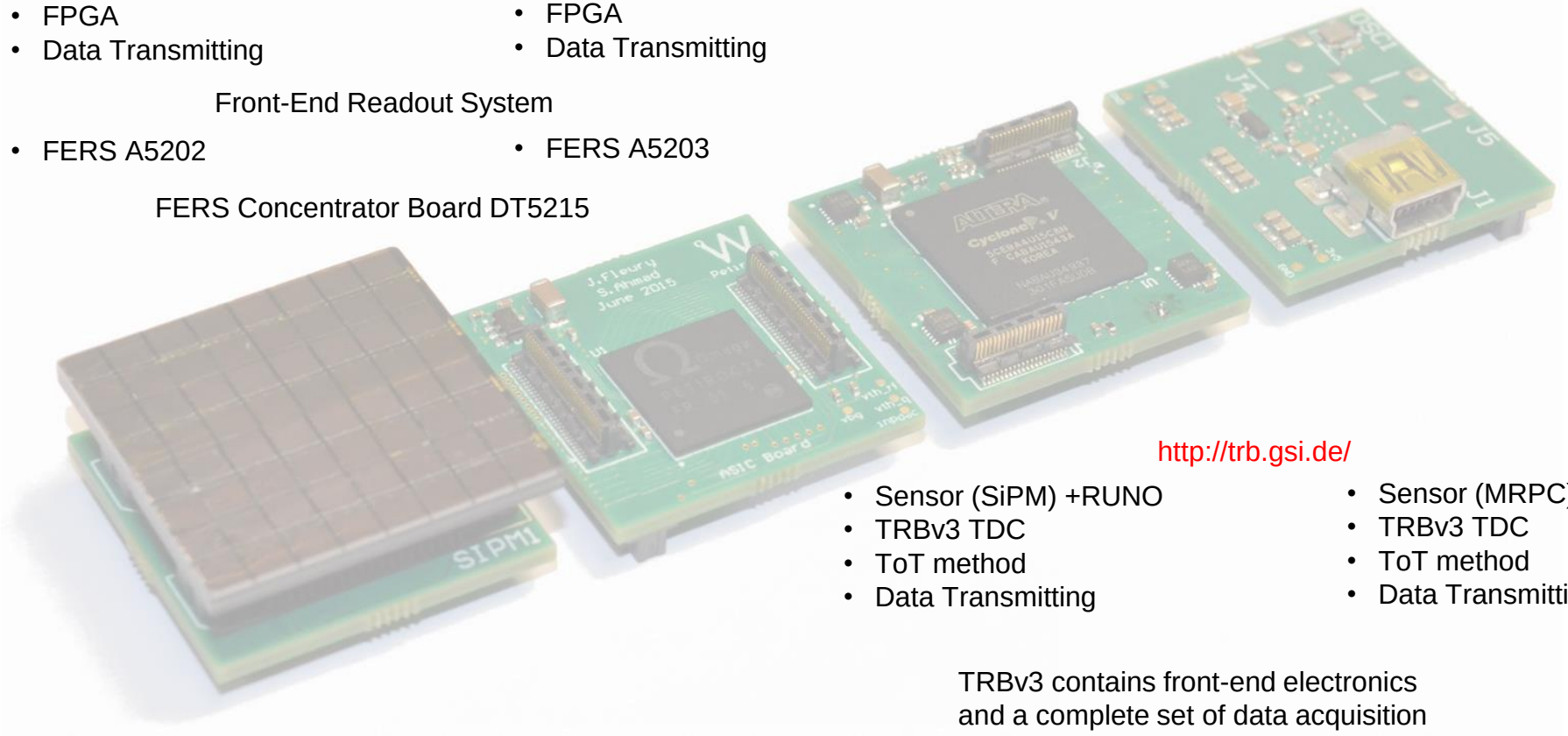
- Sensor (SiPM)
- ASIC (WEEROC family, citiroc-1A)
- FPGA
- Data Transmitting

- Sensor (MRPC) + NINO
- ASIC (picoTDC)
- FPGA
- Data Transmitting

Front-End Readout System

- FERS A5202
- FERS A5203

FERS Concentrator Board DT5215



http://trb.gsi.de/

- Sensor (SiPM) +RUNO
- TRBv3 TDC
- ToT method
- Data Transmitting

- Sensor (MRPC) + RUNO
- TRBv3 TDC
- ToT method
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TRBv3 contains front-end electronics and a complete set of data acquisition and control software.

FERS FERS+NINO vs. TRBv3 FPGA-TDC+RUNO

The only way to do great work is to love what you do. ©

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- **Sergei Morozov, Evgeni Usenko**

- **Artem Ivanov**
- **Vladimir Ladygin, Aleksey Tishevsky**
- **Vadim Babkin, Mikhail Buryakov, Sviatoslav Buzin**

- **Yi Wang at al.**

- **Michael Traxler & the TEAM**

Thank you for your attention