Передовые инженерные школы

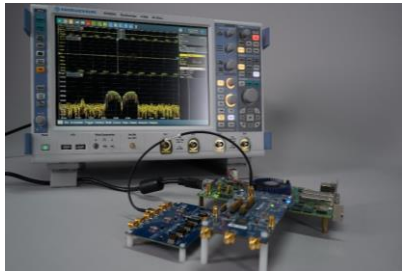
POLYTECH
Peter the Great St.Petersburg Polytechnic University

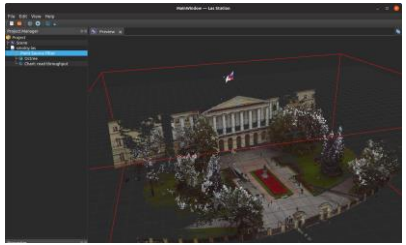
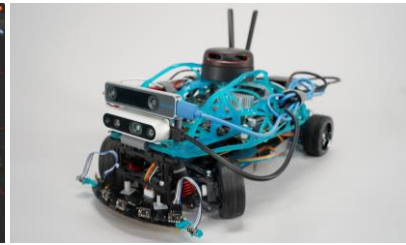
ЦИФРОВОЙ ИНЖИНИРИНГ
ПИШ СПбПУ

WCRC
ADVANCED DIGITAL TECHNOLOGIES

POLYTECH
Advanced Manufacturing Technologies Center
National Technology Initiative

POLYTECH
Laboratory
Industrial Systems for Streaming Data Processing



SPD collaboration meeting

October 24th, 2023

White-Rabbit evaluation device for SPD TSS prototyping

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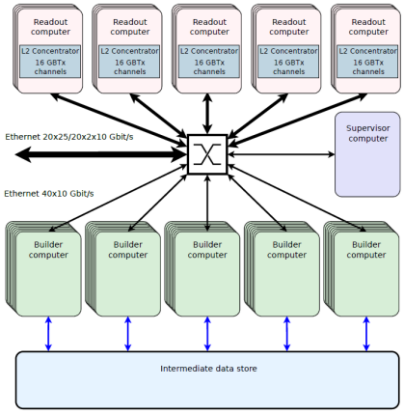
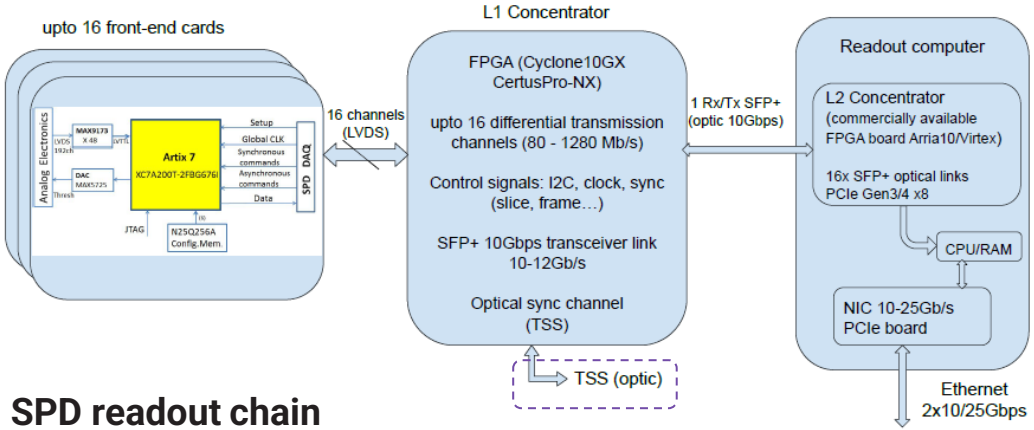
TSS instead of TCS

- TCS – Trigger and Control System
- TSS – Time Synchronization System
- Triggerless
- Higher precision
- Versatile
- More complex

- Synchronizes with NICA
- Propagates bunch crossing signal into DAQ system
- Synchronizes all the DAQ units
- Controls data acquisition process

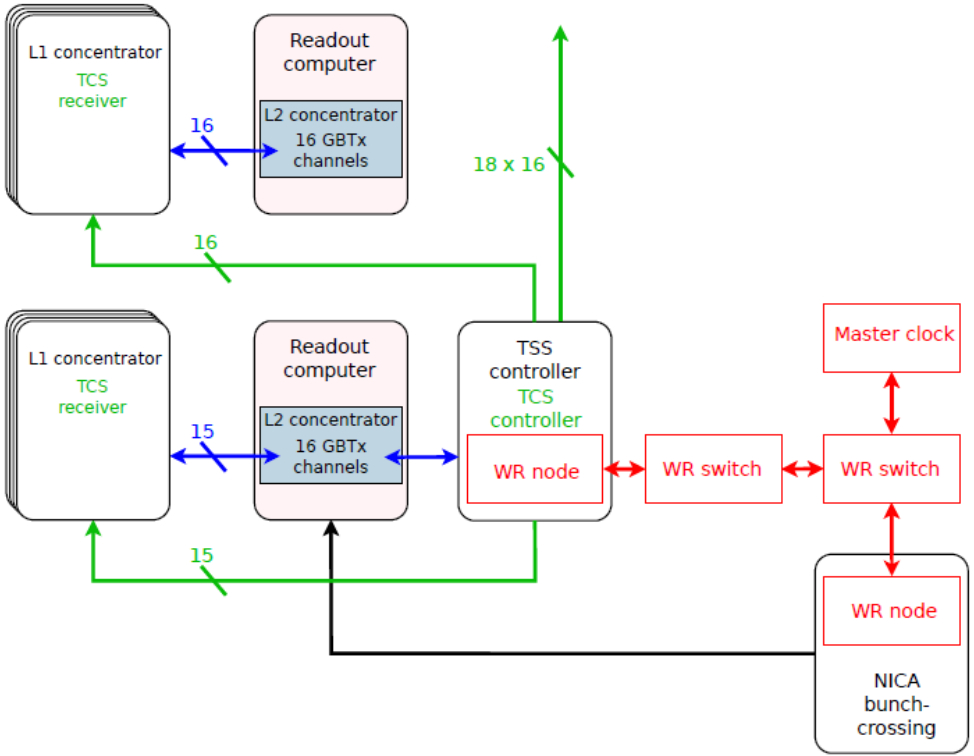


SPD slice building



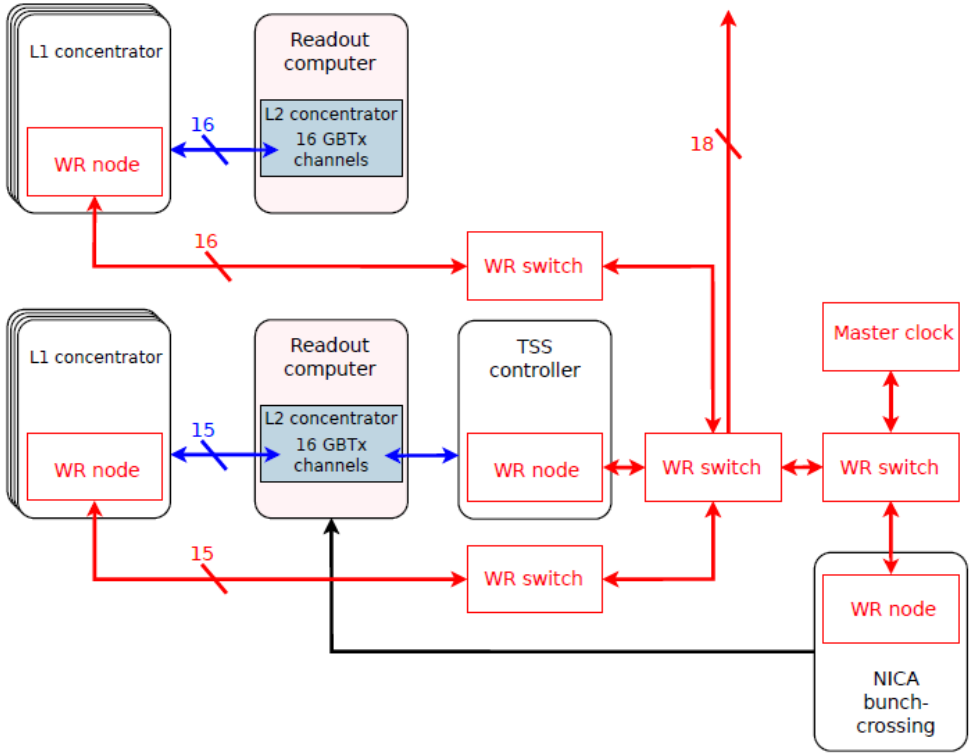
SPD readout chain

TSS architecture options. TCS-based approach



- TCS – well-known method of clock and control distribution
- TSS should have different interfaces for NICA and for DAQ
- Might be difficult to achieve the required 1 ns accuracy

TSS architecture options. WR-based approach



- WR PTP – standard protocol developed and widely used by CERN
- Same interfaces for all connections
- More elegant but expensive and sophisticated solution
- Guaranteed accuracy is much better than 1 ns

White Rabbit in TSS

- No matter what option we will choose – anyway TSS will contain at least one WR node.
- NICA uses White Rabbit protocol, so it is the most convenient way for SPD-DAQ to obtain synchronization with NICA.
- Decided to start from developing WR-compatible hardware platform.
- It should have enough resources and performance.

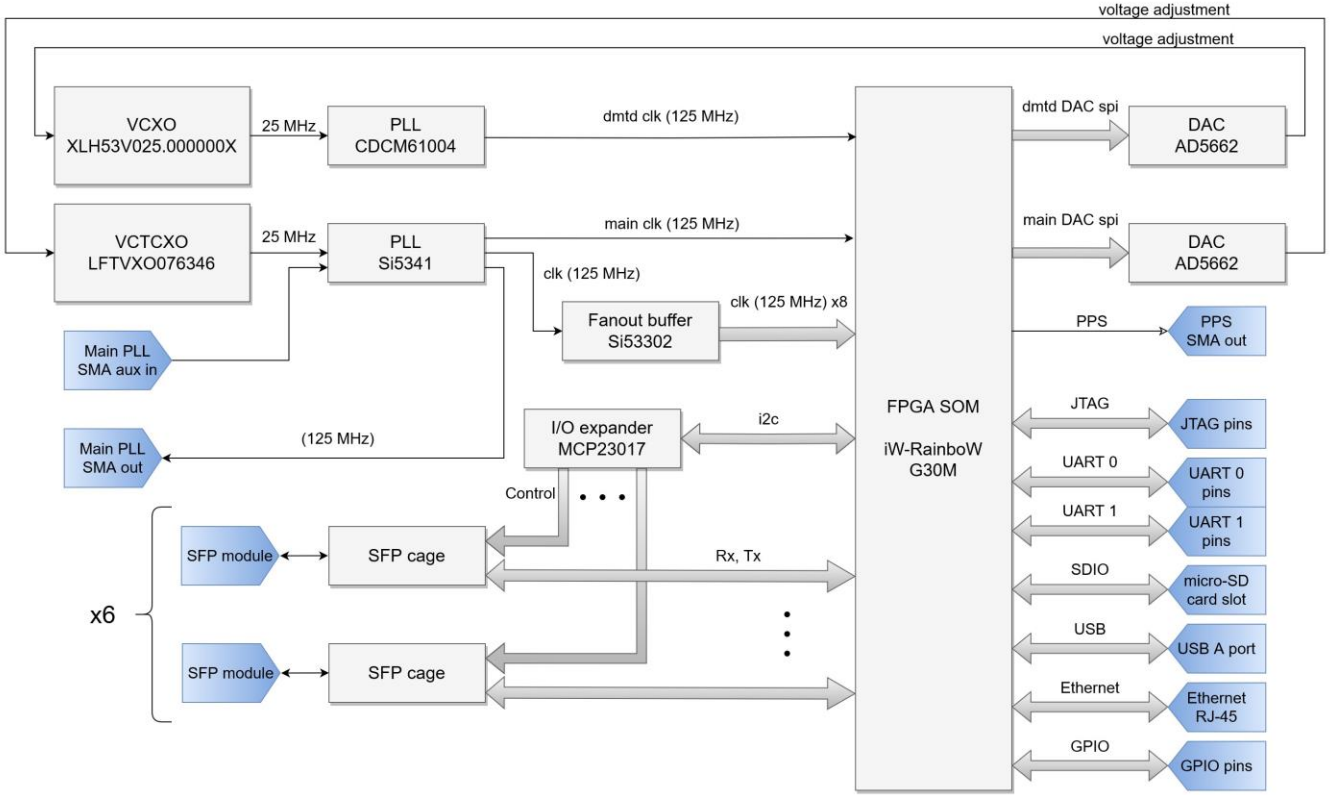
TSS development roadmap

• **HW platform: Schematic and PCB** • **White Rabbit node project porting to the HW platform**	**2022**
• TSS design option choosing: TCS-based or WR-based • TSS control protocol implementation	**2023**
• In-system debugging and testing	**2024**
• NICA interface implementation • White Rabbit switch project implementation	**Optional**

White-Rabbit evaluation board. FPGA

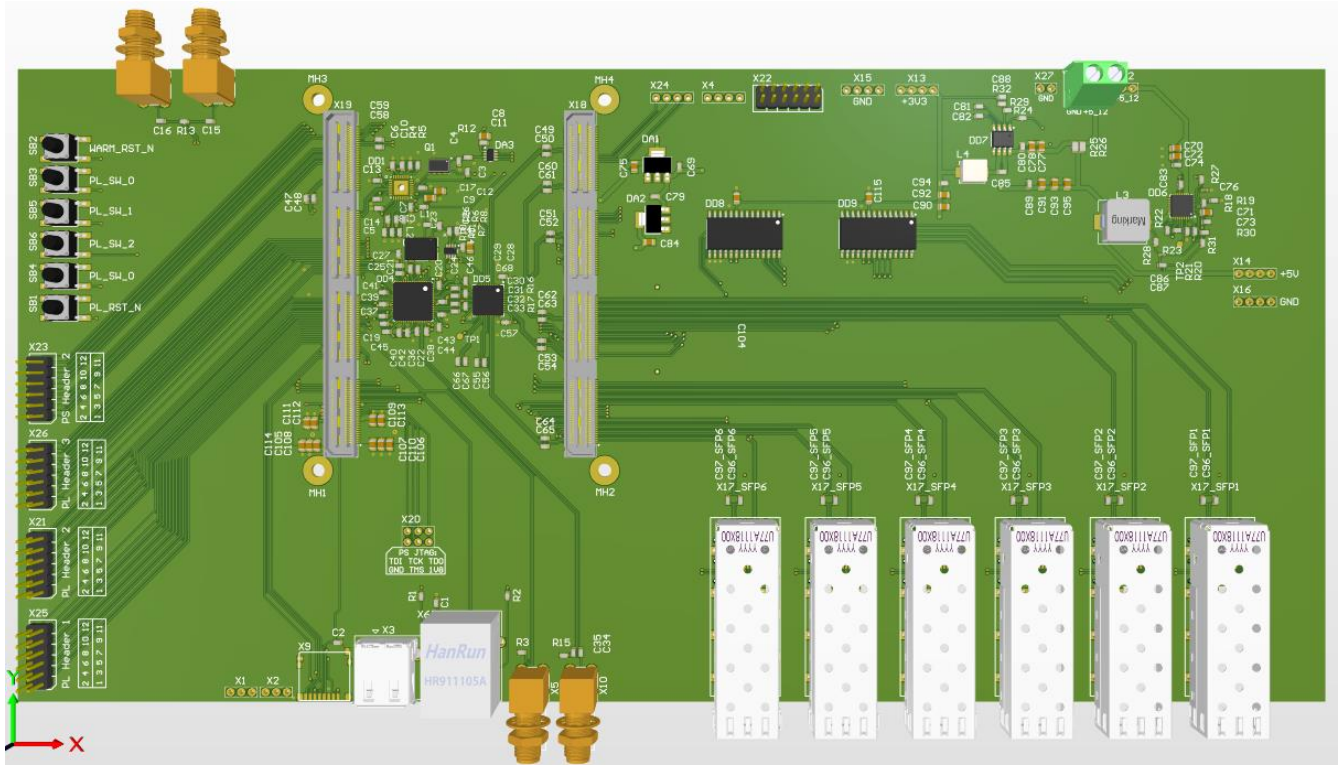
- Xilinx Zynq UltraScale+
- iWave iW-RainboW-G30M SoM with everything needed on-board
- Up to 504K Logic cells & 230K LUTs
- PL GTH High Speed Transceivers x 16 @ 16.3 Gbps
- DDR4 RAM: 4GB on PS, 2GB on PL
- Flash: 8GB eMMC
- ARM Cortex-A53 hard processor system on-board – some TSS functions could be implemented in software

White-Rabbit evaluation board. Top level view

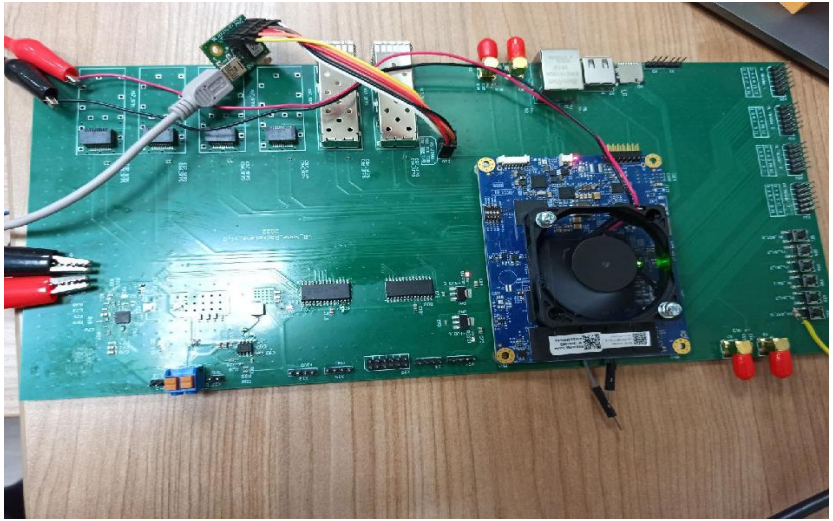


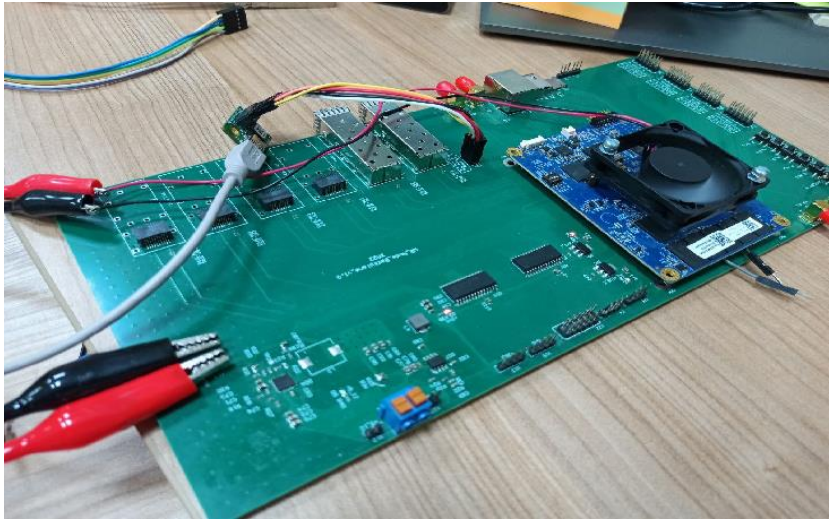
White-Rabbit evaluation board. PCB

- Custom board based on CERN White Rabbit reference design
- Multi-port baseboard with WR switch functionality – could be a multipurpose device



White-Rabbit evaluation board. PCB

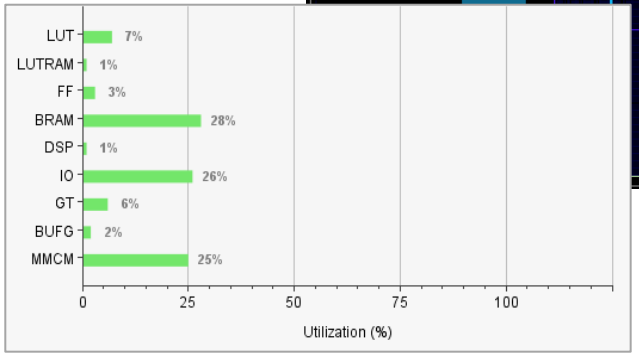


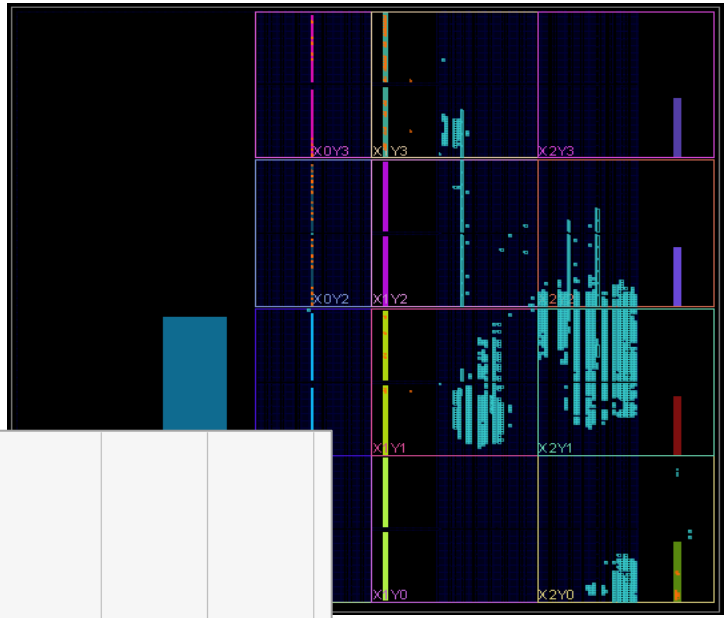


FPGA project

- Taken the most relevant WR reference design for Xilinx Zynq UltraScale+ FPGA from CERN's open hardware repository
- Ported it to our hardware platform
- Hardware debug

Resource	Utilization	Available	Utilization %
LUT	5858	87840	6.67
LUTRAM	250	57600	0.43
FF	5976	175680	3.40
BRAM	36	128	28.13
DSP	3	728	0.41
IO	53	204	25.98
GT	1	16	6.25
BUFG	7	352	1.99
MMCM	1	4	25.00





White-Rabbit evaluation board. Current and further steps

- Board setup and refinement
- Setup with SyncTechnology equipment: WRS-18A, Cute-WR-A7-PKG
- Evaluation different configuration our platform with SyncTechnology equipment

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