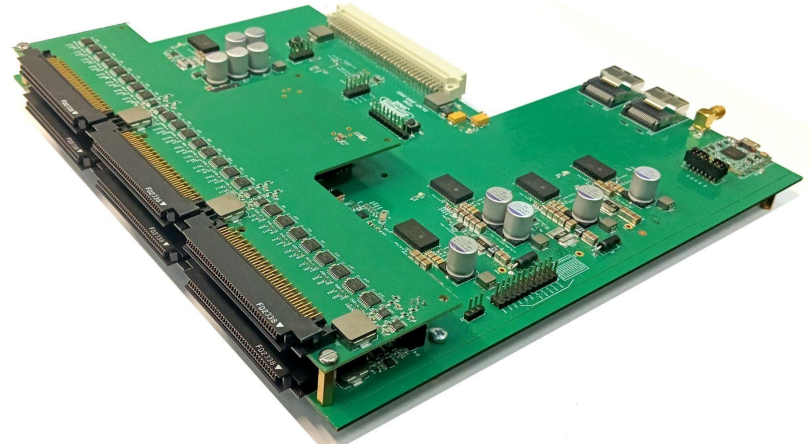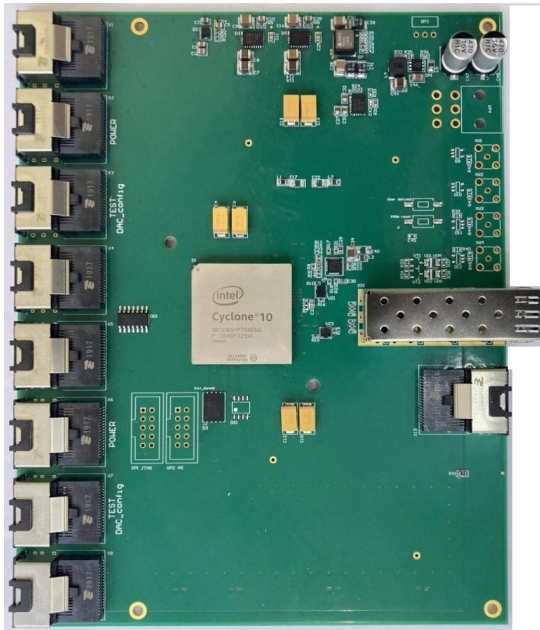# Status-quo of the L1, L2 concentrators

Tereshchenko Viacheslav
on behalf of DAQ group

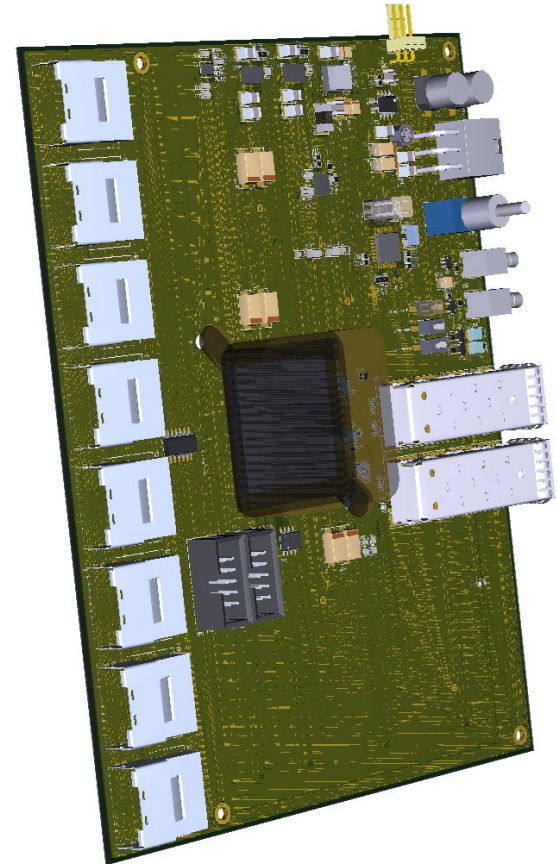# Front-end boards currently available for use

TDC 64 channels, 1ns resolution   MFDM 192 channels, 4ns resolution

0th version of the L1 concentrator board

- Designed on the Cyclone10GX FPGA
- 8x Links for frontend electronics boards (with miniSAS connectors)
- SFP+ 10Gb transceiver for data transmission
- SFP+ 10Gb transceiver for timing (White Rabbit)

AXP390 development board
# (Alinx, Titan-2 chip PG2T390H – 6IFFBG900)

AXP390

Titan-2 Platform Development Platform

Product parameters

- Based on PG2T390H-6IFFBG900 FPGA
- 8GB DDR4 64bit; 2GB DDR3 64bit
- 64MB QSPI FLASH
- x1 QSFP fiber optic interface, speed up to 40Gb/s
- x4 SFP optical fiber interface, each channel connection supports up to 10Gb/s

- 1 standard FMC LPC extension port, compatible with ALINX FMC boards
- 1 PCIe 2.0 x8 interface, single-channel communication rate up to 5Gbps
- Integrated Gigabit Ethernet, UART, TF card slot, JTAG and other common interfaces
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB
  Provides rich Demo source code and supporting tutorials, making it easier to get started
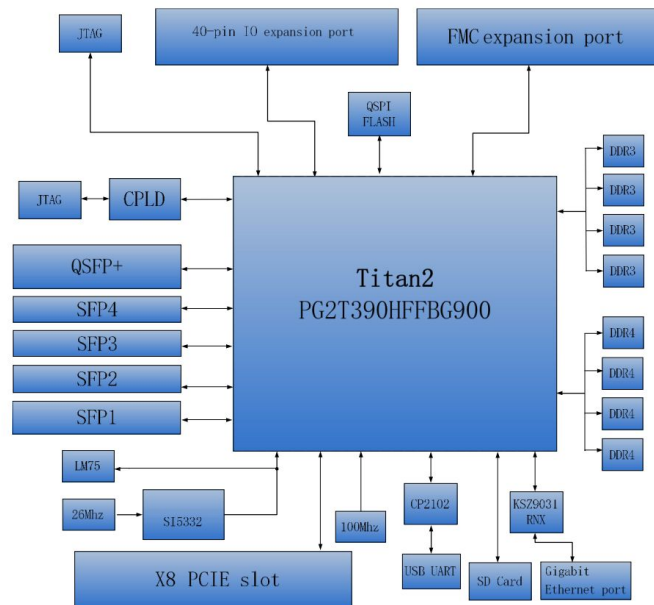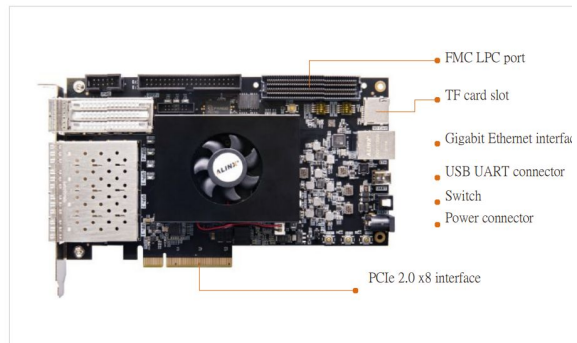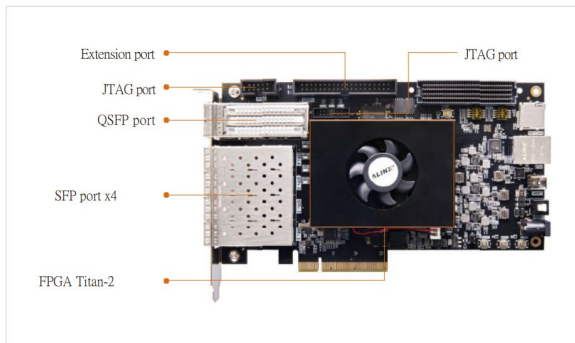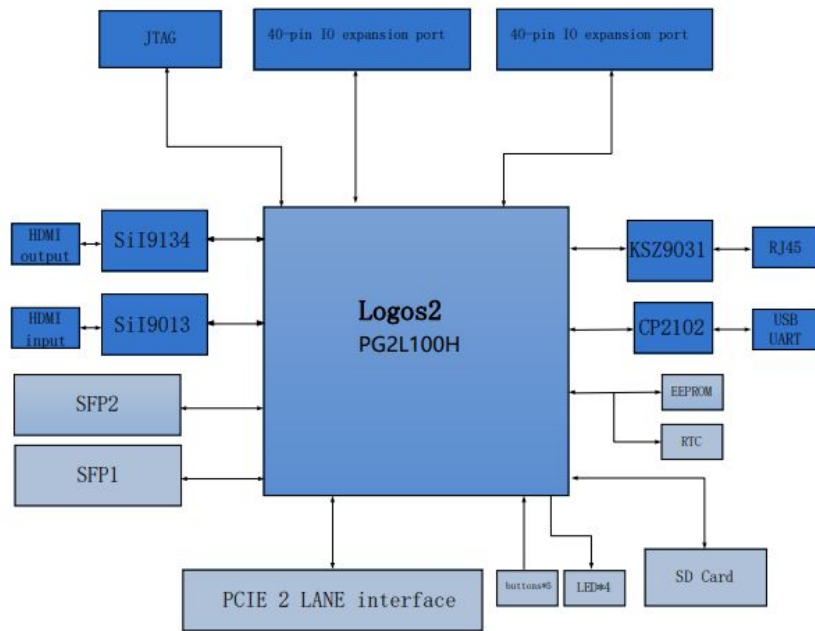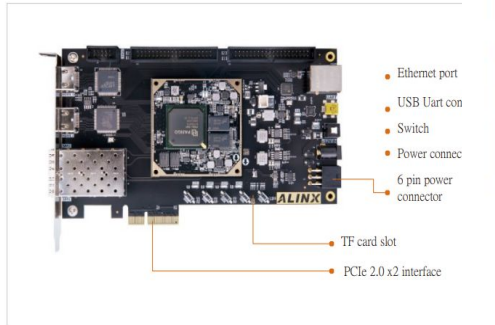
AXP100 development board
(Alinx, Logos-2 chip PG2L100H - 6IFBG676)

AXP100

Logos-2 FPGA development platform

Product parameters

- Based on PG2L100H -6IFBG676 FPGA
- 1GB DDR3, 32bit; 64MB QSPI FLASH
- x2 SFP Optical fiber interface, up to 6.6Gbps
- PCIe 2.0 x2, single channel up to 5Gbps
- 1 channel 10 / 100 / 1000M Ethernet, EEPROM 24LC04

- HDMI input & output interface, support 1080P@60Hz
- Integrated USB UART, JTAG, 40 -pin expansion port, TF card slot and other common interfaces
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB
- Provides rich Demo source code and supporting tutorials, making it easier to get started
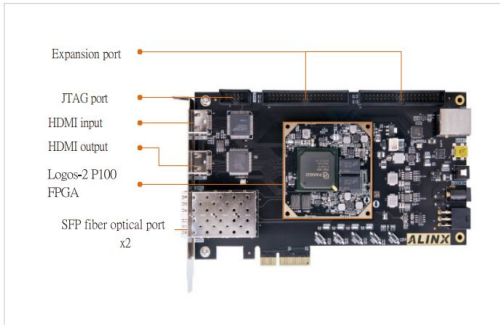

Expansion port
JTAG port
HDMI input
HDMI output
Logos-2 P100 FPGA
SFP fiber optical port x2

Ethernet port
USB Uart con
Switch
Power connec
6 pin power connector
TF card slot
PCIe 2.0 x2 interface

Comparison of AXP100 vs ASP390 boards

FPGA	TITAN-2 AXP390 (Alinx)	LOGOS-2 AXP100 (Alinx)
Equivalent LUT4	365400	99900
Flip-Flops (units)	487200	133200
Block RAM (kBits)	17280	5580
PLL / GPLL+PPLL	10 + 10	6+6
Expand IO	276	190
Differential pars	130	88
PCI-Express	PCIe 3.0	PCIe 2.0
HSST (transceivers)	8x 13,125 Gbps	8x 6,6 Gbps
Price	~1000$	~600$

Conclusions

- We are currently working on the concept of design of the L1 concentrator
- A group from Tomsk joined to the work on the L2 hub. I hope in the next few weeks we will develop a plan for further work on L2
- At the moment, it is impossible to say definitely which electronics components we will use, that means there is no certainty in the timing and price.

backup

Titan –2

Resource name		PG2T390H
CLM	LUT6	243600
	logical unit	389760
	FF	487200
	Distributed ram (Kb)	4712
DRM (36Kbits/ pc)		480
APM(units)		840
PLLs	GPLLs	10
	PPLLs	10
ADC (dual core)	Dedicated analog channel (differential input pair)	1
	Multiplexed analog channels (differential input pair)	11
SERDES LANE [1]		16
PCIE GEN2×8 CORE		1

PANGO
PG2T390H
6IFFBG900
USNSC2112
CHR88-A R1ES0-02
FACF7D0E

Logos –2

Resource name		PG2L25H	PG2L50H	PG2L100H
CLM	LUT6	17800	33400	66600
	Equivalent LUT4	26700	50100	99900
	FF	35600	66800	133200
	Distributed ram (Kb)	343	687	1273
DRM (36Kbits/ pc)		55	85	155
APM(units)		80	120	240
PLLs	GPLLs	3	5	6
	PPLLs	3	5	6
ADC (dual core)	Dedicated analog channel (differential input pair)	1	1	1
	Multiplexed analog channels (differential input pair)	11	16	16
SERDES LANE [1]		4	4	8
PCIE GEN2×4 CORE		1	1	1