VI SPD COLLABORATION MEETING
Oct 23-27, 2023
SAMARA

Development of an ASIC for Straw and MicroMegaS detectors of SPD NICA

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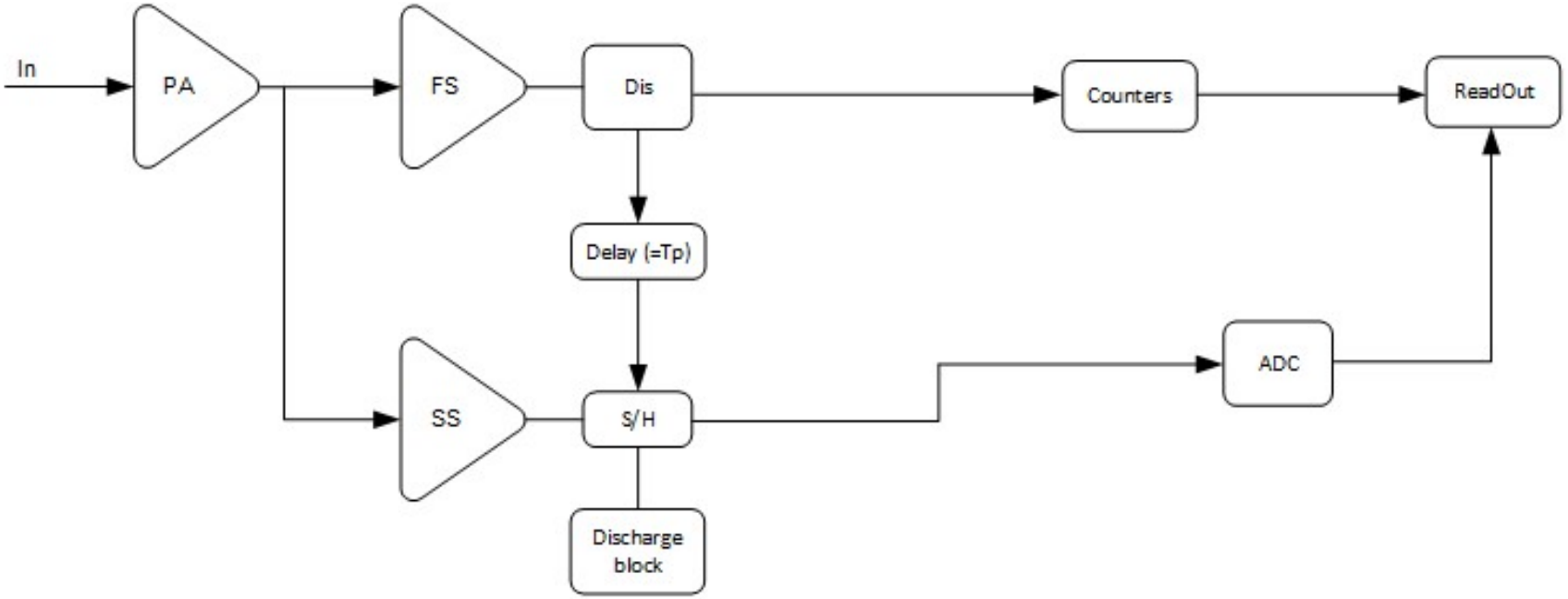
AST-SPD main specification

Detector parameters	
Negative input charge, fC	1000
Detector channel capacitance, pF	20÷100
Loading per channel, kHz	up to 200
Working mode	triggerless
Common chip parameters	
Technology	CMOS, 180 nm
Number of channels	32
Supply voltage, V	1.8
Power dissipation, mW/ch	10
Fast shaper, time channel	
Shaping time, ns	6÷10
Time channel resolution, ns	1
ENC (r.m.s.), e @ Cd=60pF	<1000
Slow shaper, amplitude channel	
Shaping time, ns	75/150/250
Shaper order	4
Gain, mV/fC	1/3/6/9
ENC (r.m.s.), e @ Cd=60pF	<1000
ADC, bit	10

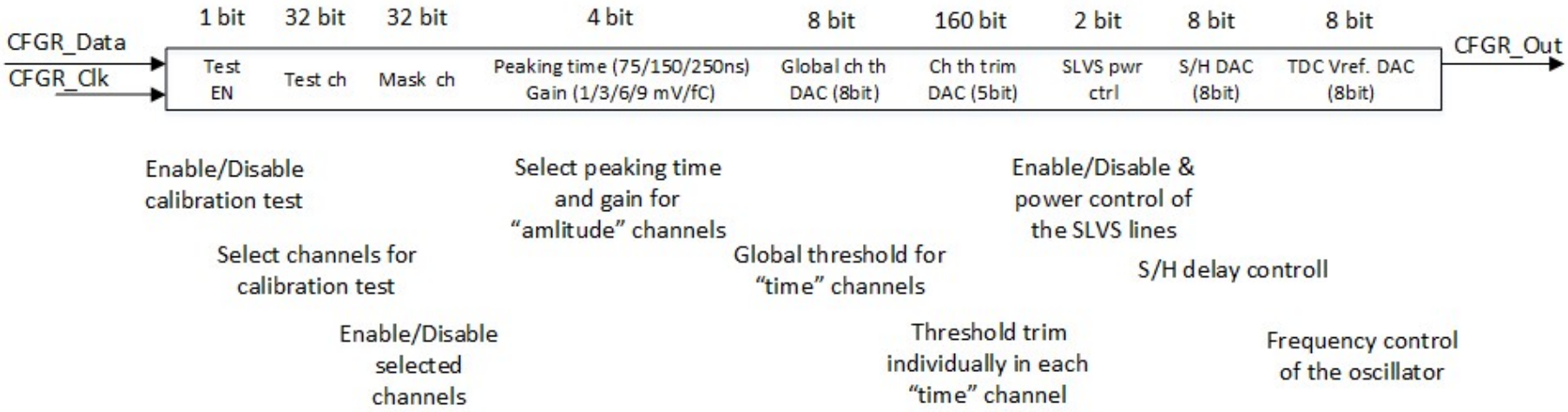
APD-SPD channel architecture



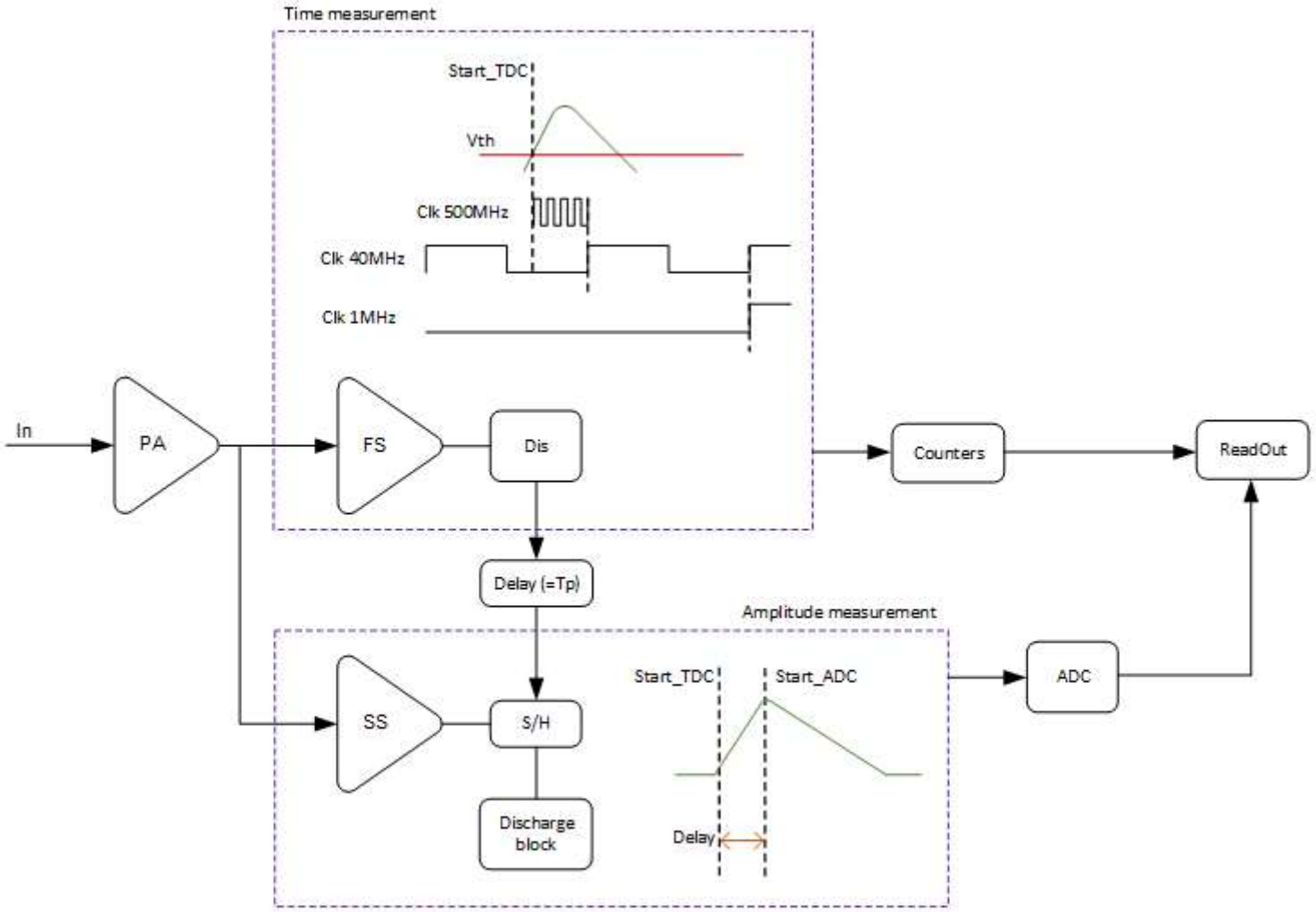
CFGR

Test ch EN	Test ch	Mask ch	Peaking time (75/150/250ns) Gain (1/3/6/9 mV/fC)	Global ch th DAC (8bit)	Ch th trim DAC (5bit)	SLVS pwr ctrl	S/H DAC (8bit)	TDC Vref. DAC (8bit)

Configuration register



TDC @ ADC



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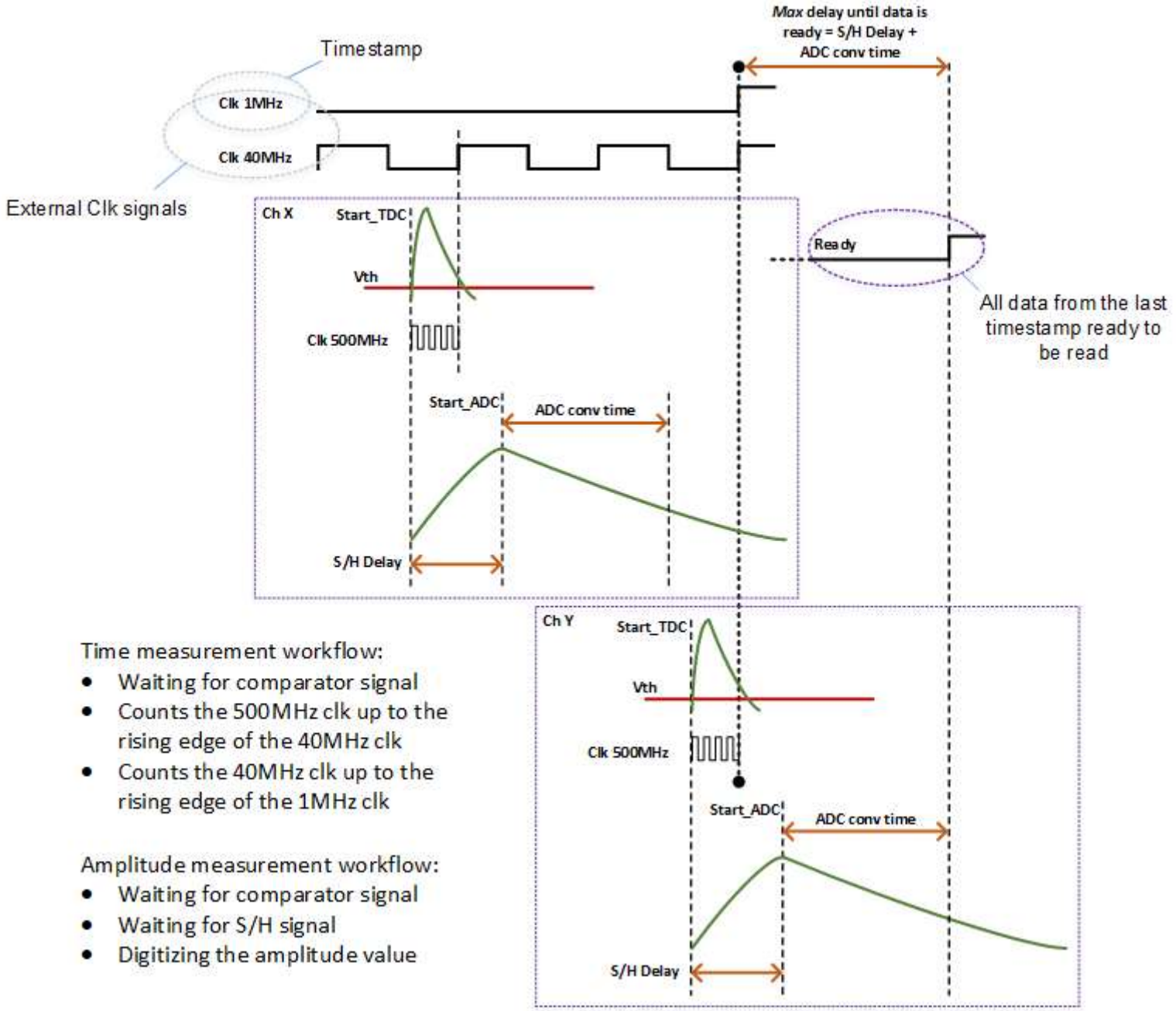
TDC @ ADC details



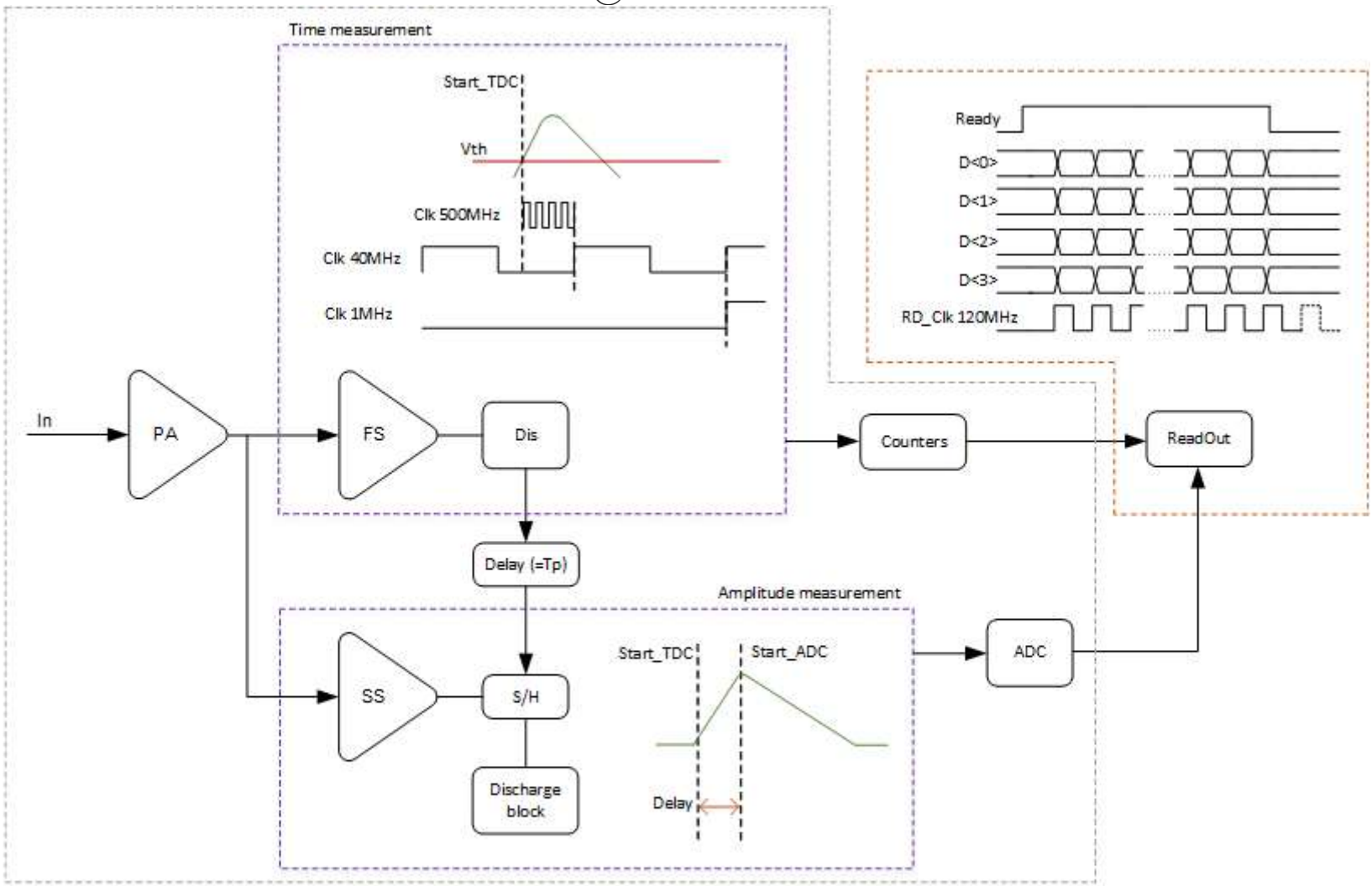
Time measurement workflow:

- Waiting for comparator signal
- Counts the 500MHz clk up to the rising edge of the 40MHz clk
- Counts the 40MHz clk up to the rising edge of the 1MHz clk

Amplitude measurement workflow:

- Waiting for comparator signal
- Waiting for S/H signal
- Digitizing the amplitude value

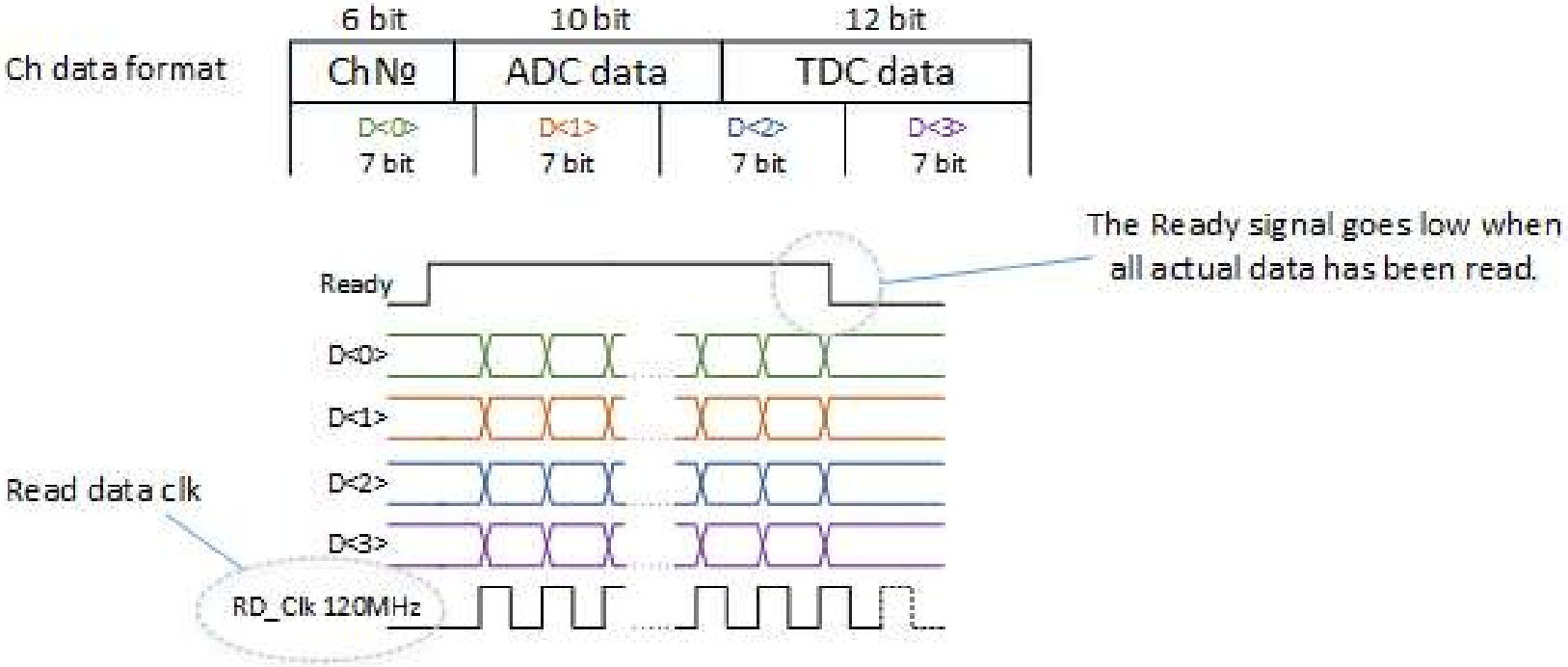
TDC @ ADC readout



CFGR

Test ch EN	Test ch	Mask ch	Peaking time (75/150/250ns) Gain (1/3/6/9 mV/fC)	Global ch th DAC (8bit)	Ch th trimm DAC (5bit)	SLVS pwr ctrl	S/H DAC (8bit)	TDC Vref. DAC (8bit)

AST-SPD data format



Pin Assignment/Function

Pin name	Number of pins	Description&Comments
Analog pins		
Inputs		
In	32	Analog input, ESD
Test channel		
In_test	1	Test input, ESD
Out_fs	2	Differential output of fast shaper
Out_ss	2	Differential output of slow shaper
Out_S/H	2	Differential output of S/H
Calibration		
vdc_cal	1	Calibration voltage
Digital pins		
Reset		
RS	1	Set to default state (reset data register, current trigger states), 1.8V CMOS
Configuration register		
CFGR_Data	1	Configuration register input, 1.8V CMOS
CFGR_Out	1	Configuration register output, 1.8V CMOS
CFGR_Clk	1	Configuration Register clock, 1.8V CMOS
CFGR_Rst	1	Configuration register reset, 1.8V CMOS
Data output		
Ready	2	Data output request, SLVS
Data_Out<1:4>	8	Data output, four buses, SLVS
External clock signals		
Clk_1MGz	2	Time stamp, SLVS
Clk_40MGz	2	TDC counter, SLVS

Pin Assignment/Function

Pin name	Number of pins	Description&Comments
RD_Clk	2	Read data, SLVS
OR circuit		
OR	2	OR output, SLVS
Calibration		
tinj	2	Charge injection into selected channels, SLVS
Analog power supplies		
VDD1, VSS1	12	Power and ground CSP, FS, SS, six through buses
VDD2, VSS2	8	Power and ground Dis, four through buses
VDD3, VSS3	8	Power and ground S/H, ADC, four through buses
VRP	2	ADC reference voltage, 1.4 V, two through bus
VCM	2	ADC reference voltage, 0.9 V, two through bus
VRN	2	ADC reference voltage, 0.4 V, two through bus
Digital power supplies		
VDD4, VSS4	8	Power supply for digital part, four through buses
VDD5, VSS5	8	Power supply for SLVS receivers and transmitters, four through buses
VDD6, VSS6	8	ESD power supply, four through buses
VOSC	2	TDC reference voltage, (0.9÷1.6) V, through bus
Total	123	

Configuration register

Description&Comments	**Number of bits**
Global bits (defaults are 0)	
Shaping time: 75, 150, 250 ns	2
Gain: 1, 3, 6, 9 mV/fC	2
Channels threshold DAC	8
S/H DAC	8
TDC reference voltage DAC	8
SLVS power control	2
Channel bits (defaults are 0)	
Channel threshold trimming DAC	5
Channels calibration	32
Channels mask	32
Test channel enable	1

Development stages of the AST-SPD chip

1) AST-SPD topology development
Terms of work: from 01/10/2023 to 30/06/2024

2) Manufacturing of wafers with AST-SPD chips of the first iteration
Terms of work: 01/01/2024 to 31/12/2024