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Design of the prototype ASIC for BM@N STS

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Introduction
The presented design describes a prototype of an application specific integrated circuit (ASIC) for use with silicon microstrip sensors of the BM@N (Baryonic Matter at Nuclotron) facility [1] at the upcoming NICA collider.
The structural diagram, developed layout, and main electrical parameters of the ASIC are presented.
The prototype ASIC includes all the main complex functional blocks of the future full-scale version of the ASIC. For the fabrication of the chip a CMOS process of 180 nm node was chosen.
ASIC structure
The particles passing through the microstrip sensors create a charge on the strip by knocking out electrons or holes. The task of the chip is to amplify the signal, shape it, perform signal amplitude sampling and digitize it for all strips, and finally transmit this information outside via the SLVS interface. Figure 1 shows a simplified structural diagram of the presented microchip.

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Fig. 1. Block diagram of the prototype ASIC
The prototype ASIC has 8 working + 2 additional outermost (test) analog channels for readout signals from microstrip sensors. Each channel consists of such blocks as a low-noise charge-sensitive amplifier (CSA), a time-variable amplifier-shaper with conversion times of 200-300-500 ns (SH), a polarity switching key (SW). Blocks of a comparator (CMP) and a peak detector (PD) define the presence of a channel signal and retrieve the channel peak amplitude.
The threshold value for CMP is set by a 4-bit digital-to-analog converter (DAC). The duration of the CMP signal is determined by the time above the threshold. PD is supplemented with an auxiliary comparator circuit that provides signal type of peak find (PF) and reset the charge of the storage capacitor by Reset_PD signal.
The chip also includes an input calibration system based on 8-bit DAC. Calibration is performed by a digital slow control block, and data is written to it via the SPI interface.
ASIC is a prototype for its future full-scale 128-channel version. The close functional analog of this prototype chip is STS XYTER [2,3]. Since the maximum signal frequency is 100 kHz, one 8-bit ADC is used to successively process all channels.
Figure 2 shows the layout of the prototype ASIC. The main blocks are depicted on it. It has geometric dimensions of 5000 μm * 5000 μm. The contact pad frame contains 158 pads.

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Fig. 2 Placement of blocks on the ASIC layout
The layout is planned to be used in an unpackaged version In addition to the signal path, the microchip includes test structures for optimizing subsequent ASIC launches. The digital block was also designed with the ability to upscale it to a 128-channel chip version. The main characteristics of the chip are given in table 1.
Table 1

- Number of analog channels –8 + 2 (outermost test channels);
- Input signal range –3.6 fC (1 mip –the most typical signal) to 108 fC (30 mips);
- Polarity –selectable (positive or negative);
- ENC –8 + 2 < 1500 el at Cdet up to 30 pF;

- Shaper peaking time –programmable: 200, 300 or 500 ns;
- Channel signal rate –< 1 кГц;
- ADC –10 bit at 40 ns conversion time);
- Power consumption –100 mW (in total) = 70 mW (10x analog chains + ADC) + 20 mW (digital part) + 10 mW (test blocks);
- Control interface –SPI;
- Additional test blocks –SLVS TX + RX, PLL, ADC. **Conclusion** In the current year a prototype of an application specific integrated circuit for silicon microstrip sensors of the BM@N installation was designed and submitted for manufacturing. The chosen technology for fabrication of the chips is the CMOS process of 180 nm node. The schematic and layout designs were done for all main complex functional units of the prototype ASIC, featured by 8 (+2 test) channels. The logical part of the project and operating protocols were developed with the ability to upscale the chip to a future full-scale version, which should have 128 (+2 test) analog channels.

Reference

[1]: Materials of the BM@N experiment website: https://bmn.jinr.ru/
[2]: K. Kasinski, W. Zubrzycka, Test systems of the STS-XYTER2 ASIC: From wafer-level to in-system verification», Proceedings of SPIE –International Society for Optical Engineering 2016 (Vol. 10031), doi: 10.1117/12.2249137
[3]: R. Kleczek, Analog front-end design of the STS/MUCH-XYTER2 - full size prototype ASIC for the CBM experiment, J. Instrum. 12 (1) (2017) C01053, doi:10.1088/1748-0221/12/01/C01053

Primary author: YAMALIEV, Salavat (Laboratory for Designing Specialized Integrated Circuits)

Co-authors: Dr DEMENTYEV, Dmitry (JINR LHEP); Mr NORMANOV, Dmitry (MEphI); Dr ATKIN, Eduard (MEphI); SHITENKOV, M.O.; Dr BUTUZOV, Vladimir (MEphI); Mr YUROVSKY, Vladimir (MEphI/SINP MSU); Dr BOCHAROV, Yuri (MEphI)

Presenter: YAMALIEV, Salavat (Laboratory for Designing Specialized Integrated Circuits)

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