



Trigger system of BM@N experiment

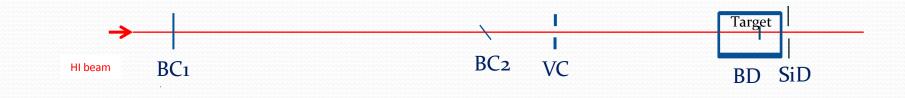
D.Bogoslovski, V.Rogov, <u>S.Sergeev,</u> V.Yurevich

# Outline

#### • Requirements

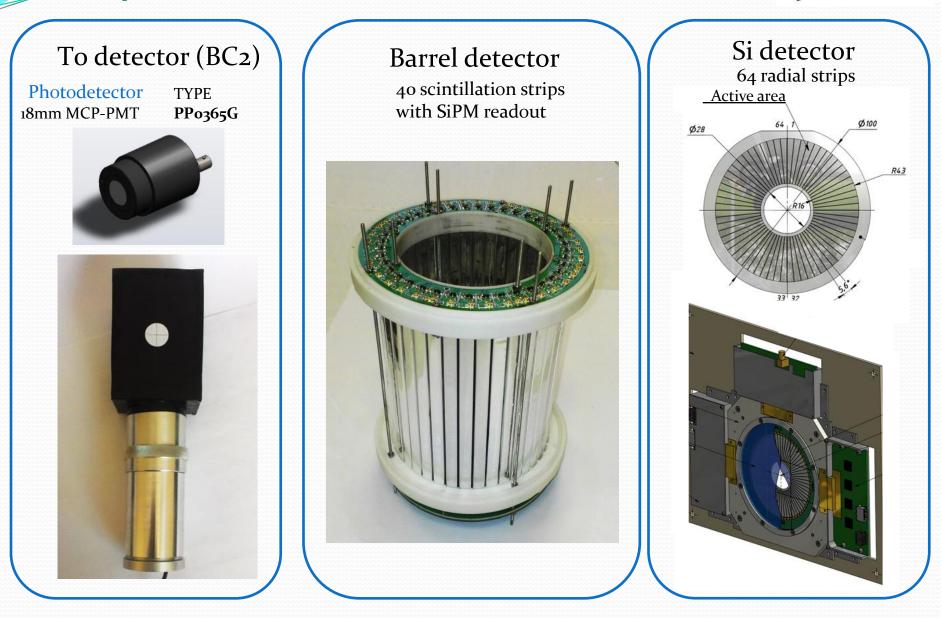
- Beam line + equipment
- Architecture choice
- Hardware
  - Architecture
  - Motherboard and Mezzanine cards
- Software
  - Architecture
  - Control and monitoring





Scintillation Detector	Photodetector	Scintillator	Operation in magnetic field
BC1	XP2020	Plastic scintillator D150×3 mm	No
BC2(To)	MCP-PMT PP2365E	Plastic scintillator D20x0.8 mm Angle 45°	Yes
VC	XP2020	Plastic scintillator D100×10 mm hole D27 mm	Yes
BD	SiPMs (Sensl) 6 x 6 mm	BC-418 plast. scintillator 150×7×7 mm 40 units	Yes
SiD	64 radial strips	Silicon D86xo.3 mm hole D32 mm	Yes

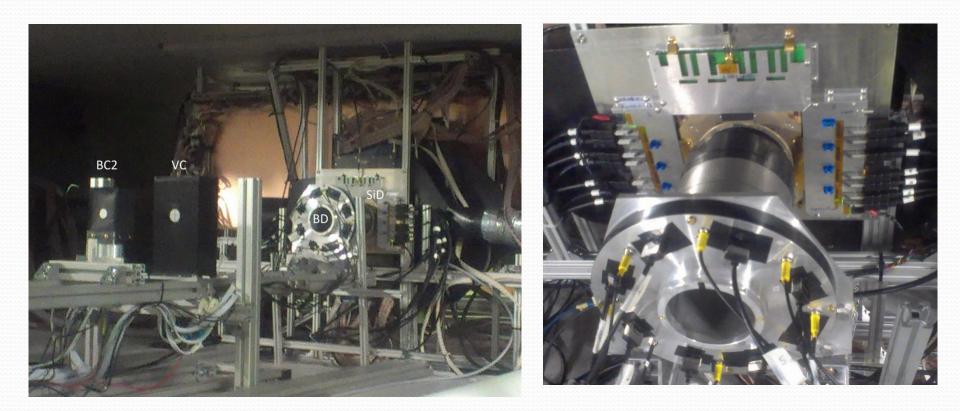
## Requirements->Detectors |



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#### Requirements -> Detectors II





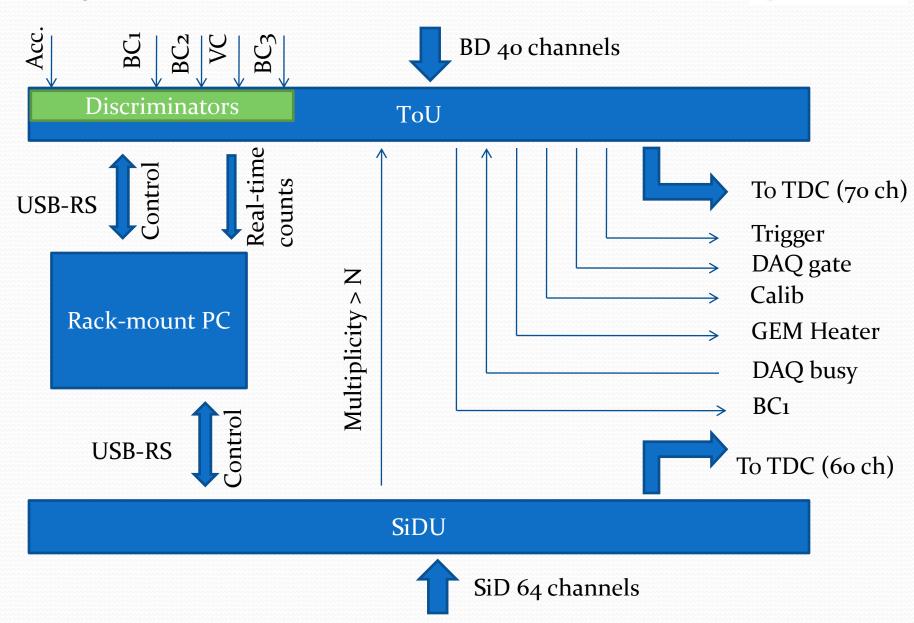
#### **Requirements** I

- We have to use short cables
- The trigger units should be installed in the restricted access area
- Adjustments and control should be done remotely
- Trigger system should generate a trigger signal based on particle multiplicity in the Barrel Detector and Si detector
- We should use two trigger units ToU and SiDU connected by LVDS
- The rack contains NIM crate with extra equipment
- The control PC is a rack-mount industrial PC located in the trigger system rack

### Requirements II

- All input signals should be sent to TDC to get event timing
- Trigger unit should generate gate and trigger signals to subsystems
  - Spill gate
  - LED calibration gate
  - LED flash signal
  - GEM Heating signal
- Trigger unit should generate beam/calibration event flag signal to DAQ
- Trigger system contains PMT HV power supply (by HVSys, Dubna) and SiPMT BV power supply (selfmaid)

#### Requirement->Architecture



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# **Requirements->realization**

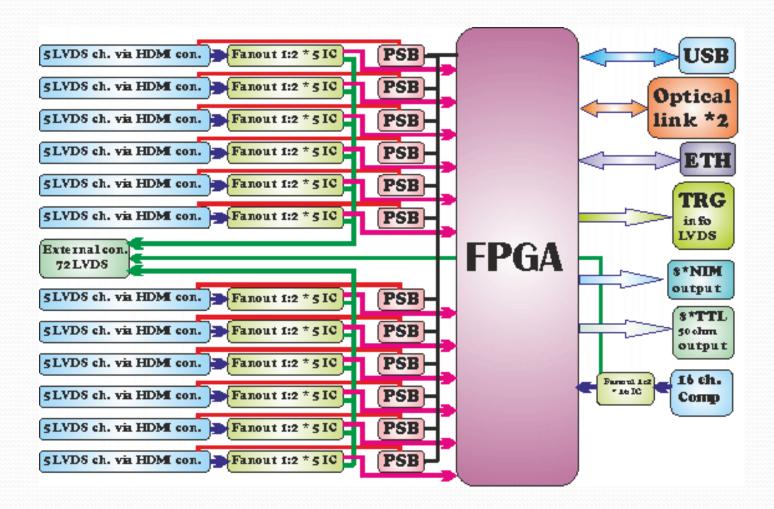
- Trigger system rack located near the magnet
- No magnetic field influence observed
- No radiation damage or SEU observed



### Hardware I

- Trigger unit consists of
  - Mother board containing
    - FPGA Altera Cyclon5
    - Low jitter signal splitters
    - USB, Ethernet and Optical link interfaces
  - Mezzanine boards
    - 4 Input boards with discriminators, 4 channels each
    - 4 Output boards NIM signal, 4 channels or
    - 4 Output boards 50 Ohm TTL , 4 channels
    - 12 LV power supplies, +8V adjustable ,+8V adjustable, -7.2V fixed
    - LVDS output buffer

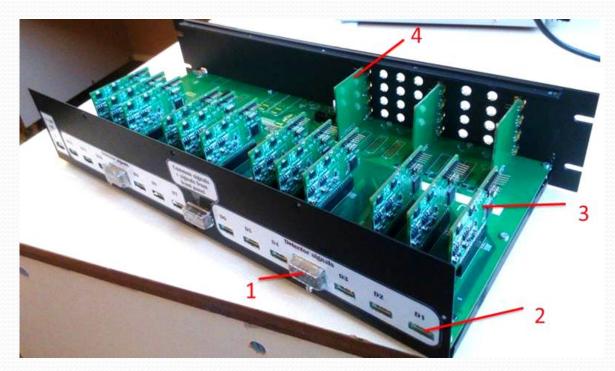
#### Hardware II





#### Hardware III



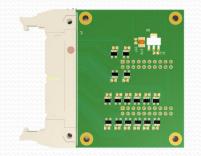




Input module



Output NIM module



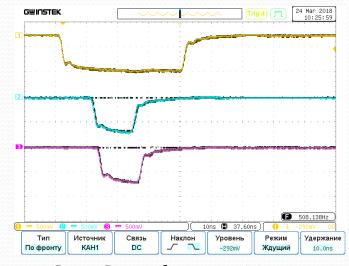
Output LVDS module



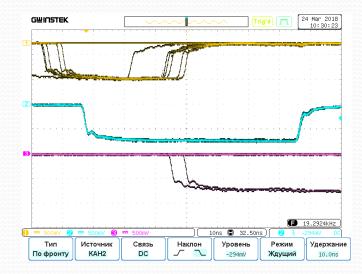
Output 50 Ohm TTL module

### Hardware IV -> features

- ToU Logics contains up to 12 adjustable delay lines and shapers
- Delay and shaper settings could be adjusted with ~0.7 ns step
- ToU contains 4 multiplexers providing connection to the logics key points for simple trigger adjustment



BC1, BC2 and Beam\_Trigger



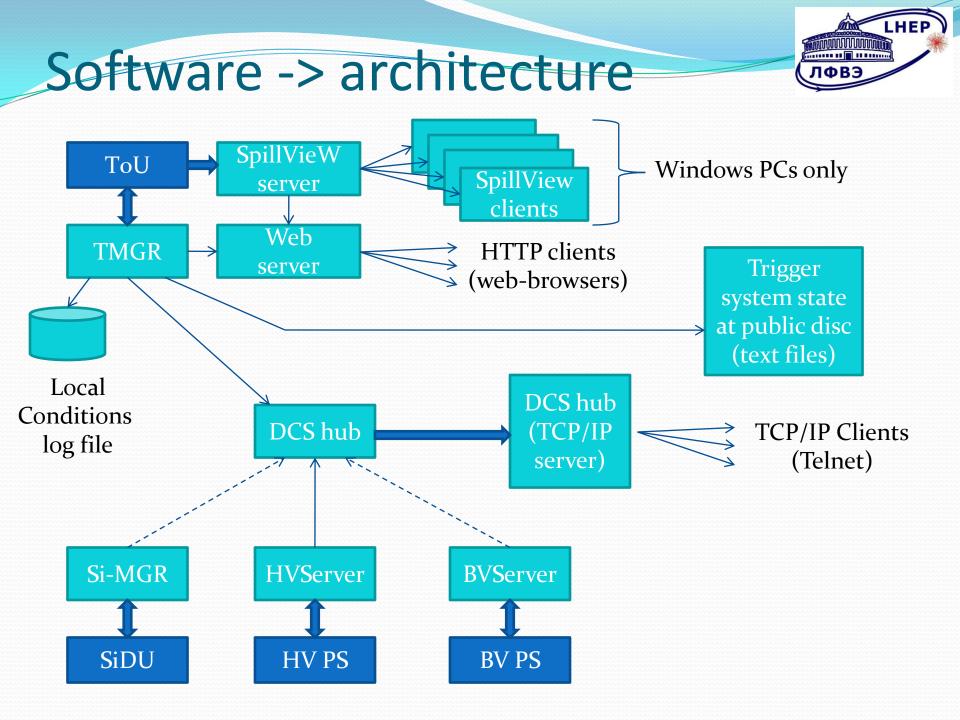
BC1, SiD and DAQ\_Trigger

#### Hardware -> Summary

- Developed in 2015
- Used in experiments BM@N and SRC
- No electronics failures observed
- Mechanically damaged Molex connectors -> replaced

# Software -> requirements

- Software should allow to the shifters to select a trigger type in a simple way
- ToU hardware has > 100 controls => software should have extended GUI
- The spill data information should be presented to the BM@N shifters and to the accelerator shifters => client/server architecture
- The actual trigger system state should be sent to the MN@N DCS



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@00#0E25\$07000605

Configuration

Shaper

74 🕃 75.7ns

XXXXXX

N(SID)> 3 👸

•

72 🕃 65.2ns 20780

Sarrel Silicon detector Mutiplicity1

- - -

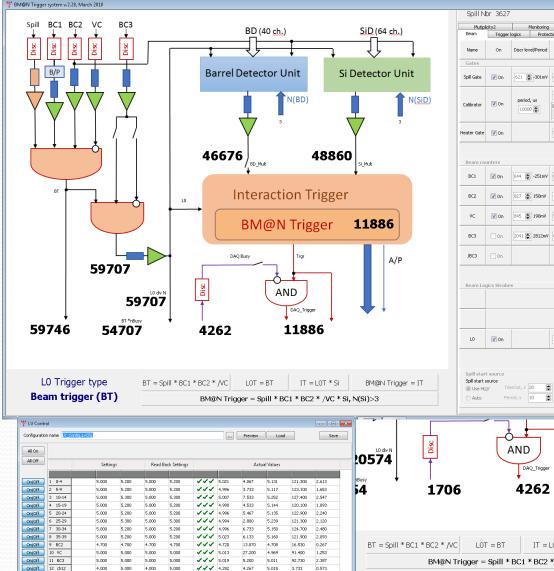
Exit

Multiplexers

Count

15961

### Software -> ToU manager



	Spill N	or 3627				0	00#0E <u>2</u> 5\$	07000605		Exit						
)	Mutipli Beam	city2 Trigger		onitoring Protec		Cor Barrel	nfiguration Si	icon detei		plexers Mutiplicity1						
<u>,</u>	Name	On	Discr leve	l/Period	Dela	y	Shaper/	Length	Count							
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nit	Spill Gate	🗸 On	621 🖨	-301mV	650 8	s ms	3000	ns 🕈	3627							
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	Heater Gate	🔽 On			5200 8	🖨 ms	5000	🖨 ms								22
												Spill N	br 3613			
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	BC2	💟 Ön	827 🕃	150mV	42 💭 41	.2ns	0	15.8ns	63867			Name	On	Discr	Del	lay
	VC	🗸 On	845	190mV	5 🐑 12	2.0ns	67 😧	70.5ns	25526		E	BD_Mult	🗌 On		23 💭 :	28.7r
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BM@N T	rigger =	Spill *	BC1 *	BC2	* /VC	* Si,	N(Si):	>3								

# Software -> ToU manager II

Spill Nbr 3624         @00#0E2\$407000605         Exit           Mutplicity2         Monitoring         Configuration         Multiplexers           Beam         Trigger logics         Protection         Barrel Silicon detector         Multiplexers           3806         4388         4118         3738         6685         4907         4263         4559           4956         3965         5575         5539         6347         6053         4552         6392           6664         9285         12892         6068         20247         23862         34664         29942           15272         42327         39325         32317         34702         41251         28744         25493           30188         19320         35950         17142         16903         9739         7962         22368           Channel #         X00000X								
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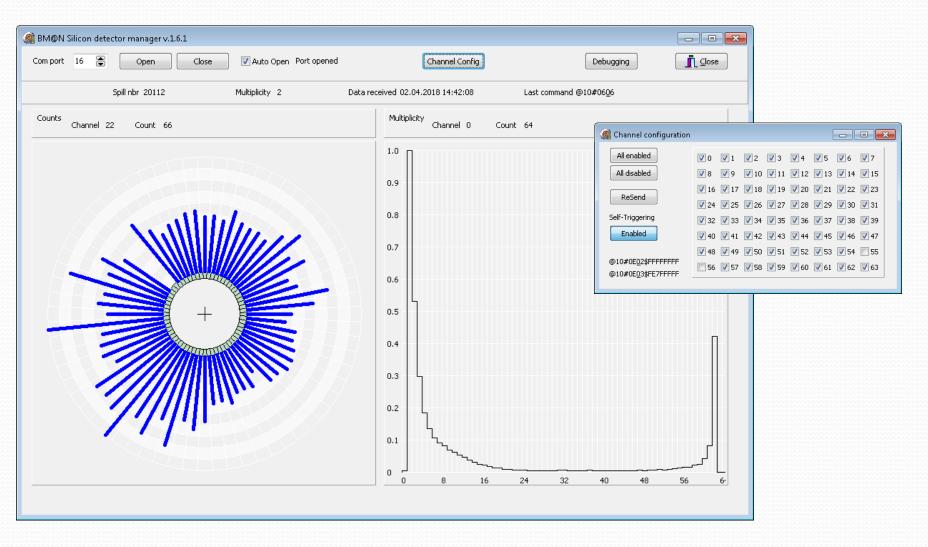
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				_
	Beam i	ntensity		
BC	21	166	5585	
BC1_	in	167	7816	
E	3T	98	432	
	Beam f	ocusing		
BT/BC	21	0.5	908	
B	eam ba	ckground		
VC/BC	21	0.2	417	
Tı	rigger n	nonitoring		
MinBia	as	98	433	
No interactio	on		0	
Tr	gr	19	643	
MinBias/E	вт		1	
noInteract/E	вт		0	
Trgr/E	вт	0.1	.995	
Trgr_Bsy/Trg	gr		1	
BT Bsy/E	зт	0.8	647	

Spill Nbr 3631		@00#0E25\$07000605							
leam Trigger logics	Protection	Barrel Silicon detector	Mutiplicity1						
Mutiplicity2	Monitoring	Configuration	Multiplexers						
MUX1									
0 BC1_inDelO5		🔘 8 BT							
1 BC2_inDelO5		9 L0_inDelOS							
2 VC_inDelO5		10 BD_Mult_inDelOS							
3 BC3_inDelOS		11 SiD_Mult_inDelOS							
4 BC1		🗇 12 Min_Bias							
5 BC2		🔘 13 LO							
🔘 6 VC		14 BD_Mult							
7 BC3		15 SiD_Mult							
MUX2									
© 0 BC1_inDelOS		🗇 8 BT							
1 BC2_inDelOS		9 L0_inDelOS							
2 VC_inDelOS		10 BD_Mult_inDelOS							
③ 3 BC3_inDelOS		11 SID_Mult_inDelOS							
4 BC1		12 No_Inter							
🔘 5 BC2		🔘 13 LO							
6 VC     1		14 BD_Mult							
🔘 7 BC3		🔘 15 SiD_Mult							
MUX3									
0 BT		8 outO5_Pul1							
1 L0_inDelOS		Ø DAQ_Busy							
🔿 2 LO		10 Busy							
3 Min_Bias		11 DAQ_Trigger							
4 No_Inter		12 Trigger_inProt							
🗇 5 BD_Mult		🔘 13 Prot							
🔘 6 SiD_Mult		14 Trigger_Abort							
7 Pul1_zdc_led		15 Evnt_Good							
MUX4									
🖱 0 BT		8 outOS_Pul1							
🔿 1 L0_inDelO5		Ø DAQ_Busy							
🖱 2 LO		10 Busy							
🔿 3 Min_Bias		11 DAQ_Trigger							
0 4 No_Inter		12 Trigger_inProt							
🖱 5 BD_Mult		🔘 13 Prot							
🖱 6 SiD_Mult		14 Trigger_Abort							
7 BT_Busy		① 15 Evnt_Good							

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#### Software -> SiDU manager



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#### Software->HV & BV managers

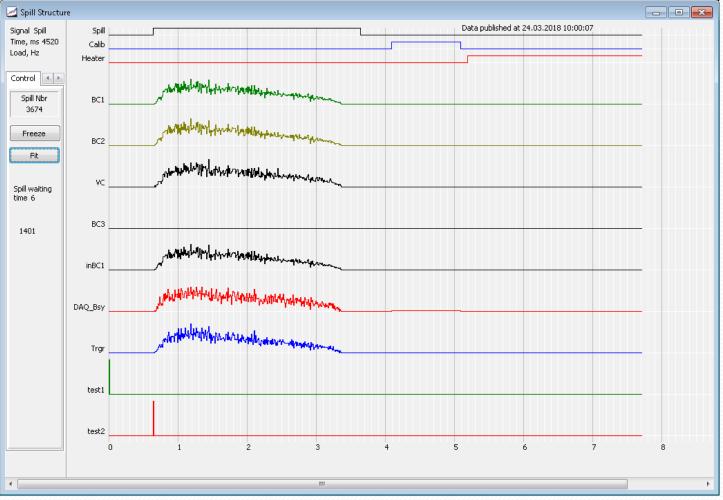
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HV_System	ns SM32_22(	) Control v1.3									<b>—</b>		
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Control Care		nager Service		onnguration nie name Conngz.	INCOMING				🗨 Load C	onfig Save Co	nrig		
Control Conr	iguration mai												
1 BC1	On/Off	Uset, V 1600 💌	Status On	Uout, V 1601 Iout, uA 107	9 Ustby, V 328	RampUp 10	00 🗭 F	RampDn 100 💌 Pro	ot.delay(ms) 0.0 💌 1	max, uA 2998	-		
2 BC2	On/Off	Uset, V 1575 💌	Status On	Uout, V 1575 Iout, uA 85	Ustby, V 326	RampUp 10		SIPM_LV_PS_x16_Manage	r, v8.1.1. Bogoslovskij Dmitrij. 1 U set [0 30,18 v		Li sentral (0, -2	0.10.1	
3 VC	On/Off	Uset, V 1450 💌	Status On	Uout, V 1449 Iout, uA 252	Ustby, V 324	RampUp 10		Unit_1 Ch1 57671 •	O set [0 30, 18 ♥		U control [0 3	87%	
4	On/Off	Uset, V 325 💌	Status Off	Uout, V 6 Iout, uA 0	Ustby, V 325	RampUp 10		Ch2 57671 •	▶ Set 26.1	58 V 🔽 ON	26.524∨ 26.635∨	87%	0D0E
5	On/Off	Uset, V 327 💌	Status Off	Uout, V 0 Iout, uA 0	Ustby, V 327	RampUp 10		Ch4 57671		58 V 🔽 ON	26.405 🗸	87%	
6	On/Off	Uset, V 326	Status Off	Uout, V 0 Iout, uA 0	Ustby, V 326	RampUp 10		Ch5 57671 • Ch6 57671 •		58V 🔽 ON	26.429∨ 26.325∨	87% 87%	0D02
7	On/Off	Uset, V -1	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65		Ch7 57671 • Ch8 57671 •			26.341 ∨ 26.532 ∨	87% 87%	0CF7 0D0F
8	On/Off	Uset, V -1	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65		Ch9 57671 •		58 V V ON	26.357∨ 26.548∨	87% 87%	0CF9
9	On/Off	Uset, V -1	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65		Ch11 57671 •		58 V 🔽 ON	26.627∨ 26.849∨	88%	0D1B
10	On/Off	Uset, V -1	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65		Ch13 57671	Set 26.1	58 V V ON	26.786 🗸	88%	0D2F
11								Ch14 57671  Ch15 57671	Set 26.	58 V 🔽 ON	26.444∨ 26.706∨	87% 88%	0D04 0D25
	On/Off	Uset, V -1	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65		Ch16 57671  Broadcast U[116] set		Time	Run State	87% 6385 Tack 78 m	
12 BCX	On/Off	Uset, V -1 💌	Status Rpg Dn	Uout, V -1 Iout, uA -1	Ustby, V -1	RampUp 65	5535 💽	COM_Port cfg	Port_Status Port_BPS	09:58:33	_		
								\\_COM8 115200, n, 8, 1	C notActive 115200		*	Get	ADCval GetID Name: LV_PS.cfq
							l	-Transceive -ength12 CRC-32	Receive	RC-32 20 Len	gth	Los	ad Cfq Save Cfq
								T>1 WDA 0xE147 T>1 WDB 0xE147 T>1 WDC 0xE147 T>1 WDC 0xE147 T>1 WDD 0xE147	<ul> <li>R&gt;:0x01&gt;WDA \$</li> <li>R&gt;:0x01&gt;WDB \$</li> <li>R&gt;:0x01&gt;WDC \$</li> <li>R&gt;:0x01&gt;WDC \$</li> </ul>	0B 0xE147 0C 0xE147			aloq Load Cfq Dialoq Save Cfq telp Graph.
								T>1 WDE 0xE147 T>1 WDF 0xE147	E R>:0x01>WDE \$ R>:0x01>WDF \$			-	Clear
								Service S> Comm32dim.Bits=8 S> Comm32dim.StopBits= S> Comm32dim.CommPc S> Comm32dim.ReadInte S> Unit 1 detected	ort=\\.\COM8			Clea	1 ra* ar Send_String \$30 Send_Byte
												-	



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#### Software -> Web server



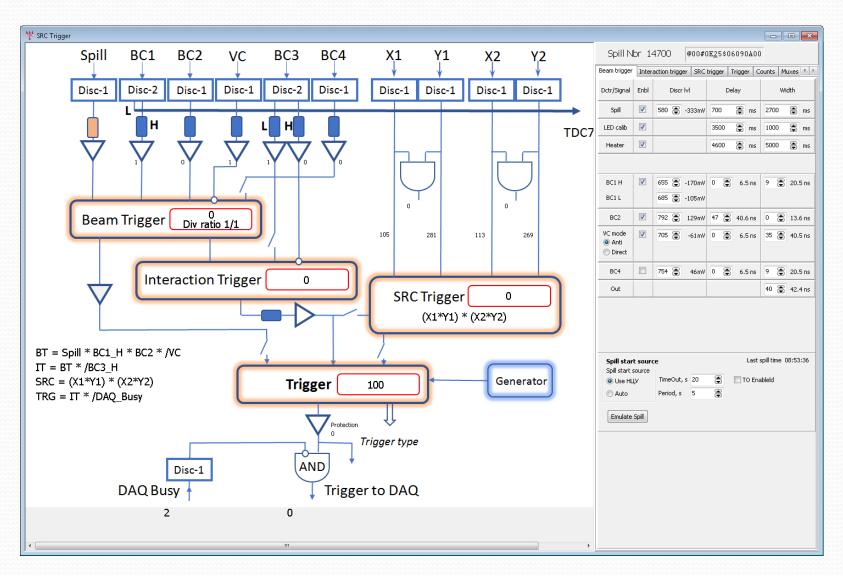
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C (10.93.118.246:80	80							0.00 \$
March 2019	B	M@	NT	RG	M	GR		
Beam intensity								
BC1	352513			Spill nbr. 427	3 24.03.2018	8 12:16:16		
BC2	221542							
VC	88102	Spill					24.03.2	2018 12:16:16
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VC/BC1	0.24992	1	A WALNEV HIM	and high providence	mystern .			
BT/BC1	0.58255	BC1			al allowed			
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Bd/Tr	8.16144	VC	^		an and			
Si/Tr	6.90804							
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XXX	0	BC3						
XXX			whenhow	had any hour hour				
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BC2	221542	test1						
VC	88102							
BT BD Mult	205357							
	236184	test2						
Si Mult	199912	0		2	3	4	5	6

# Conclusion

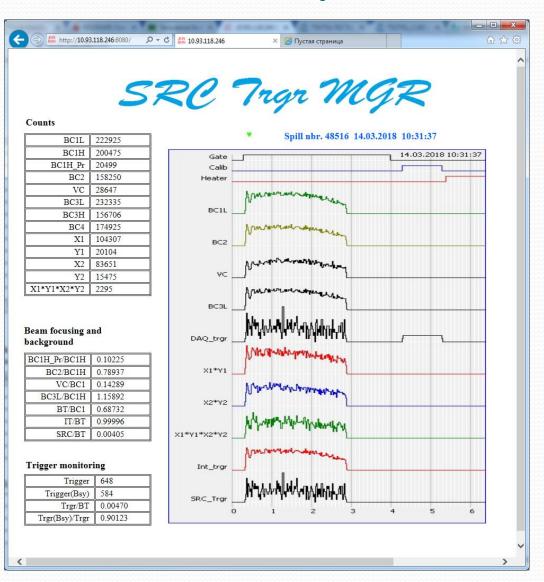
- Trigger system works since 2015. It provides comfortable and user-friendly GUI
- Five modules have been manufactured
- Used in two experiments BM@N and SRC
- No electronics failure observed. We met only "external" problems – bad 220V power and mechanical damage of a Molex TDC cable connector
- The system has been interfaced to the DCS system (no DCS commands accepted, the Trigger State transfer only)
- Almost all FPGA recourses have been used. Further ToU extension requires a motherboard redevelopment



#### Software -> SRC experiment



#### Software -> SRC experiment



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