Prototype chip development for STS: status and plans

on behalf of NRNU MEPhI ASIC Lab
E. Atkin
evatkin@mephi.ru

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Plan

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Introduction

Modern (quite complex) application specific integrated circuits (ASICs) for experiments such as BM@N require at least 3-4 prototyping stages, each including the chip design, using the CAD system, manufacturing of few tens chips and their lab tests

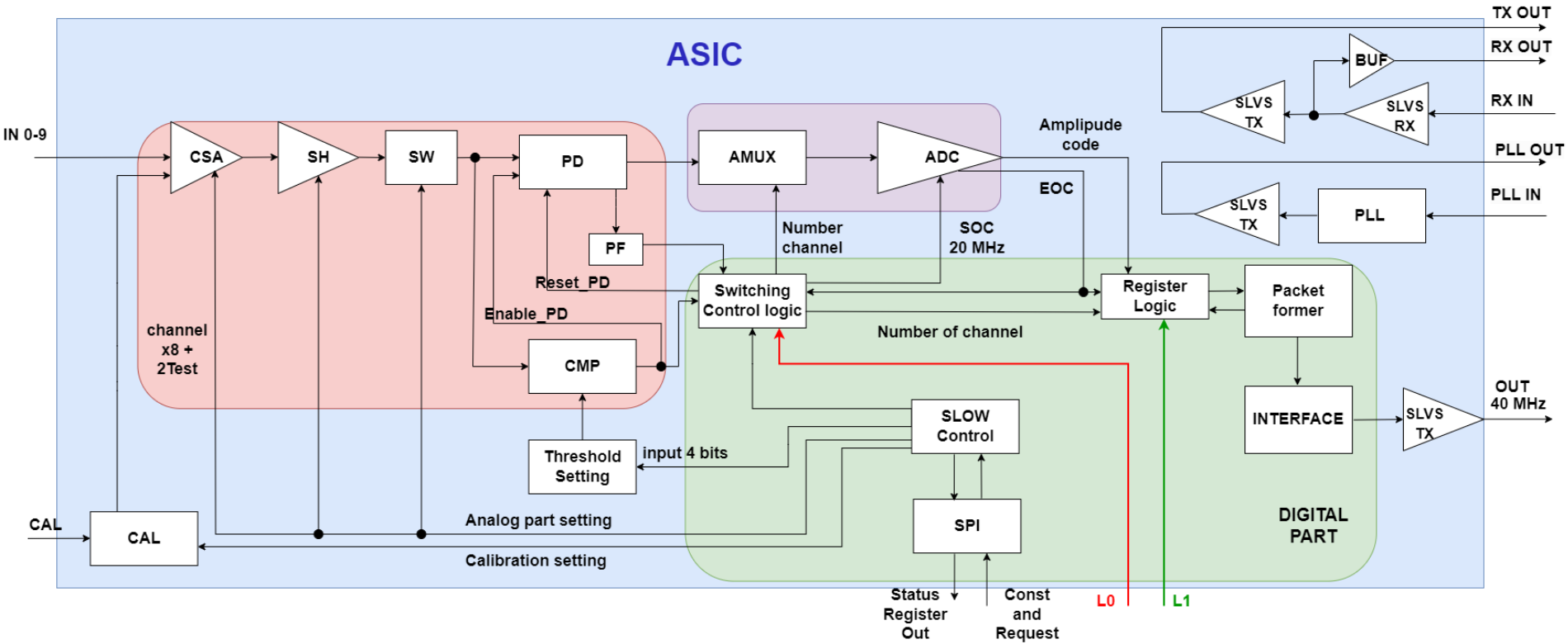
Here presented is the development of the 1st prototype version of an ASIC to be developed to read out signals of STS microstrip sensors.

To save money during the prototyping phases, the 1st prototype version has been aimed to develop a structural diagram, design all the basic building analog blocks, required for a future full-scale version of the ASIC, as well as to develop digital and interface parts

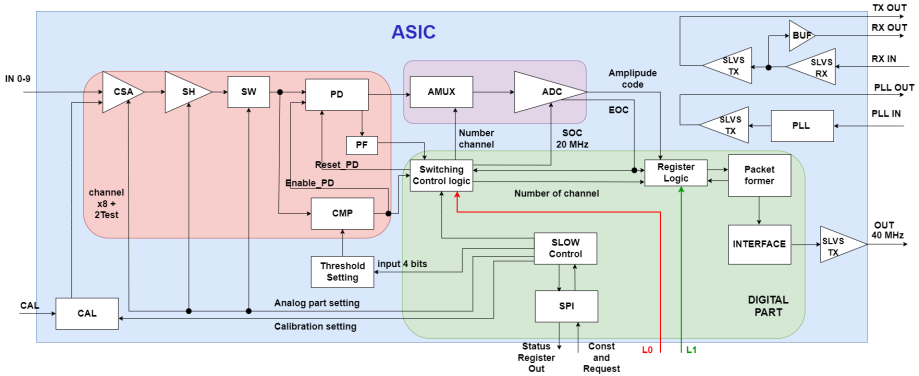
Key specifications of the 1st prototype

Parameter	Value
Number of analog channels	8 + 2 (outermost test channels)
Input signal range	3.6 fC (1 mip – the most typical signal) to 108 fC (30 mips)
Polarity	selectable (positive or negative)
ENC	< 1500 el at C_{det} up to 30 pF
Shaper peaking time	programmable: 200, 300 or 500 ns
Channel signal rate	< 1 кГц
ADC	10 bit at 40 ns conversion time
Power consumption	100 mW (in total) = 70 mW (10x analog chains + ADC) + 20 mW (digital part) + 10 mW (test blocks)
Control interface	SPI
Additional test blocks	SLVS TX + RX, PLL, ADC

Block diagram (simplified)



Structure and design team



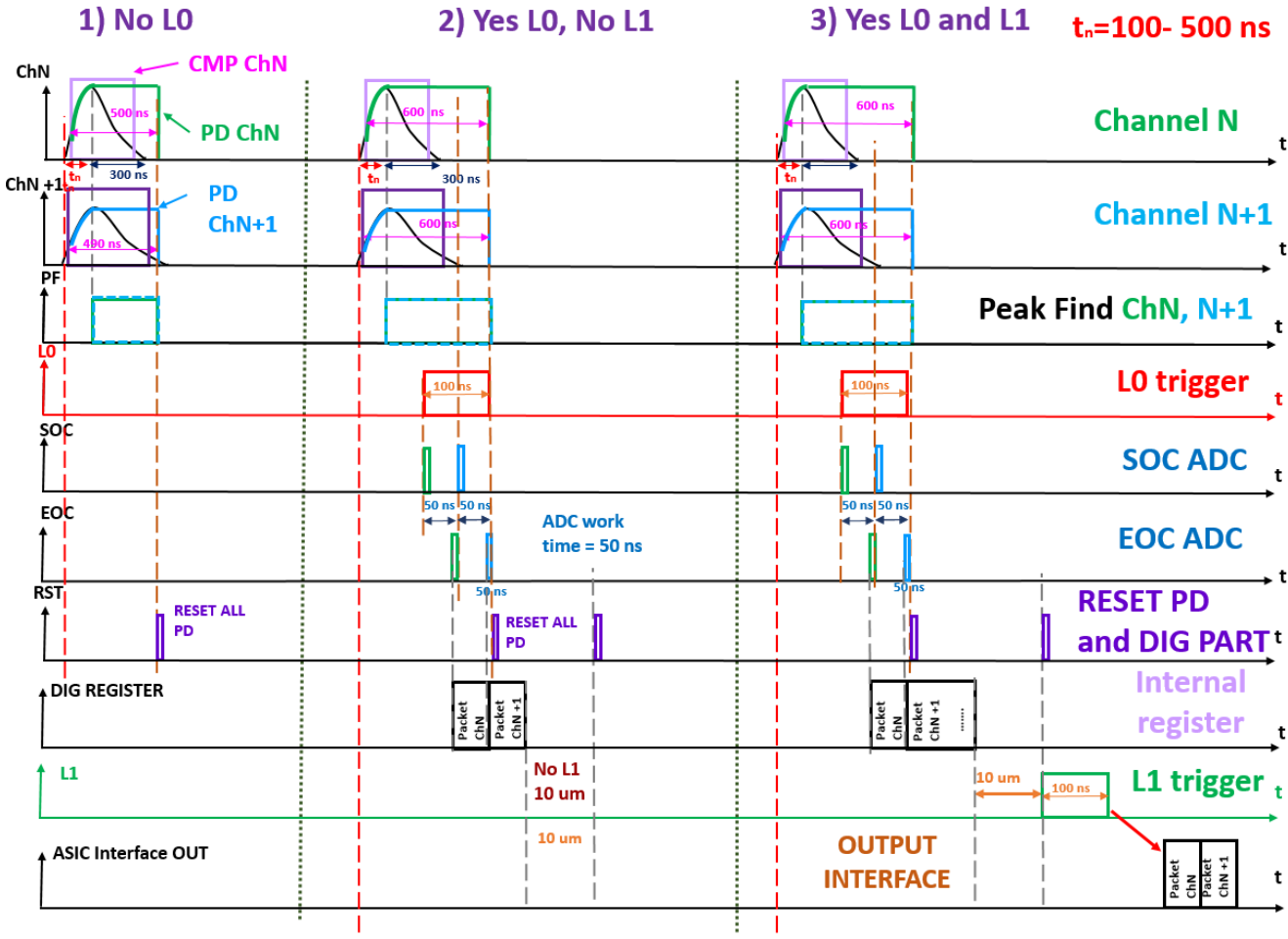
A design route was chosen as Digital On Top: the top level of the project was presented as predominantly digital due to the complexity of the digital part and the need to have a GBTX type interface in the future full-scale version

Part	Designers
Analog: set of 10 analog chains type of ESD+CSA+SH+pol_SW+PD	E. Atkin, S. Yamaliev, Yu. Bocharov, V. Butuzov
Mixed signal: AMUX (incl. ADC driver), ADC	Yu. Bocharov, V. Butuzov
Digital and Digital on Top assembly of whole chip	D. Normanov, P. Ivanov, V. Yurovsky
Auxiliary (analog calibration system, emulator for digital part) and test blocks (SLVS TX+RX, PLL, stand alone ADC)	E. Atkin, S. Yamaliev, V. Yurovsky, D. Normanov, Yu. Bocharov, V. Butuzov

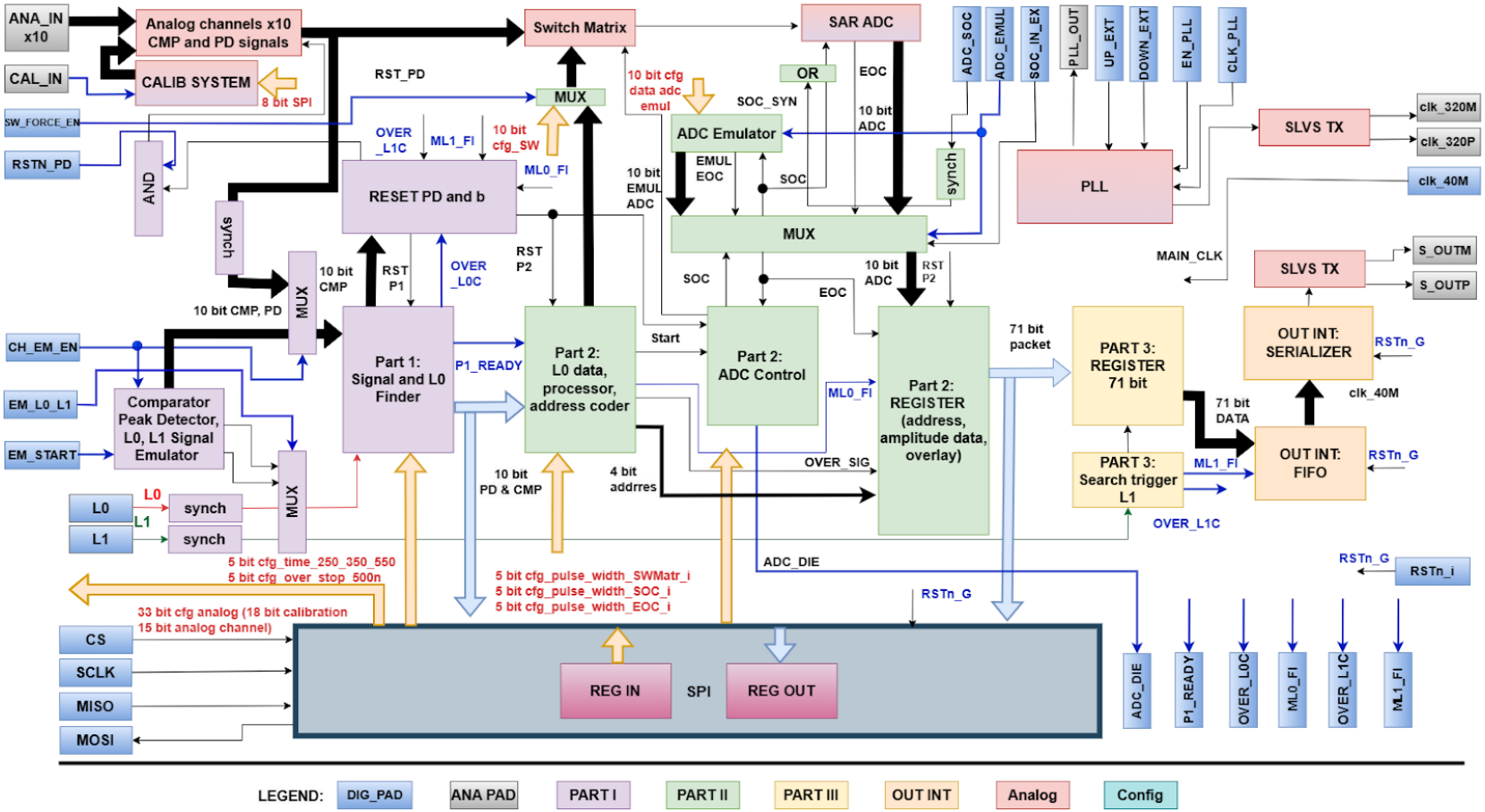
Typical chronograms versus L0 & L1 triggers

The synchronization of the BM@N setup is provided so that the chips process input signals with a maximum frequency of 100 kHz by 2 triggers:

L0 with a frequency of 10 kHz and a delay of up to 500 ns
and
L1 with a frequency of 50 kHz and a delay of up to 10 μs



Digital part



Layout

Process – 180 nm CMOS

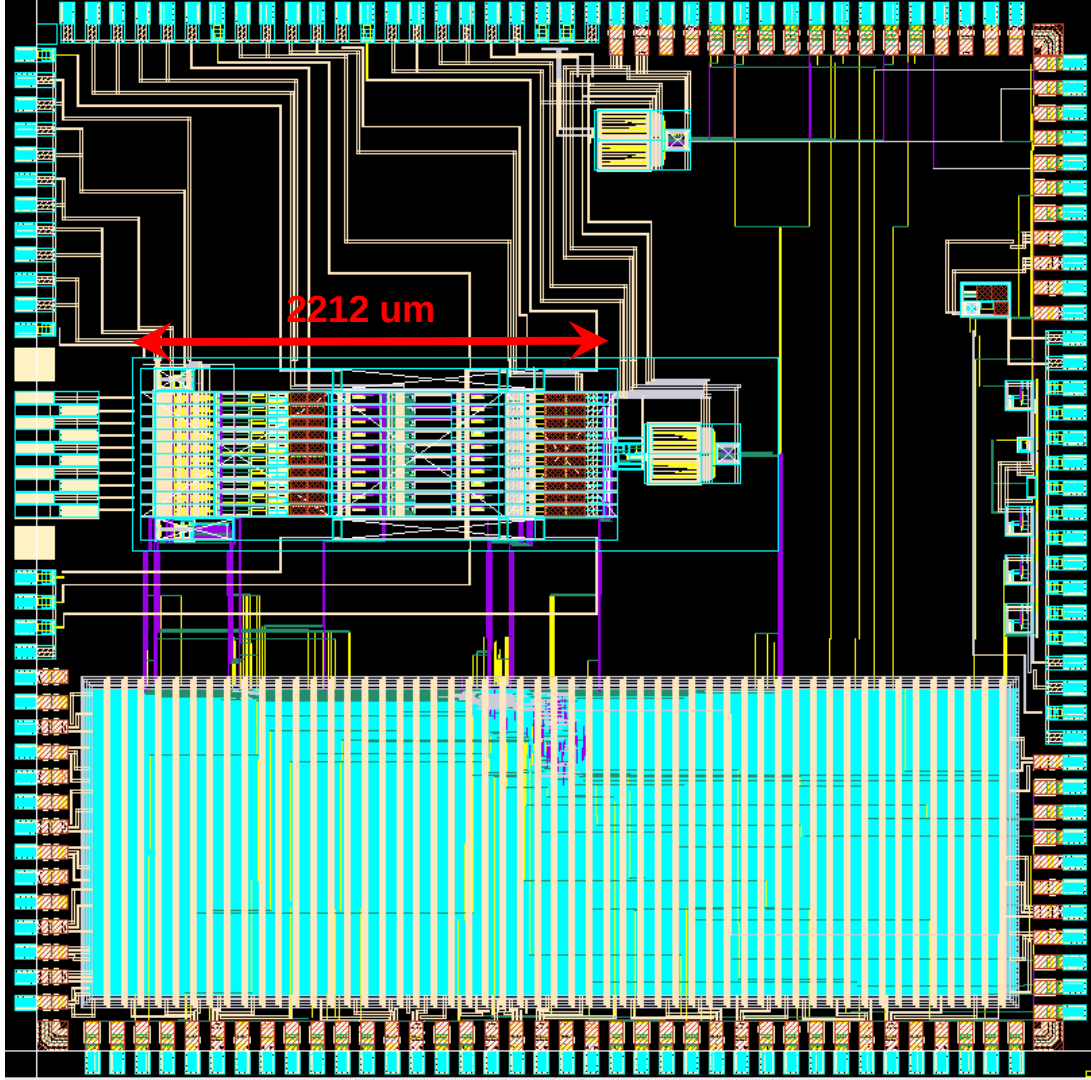
Die size – 5000 x 5000 um

Nb. of analog channels – 8 + 2 (test)

Channel size – 2212 x 57 um

Size estimation for 130 channels: 57*(128+2) = 7410 um

Total nb. of pads (IO cells) – 158, incl. 1) 10 frontend pads, sized by 180 um x 60 um; 2) 16 analog VSS pads, 16 analog VDD pads, 24 digital VSS pads, 24 digital VDD pads



Main building parts

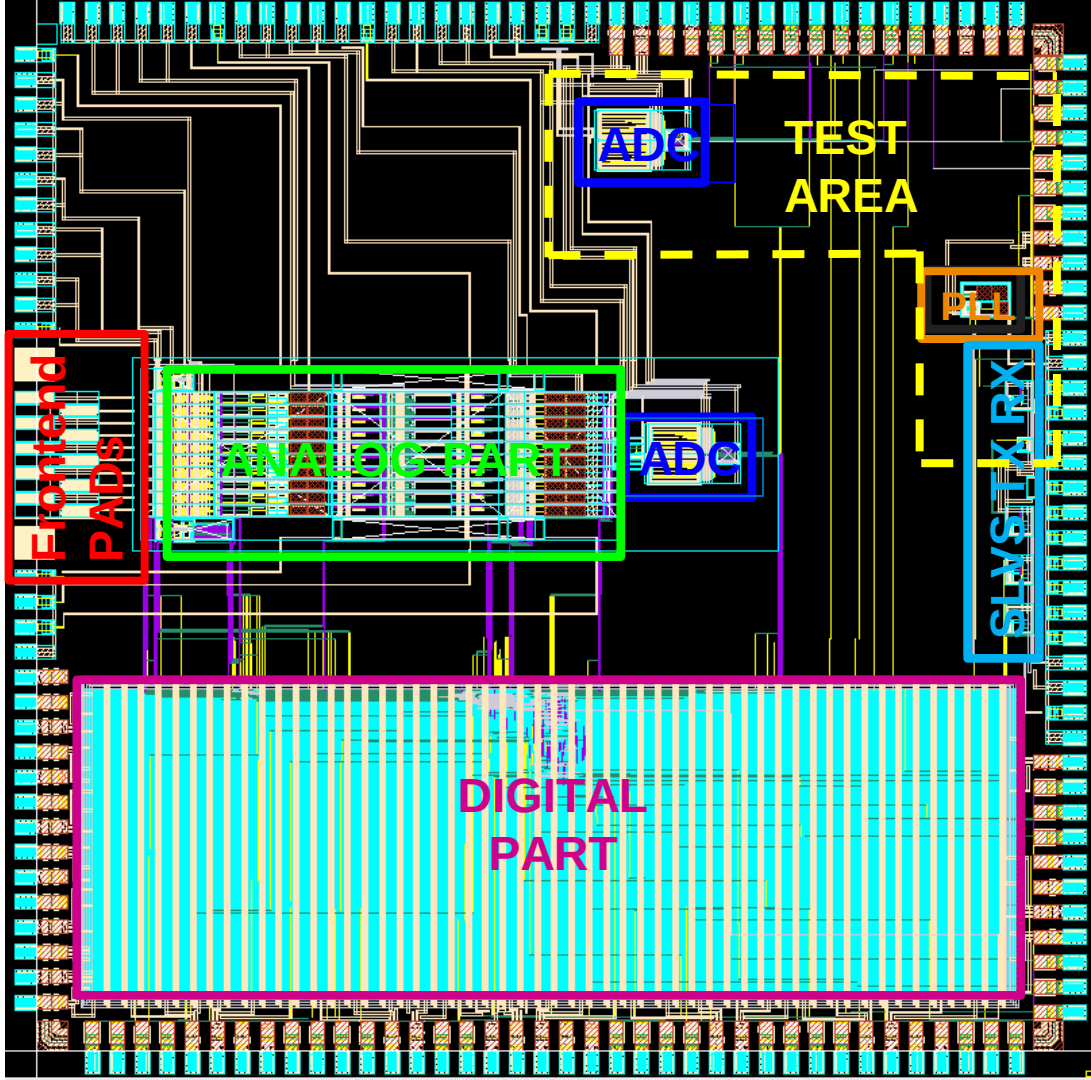
- mostly differential Analog front-end part, including 10 channels of the chain: ESD+CSA+SH+PD and MUX

- 10-bit ADC – one per whole set of analog channels

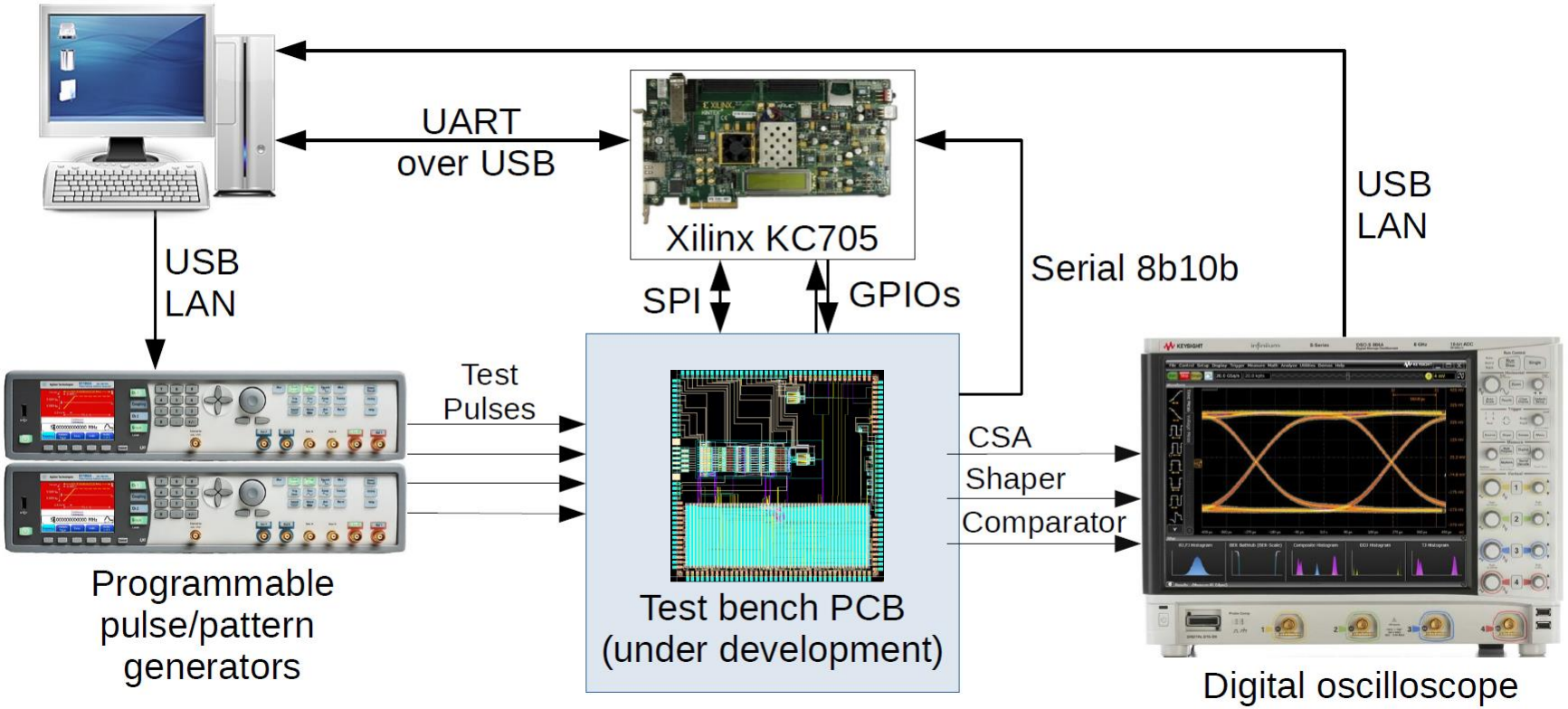
- Digital part, processing packet exchange under SPI control, and followed by SLVX TX

- Test block area, including stand-alone ADC, PLL, SLVS TX & RX

The design of both the analog and digital parts as well as operating protocols were carried out in such a way that they could be used in the subsequent upscaling to the full-scale version for 128 (+ 2 test) channels to be placed within area of 10 mm * 7 mm



Lab test bench



Summary

1) The prototype ASIC for STS has been designed under the 1st stage of the contract between JINR and NRNU MEPhI, signed late December 2022
2) Submission for tape out has been done late July 2023
3) State registration of the topology of the developed prototype chip is planned in the near future
4) Manufacturing of the chips should be made in 180 nm CMOS process by January 2024. Output → 50+ caseless chips
5) The design of the laboratory test bench and the corresponding measurement technique have been started and to be ready before chip supplying
6) The first test results for the ASIC are expected in Spring 2024
7) My gratitude to all the staff members of JINR and SINP MSU, who participated both in the elaboration of the specifications for the chip and in the development of its structural scheme