Progress in the HGND electronics development

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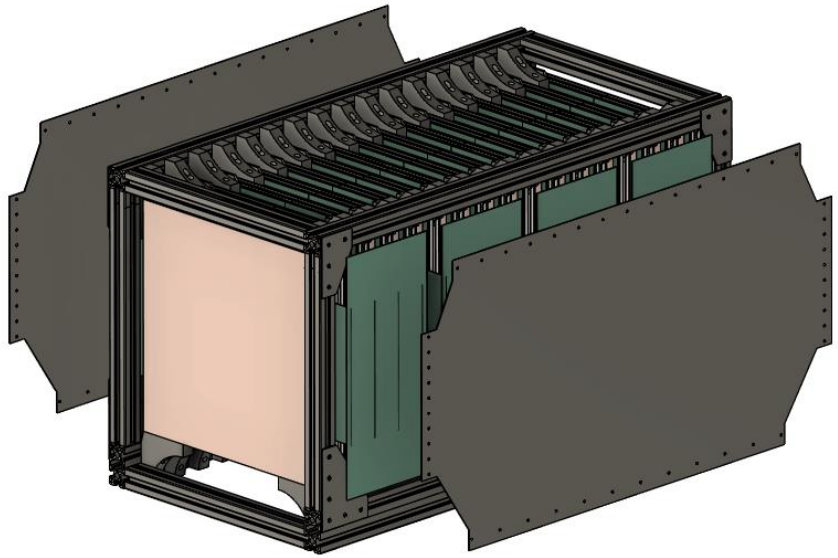
on behalf of HGND team

11th BM@N Collaboration Meeting
28–30 November 2023 LHEP JINR



HGND main features:

- 16 active layers assembled from 11 x 11 scintillator cells 40x40x25 mm^3 and placed between absorber plates.
- Individual light readout by one EQR15 per each scintillator cell.
- 121 readout channels per layer.
- 1936 readout channels in total.

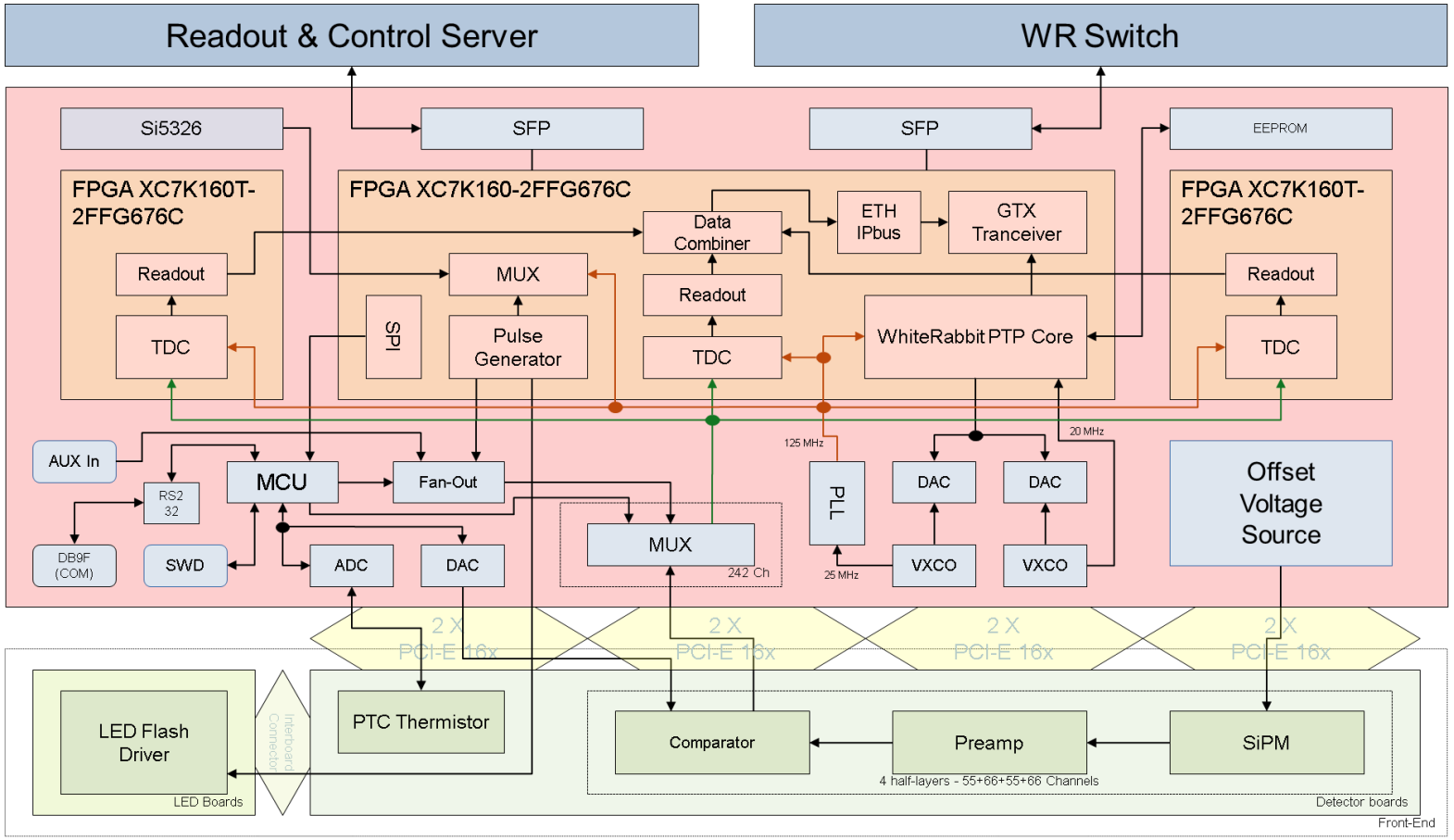
Main requirements to readout electronics:

- Event time resolution <150 ps.
- Charge measurement dynamic range ~15 -20.
- No space for the cable connections or digital electronics in the detector layers.
- Average readout rate < 1 kHz per scintillator cell.

Main HGND electronics design ideas:

- 66 or 55 fast EQR15 SiPMs with 20 dB amplifier and comparators on one PCB
- Single level Time-Over-Threshold measurement with slewing correction for amplitude and time.
- The FPGA-based 100 ps resolution multichannel TDC based only on documented FPGA features
- Only one LVDS line to readout board per channel through the PCB edge PCIe x16 connectors
- No analog signals between detector and readout PCBs
- Hardware pulse response correction to fit the single-exponent decay model **(see N.Karpushkin presentation**).

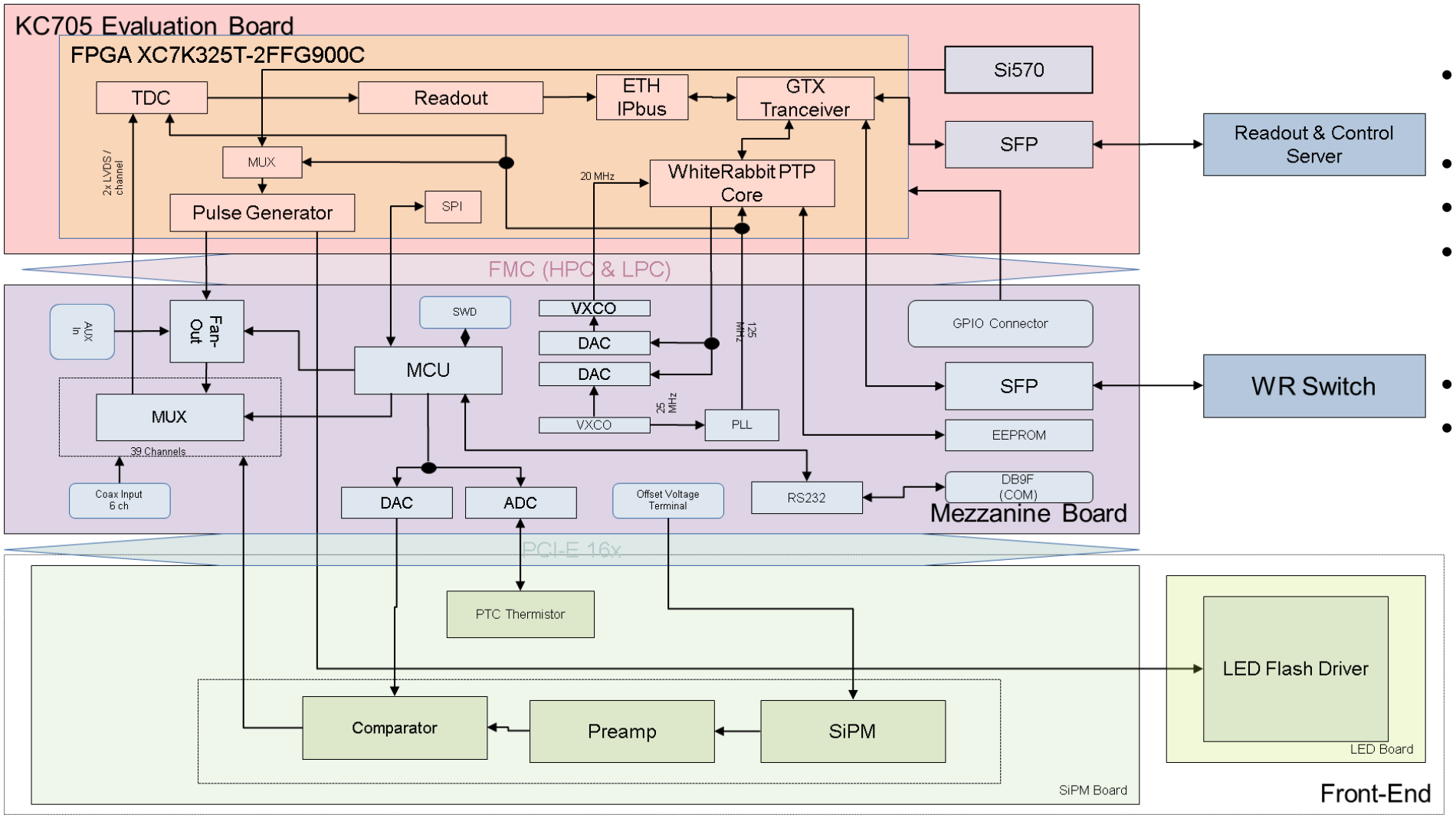
Readout electronics board



- 242 readout channels with the 3 FPGA CX7K160T FPGAs per board.
- HGND - 8 readout boards
- White Rabbit as synchronous clock source, timing and trigger
- UDP IPbus protocol for data transfer and control
- SiPM offset voltage source and comparator threshold control
- Self-test features
- 4 PCIe x16 connectors for detector boards

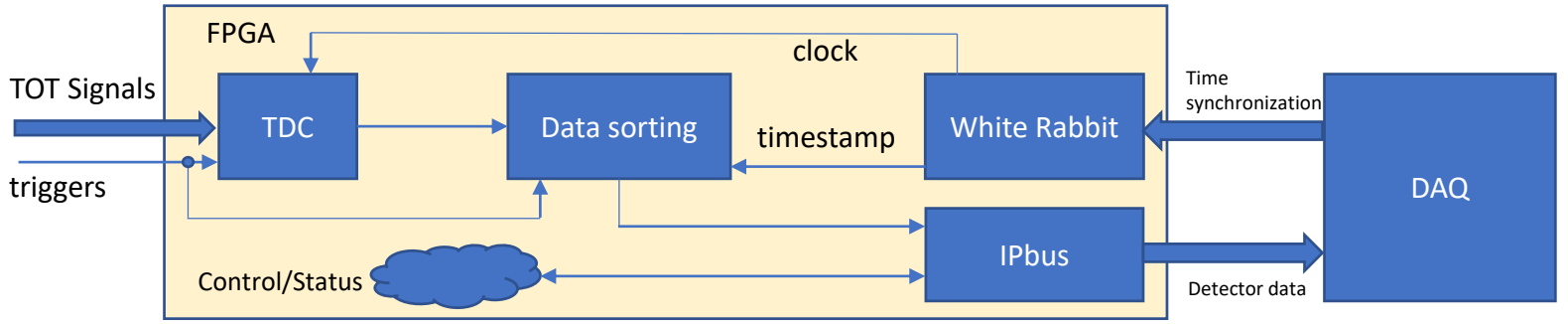
***There will be two type of readout boards – left and right (55+66+55+66 and 66+55+66+55 channels per connector respectively)**

Readout board prototype



- Based on KC705 evaluation board
- 39 readout channels.
- White Rabbit hardware
- SiPM offset voltage source and comparator threshold control
- TDC self-test and calibration
- 1 PCIe x16 connectors for detector half-layer board

The FPGA firmware development

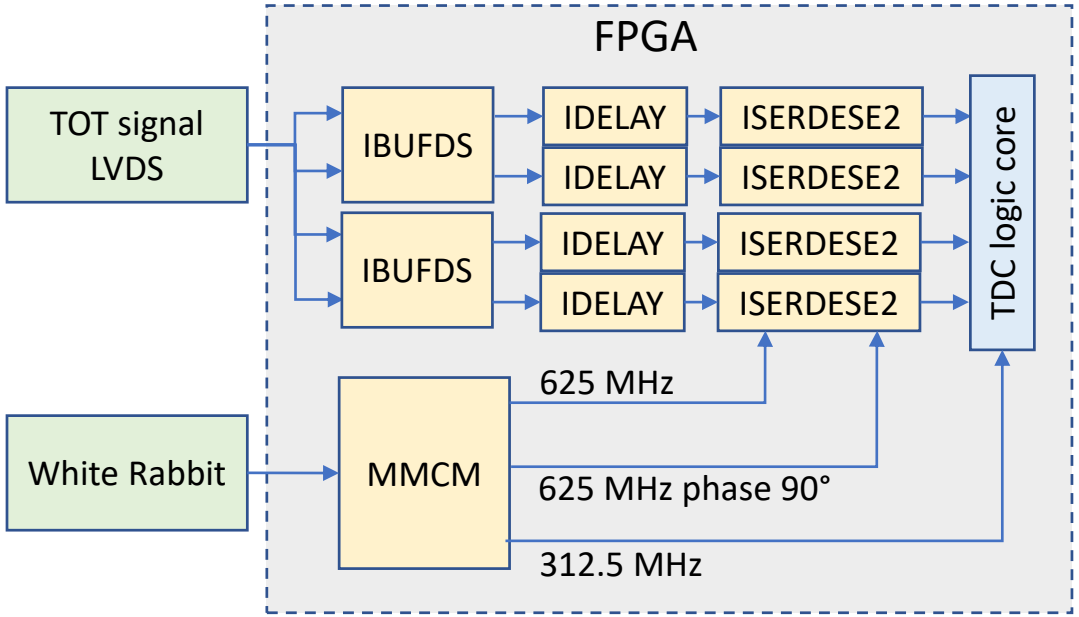


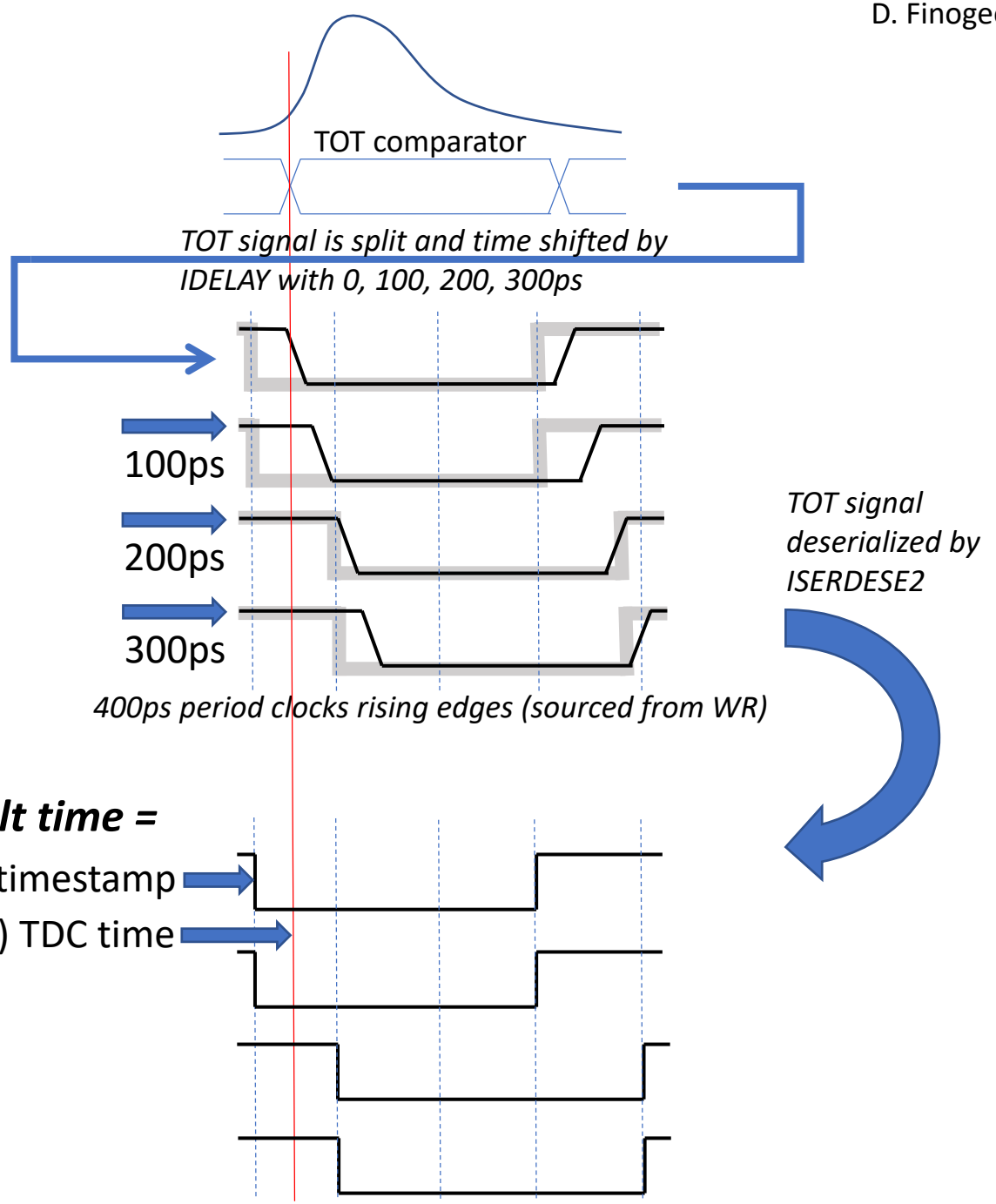
HGND firmware readout functional scheme

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip
- White Rabbit (WR) is used for event's time synchronization:
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events
- Ethernet UDP protocol (IPbus [1]) is used for data forwarding and board control
- Two trigger options:
  - triggered readout – only data coincidental with trigger are sent.
  - continuous readout – trigger signals are presents in the data as bit flags
- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit for 84 channels (single FPGA) is not exceed ***30 Mb/s***.

[1] J. Serrano, P. Alvarez, M. Cattin, E. G. Cota, P. M. J. H. Lewis, T.Wlostowski et al., ***The white Rabbit Project***, Proceedings of ICALEPCS TUC004, Kobe, Japan, 2009

The 100ps FPGA TDC principles of operation





The TDC is based on the Kintex-7 input serial-to-parallel converter with oversampling capability and programmable delay. The design is based on Xilinx recommendations, and uses only documented features of the FPGA within its specifications. Time value consists of the data from the 312.5 MHz counter and encoded to 5 bits data from the 4 input ISERDES (which provides 32 bits of data each 3.2 ns).

[2] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment***. e-Print: 2309.17235

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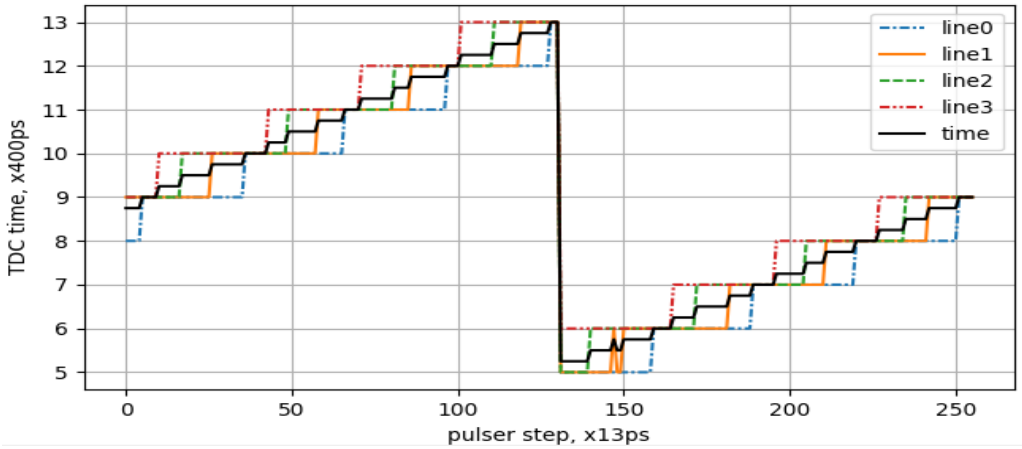
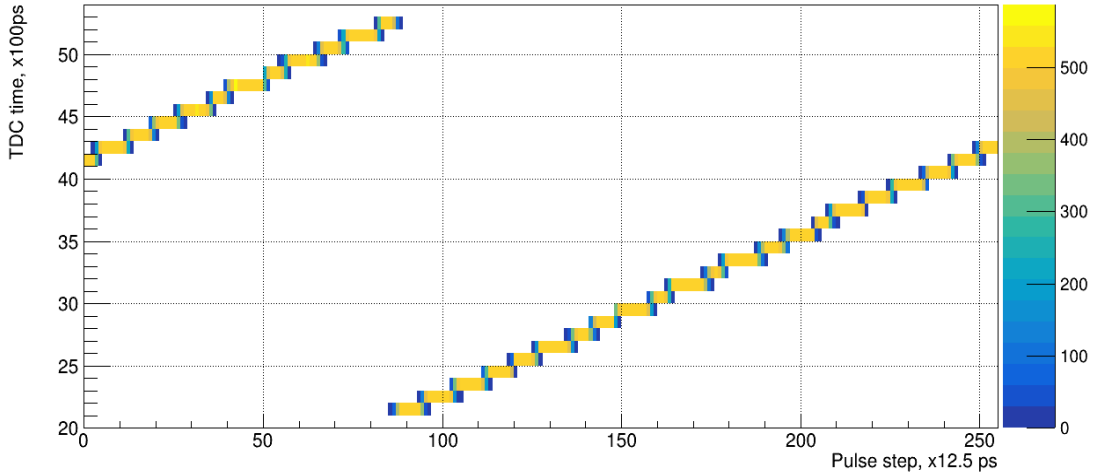
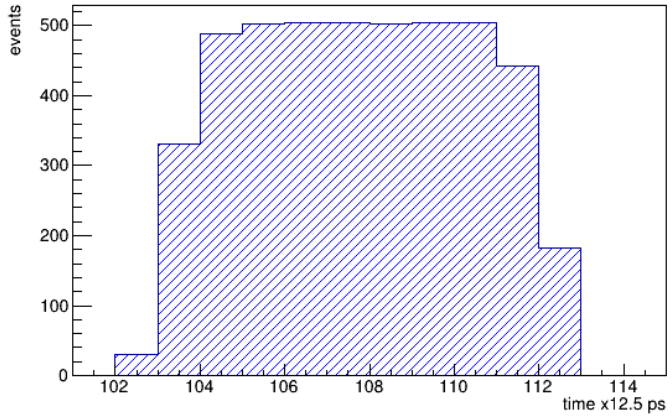
The FPGA TDC time scan results

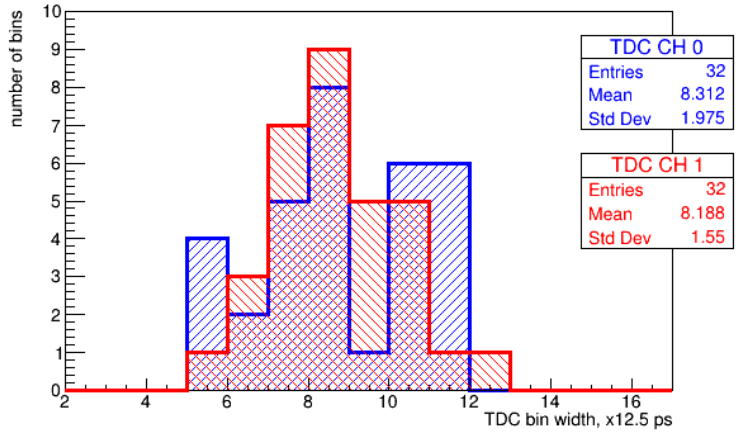


Four TDC lines and the resulting time dependence on the pulse time shift are shown. Pulses are generated by FPGA MMCM synchronously to the TDC clock with a phase step of 12.5ps. The single scan pass was taken with a digital FPGA logic analyzer.



The TDC time dependence on pulse time shift. Pulses are generated by FPGA MMCM synchronous to TDC clock, and the time step is 12.5 ps. Data was taken with PC readout, 1000 events per single time shift step.

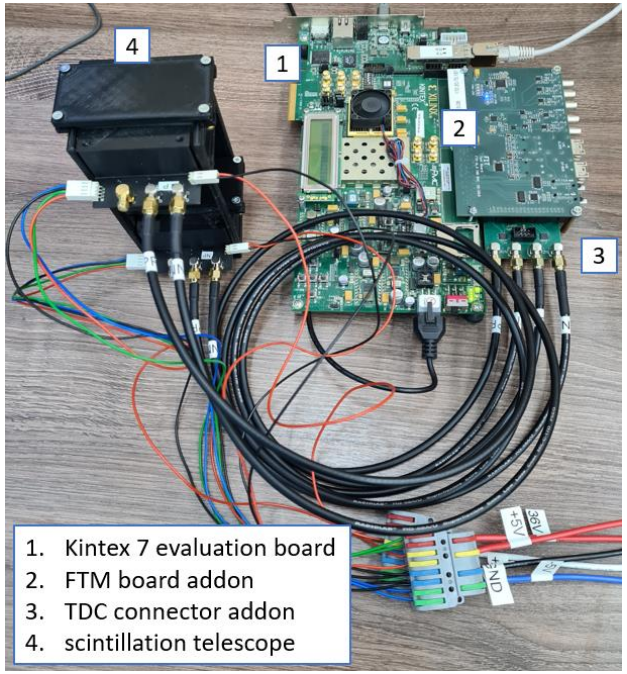




The TDC bin width measured with pulses synchronous to the TDC clock. Left: Typical TDC bin profile taken with a synchronous time scan. Right: The TDC bin width distribution for both TDC channels. The bin width value taken at the amplitude level is 30% in the bin profile. The TDC bin width distribution RMS is ***20 ps***. The main contribution to the TDC bin width distribution is the TDC line delay alignment step of 38.8 ps.

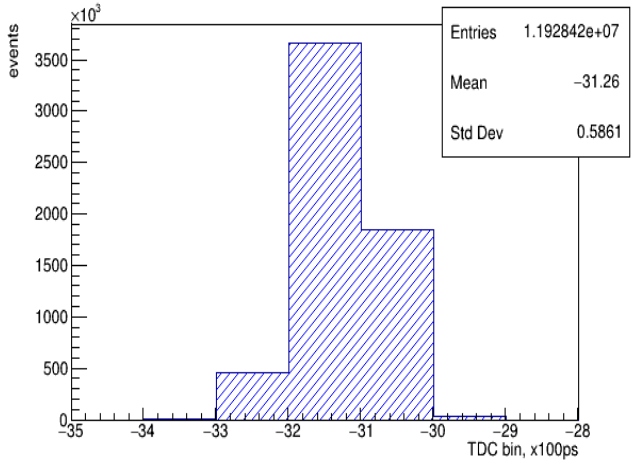
D. Finogeev

The FPGA TDC test results



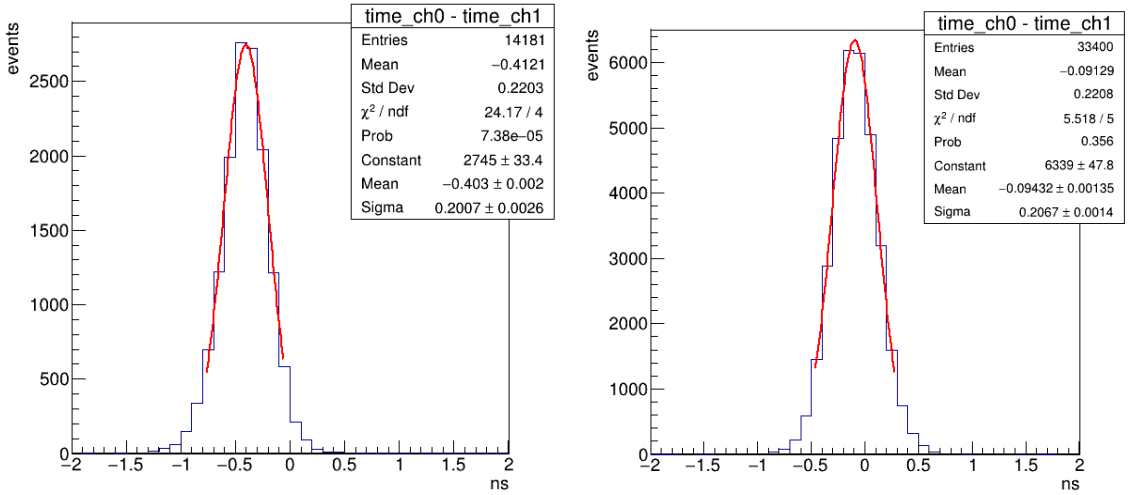
HGND scintillator cells telescope is connected to 2-channels TDC prototype based on KC705 evaluation board

The time difference distribution between two FPGA TDC channels measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).



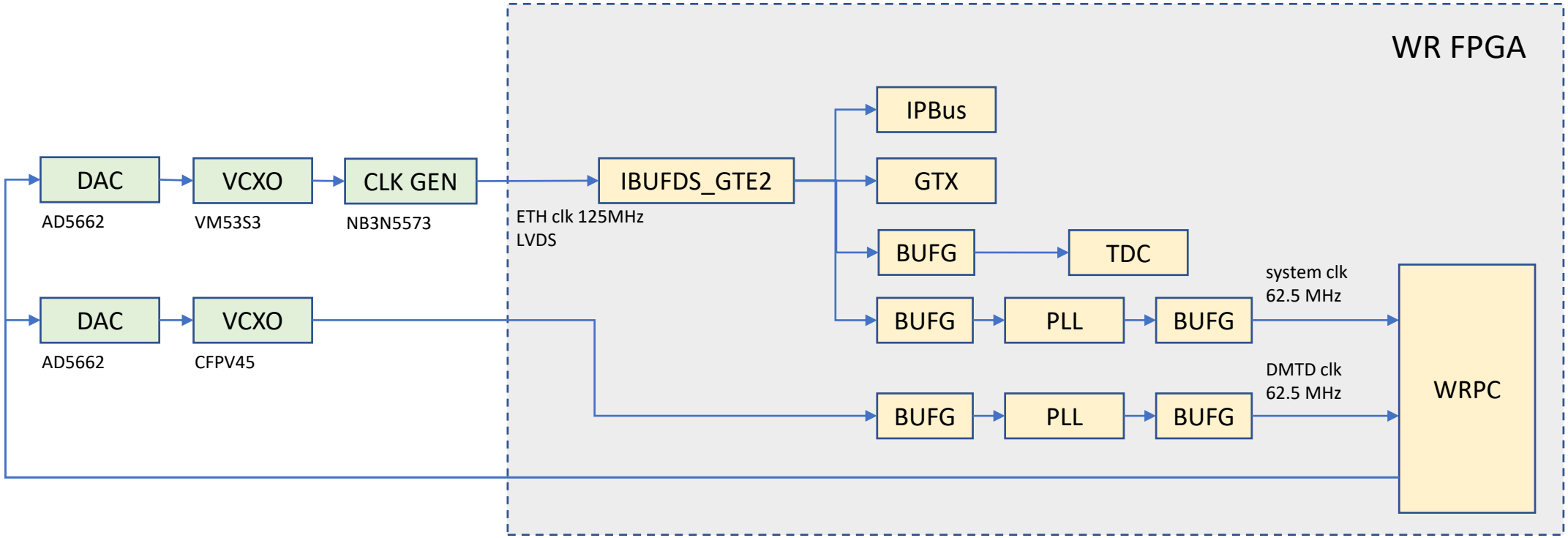
The RMS of single TDC channel is 42ps, which demonstrates good agreement with the estimated quantization error typically obtained using Tbin / √6 = ***40.8 ps***

The time resolution measurements with the FPGA TDC prototype board were performed with the 280 MeV electron beam on the “Pakhra” synchrotron in LPI (Moscow, Russia).



The time difference distributions of two cells of the telescope measured with the CAEN digitizer (left) and the FPGA TDC prototype board (right). Time resolution is ***146 ps*** per single HGND channel.

The White Rabbit implementation



- Clock generation schematic is based on White Rabbit PTP Core (WRPC)
- HDL code sourced by JINR WR core (AFI board top design)
  - g_fpga_family => "kintex7",
  - g_with_external_clock_input => FALSE,
  - g_use_default_plls => TRUE,
  - g_direct_dmtd => FALSE,

Conclusions

- The analog part of the design was developed and fully tested for single scintillator detector.

- Full-scale detector board has been designed. Now PCB design is preparing for production.

- The 100 ps TDC has been developed, implemented with K7 FPGA and tested:
  - ***42 ps*** single channel time resolution was measured with data generator DG2040 (Cycle-to-Cycle Jitter 5ps).
  - Time resolution for single HGND scintillator cell was measured with the 280 MeV electron beam on the "Pakhra" synchrotron) using developed TDC. The obtained time resolution **146 ps** is in good agreement with time resolution measured with CAEN digitizer.

- The multichannel prototype readout board is under development (expected readiness – Feb. 2024).
  Main features of the board:
  - 39 TDC channels: 33 HGND cells + 6 SMA debug channels
  - White Rabbit clock generation scheme
  - FPGA loopback pulser generator for calibration and tests purposes
  - 20 GPIO for debugging (scope, logic analyzer, etc.)
  - MCU loopback pulser MUX control

- FPGA test design (39 channels + WR + IPbus) uses < 30% of Slice LUTs - good margin for the final design

Thank you for attention!