



National Research
**Tomsk
State
University**

TSU HEP laboratory

Embedded systems

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TSU HEP laboratory facilities

High performance servers for build&testing

Intel i7, AMD Ryzen 7xxx

Dev. Boards

Intel Cyclone5, MAX10

Microsemi SF2

Xilinx Artix7, Kintex7, US, Zynq7k/MPSoC

BMTI

Manpower

Senior FPGA engineer

Middle FPGA engineer

2 junior embedded engineers-students

Expertise

FPGA and SoC:

Intel (Altera), Xilinx, Microsemi. VHDL, Verilog/SystemVerilog, UVM, cocotb and etc.

Software:

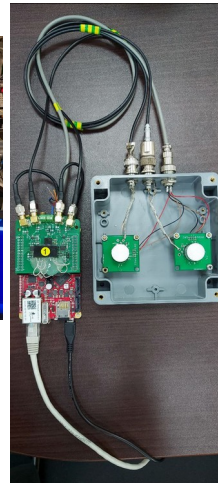
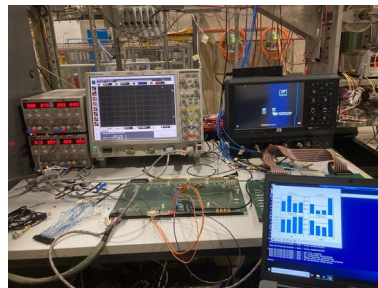
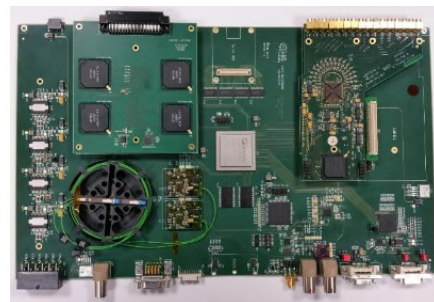
Qt, MS VS, Python, C/C++ (incl. embedded), MATLAB, CERN ROOT and etc.

Equipment:

Oscilloscopes, waveform generators and etc.

Interests:

high-performance DSP systems; front-end electronics for HEP; RTL verification.





Spectrometer core

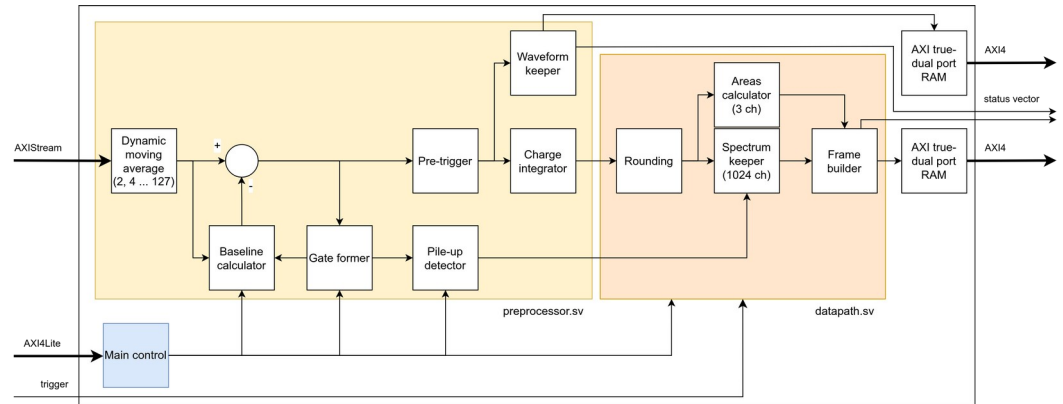
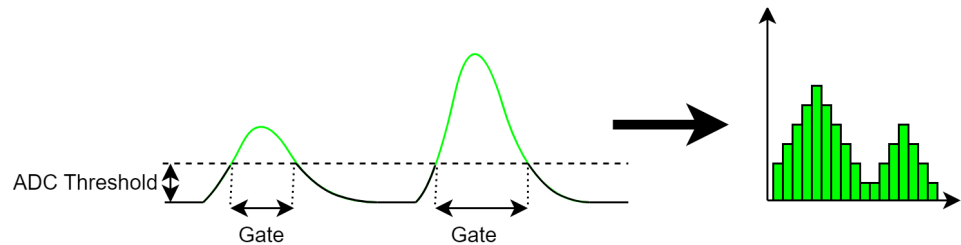
Spectrometer IP core. Vendor-free, FPGA-proven, with test environments. Ready to use.

Input:
SiPM→ADC pulses

Processing:
Moving average, decimation, baseline compensation, pile-up detection/removal, zero charge suppression and etc.

Results:
Spectrum histogram 1k..8k channels

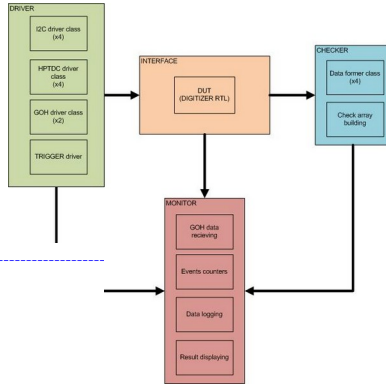
Features:
Waveforms dump
32bit pulses counters
Up to 255 channels
Full-featured AXI4 and AXIStream interfaces
*Python/C API





RTL verification

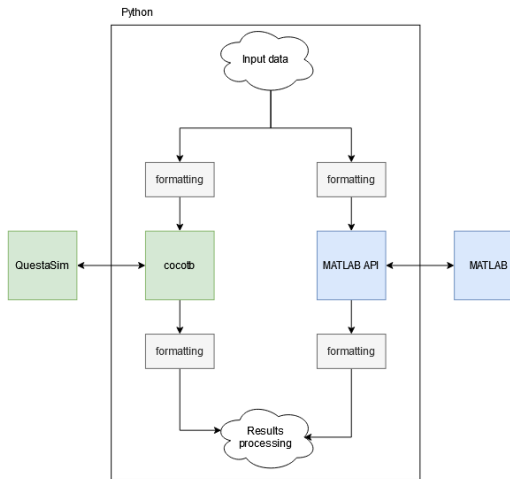
Custom SystemVerilog test environment (VMM based)



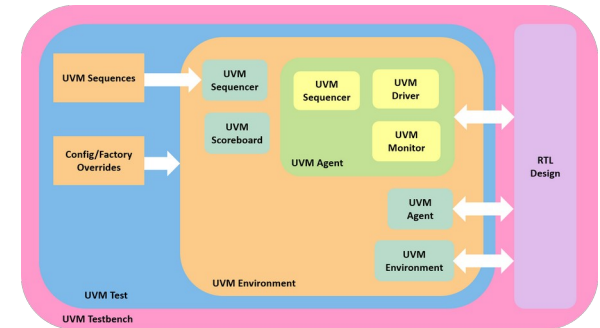
```
# Loading work_croccitvfat (behavioral)
# //-----
# $vars
# [MAIN] Enabling firmware...
# [MAIN] Run triggers...
# 01715150000 [TRIGGER]: BUNCH RESET
# 02715300000 [TRIGGER]: RUN
# 02726985000 : GCH_1 frame [1] lock
# 02726985000 : GCH_0 frame [2] lock
# 03715450000 [TRIGGER]: RUN
# 03727135000 : GCH_1 frame [3] lock
# 03727135000 : GCH_0 frame [4] lock
# [MAIN] RESULTS:
# -----
# TRIGGERS:
# | Transmitted | Locked | Passed |
# |-----|-----|-----|
# L1 | [2] | [-] | [-]
# B0 | [1] | [-] | [-]
# RESYNC | [0] | [-] | [-]
# B0_2 | [0] | [-] | [-]
# -----
# FRAMES:
# | Transmitted | Valid | Invalid |
# |-----|-----|-----|
# | [4] | [4] | [0] |
# -----
# ** Note: $stop : ../tb/tb_top.sv(214)
# Time: 3815450 ns Iteration: 0 Region: /tb_top/init_tb
# Break in Task end_testing at ../tb/tb_top.sv line 214
```

VSM 18> Project: tb (New: 3)

Modern technics: Python (cocotb)

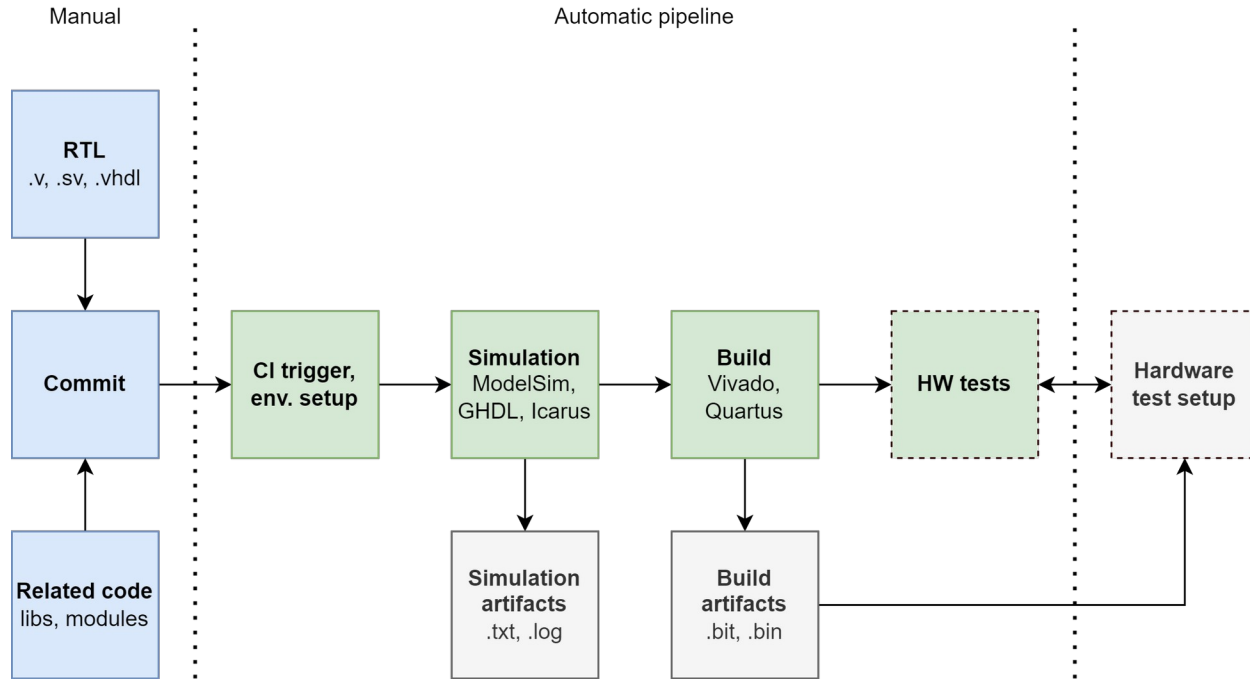


Verification with industry-standard UVM





FPGA specific DevOps tasks (CI/CD)

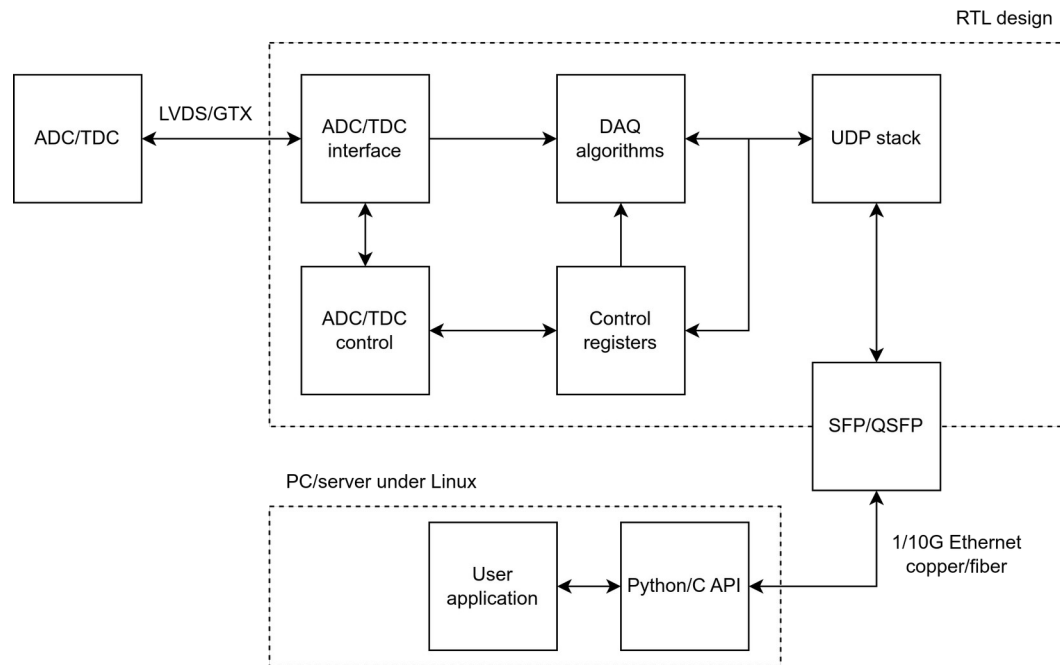




Control & DAQ system

High performance DAQ & control IP core with C/Python API. Concept

Connection via Ethernet 1/10G
AXIStream/AXI4 interfaces
UDP/IP support





Summary

System design:

Throughput analysis, design optimization, architecture creating, CI/CD (DevOps) tasks for RTL/FPGA

RTL design for FPGA/ASIC:

SystemVerilog, Verilog, VHDL, HLS

RTL verification:

cocotb, C, UVM

Embedded design:

Buildroot custom builds, Linux drivers, userspace applications

Modeling:

Python, MATLAB, Simulink

Recruiting:

We're member of Digital Design School.
Expect 1-3 embedded/verification junior engineers per year.