# Mechanical design, front-end electronics and integration of the HGND readout into the BM@N experiment data acquisition system

***D. Finogeev***, **A. Makhnev**, F. Guber, A. Izvetnyy, S. Musin, D. Serebryakov
INR RAS, Moscow

12th Collaboration meeting of the BM@N experiment May 16, 2024

# Outline

A. Makhnev:

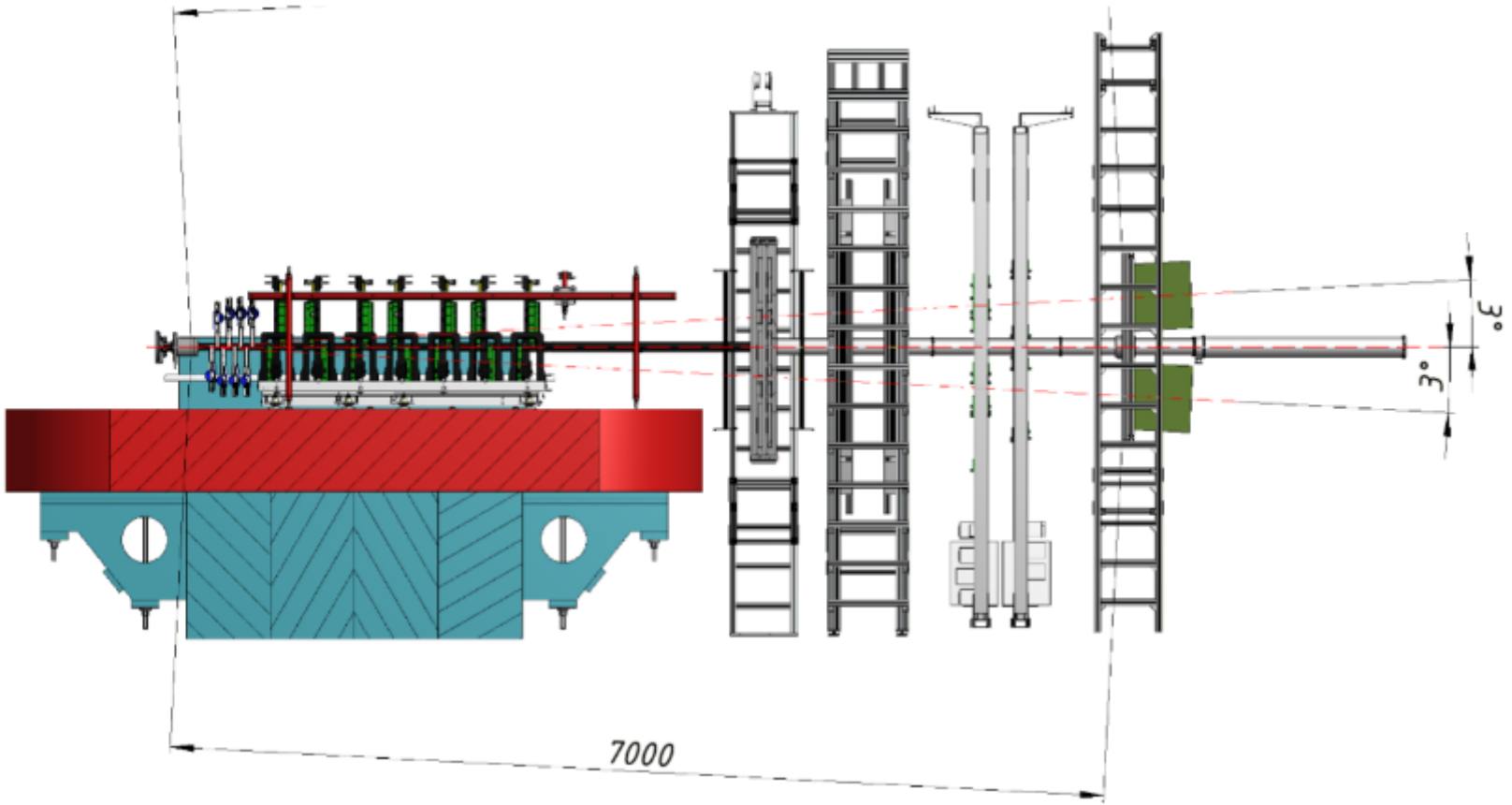
- Geometry & support structure
- FEE & LED boards assembly status,
- HGND assembly & mechanical mock-up

D. Finogeev:

- Readout board: development & tests
- Status of the DCS & readout software

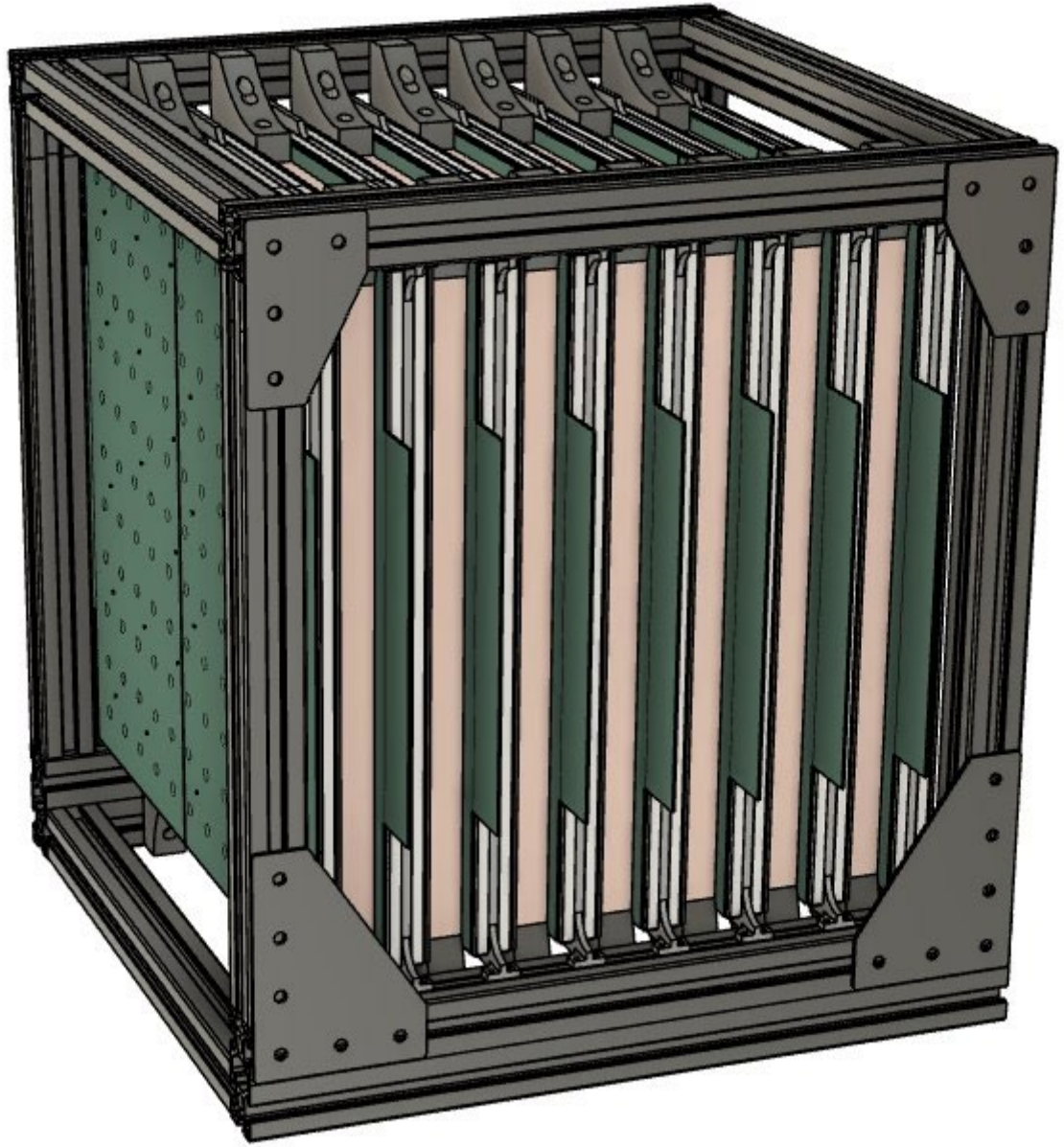
# Detector arrangement

- Detector for high-energy neutron flow measurement
- ToF method with T0 as the “start” signal source
- 7m measurement distance
- Detector is split into 2 “blocks” for improved acceptance



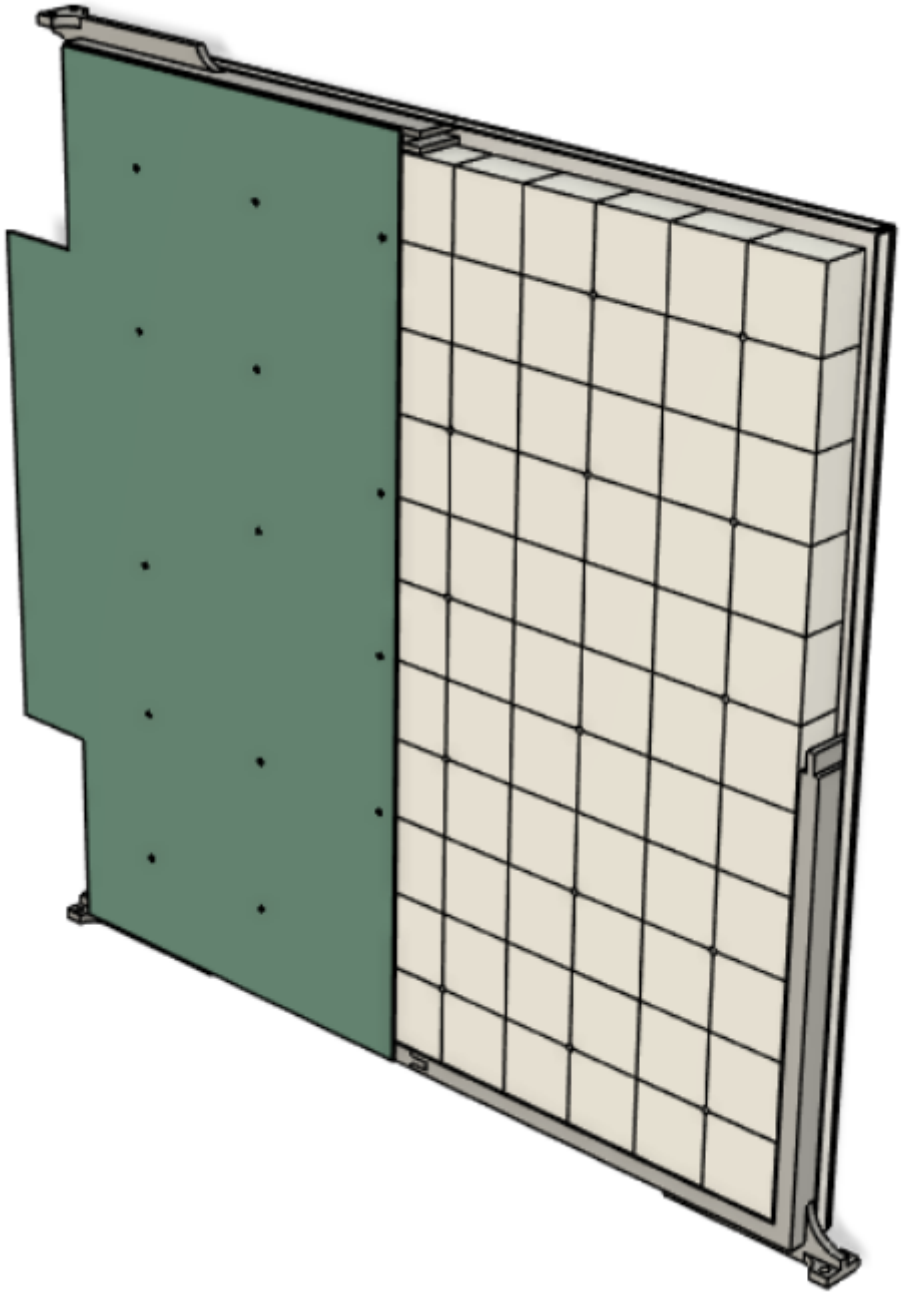
# Detector “block”

- Each block consists of:
  - A VETO-layer
  - 8 Cu absorbers
  - 8 sensitive layers
    - 11x11 grid of scintillatiors each
- Assembly is light-tight and air-cooled
- Framing is built with light-weight Al profiles

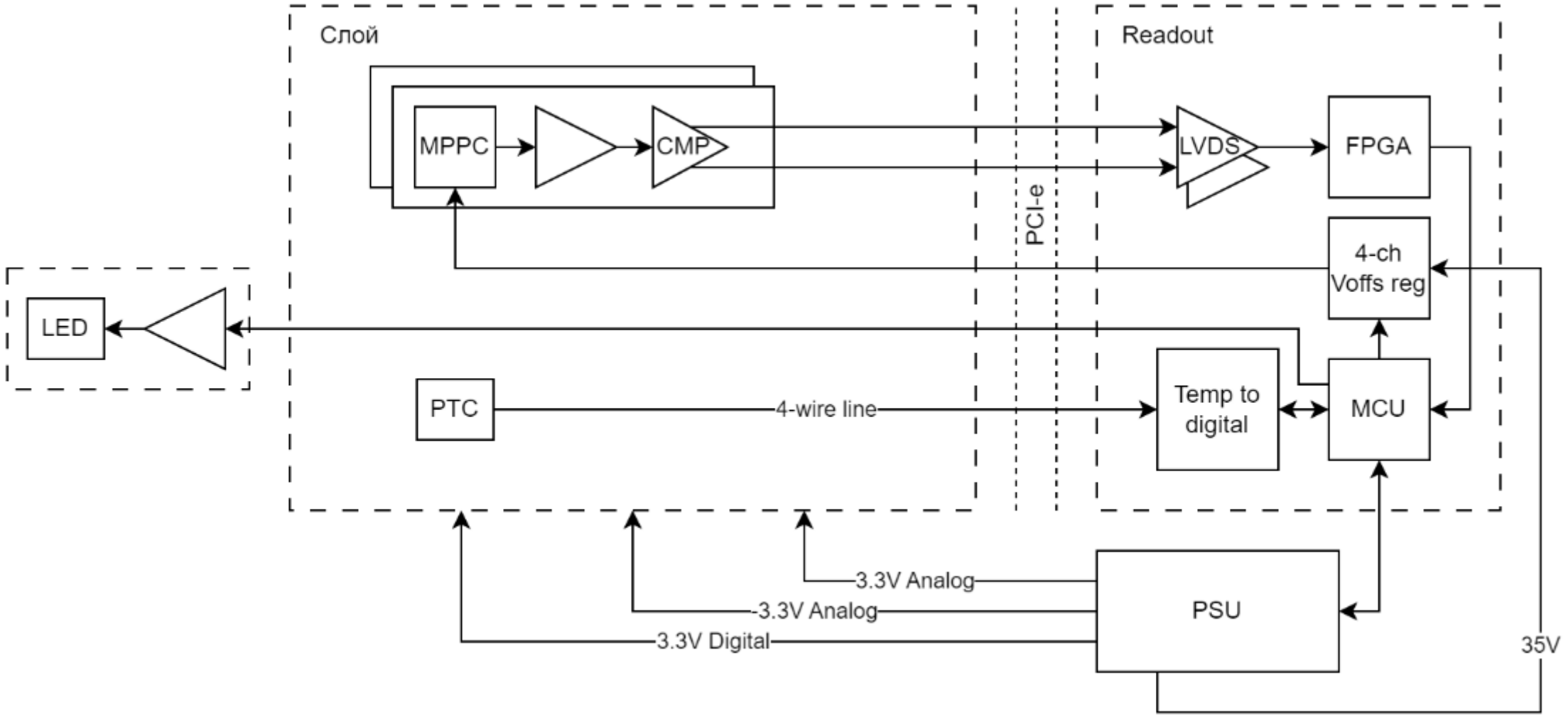


# Detector layer

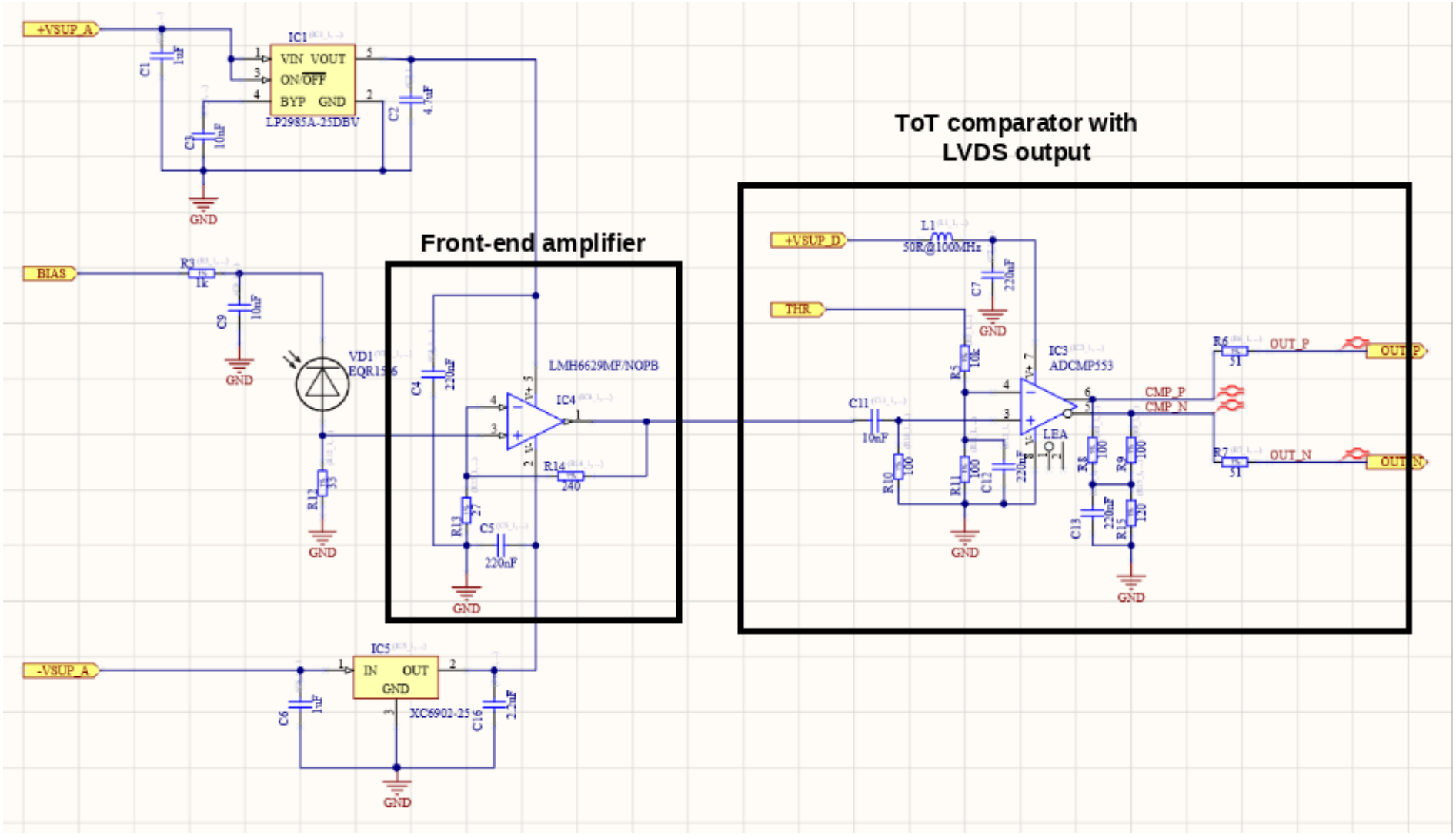
- Each layer consists of:
  - 11x11 grid of individual scintillatior tiles
  - A front-end readout board
  - An LED calibrator board
- Layer is assembled in a light-tight 3D-printed casing
- Readout boards connects to the data collection equipment via edge connectors



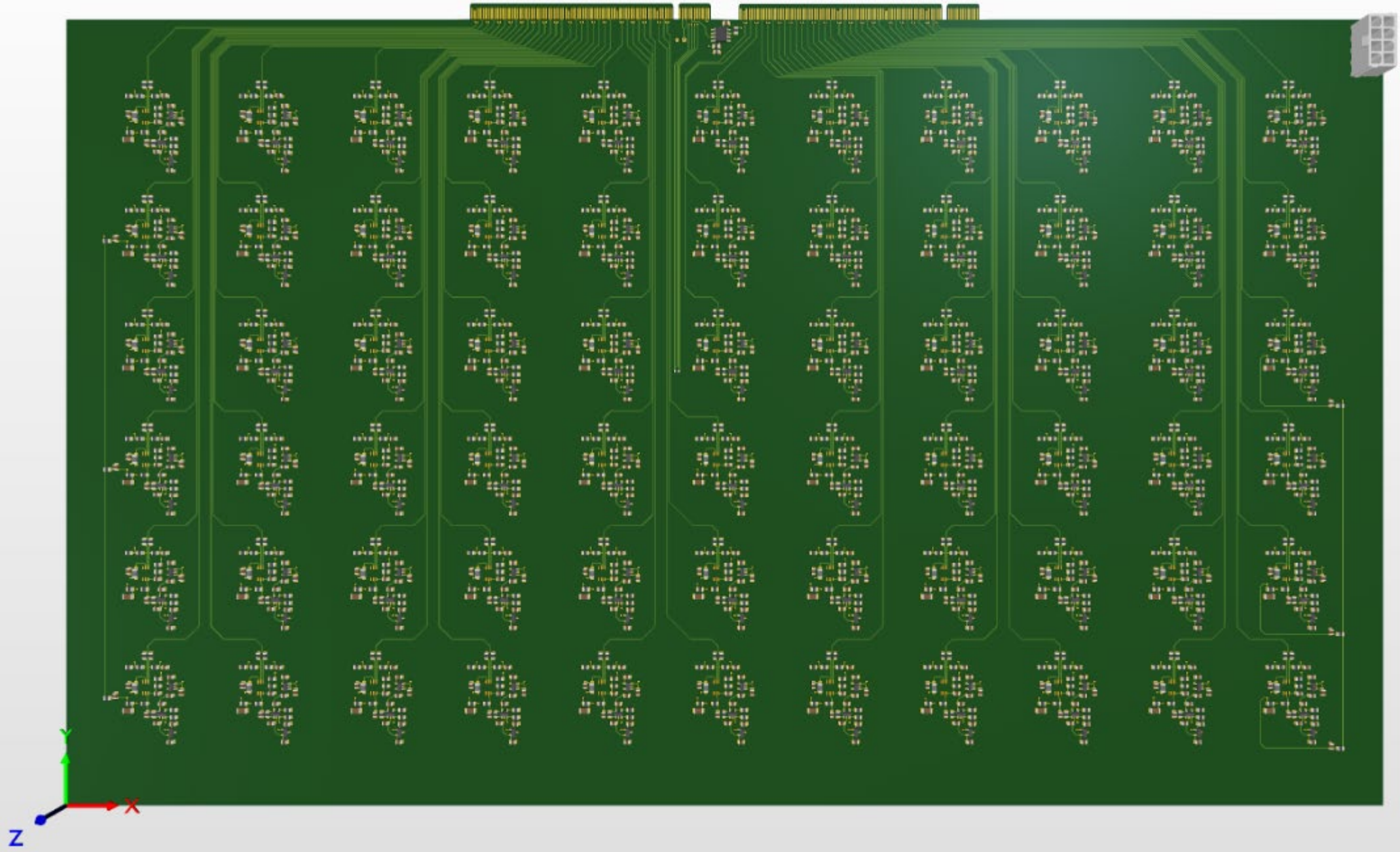
# HGND electronics architecture



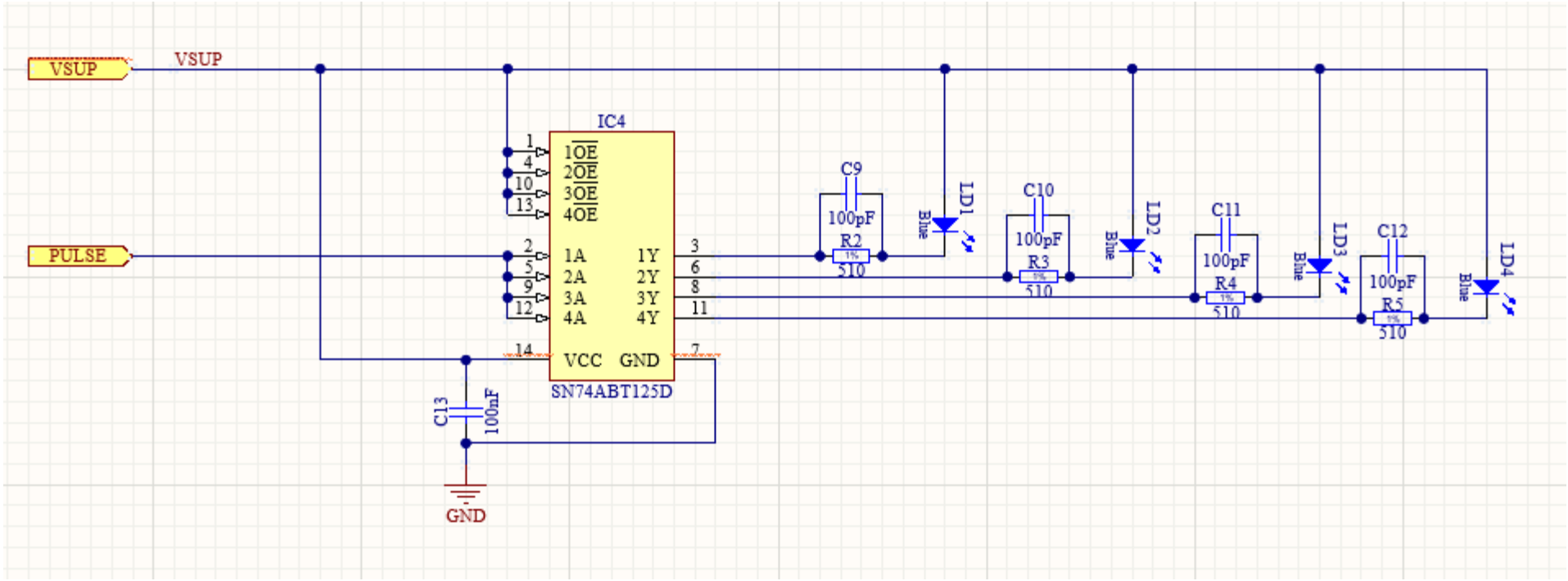
# Front end electronics



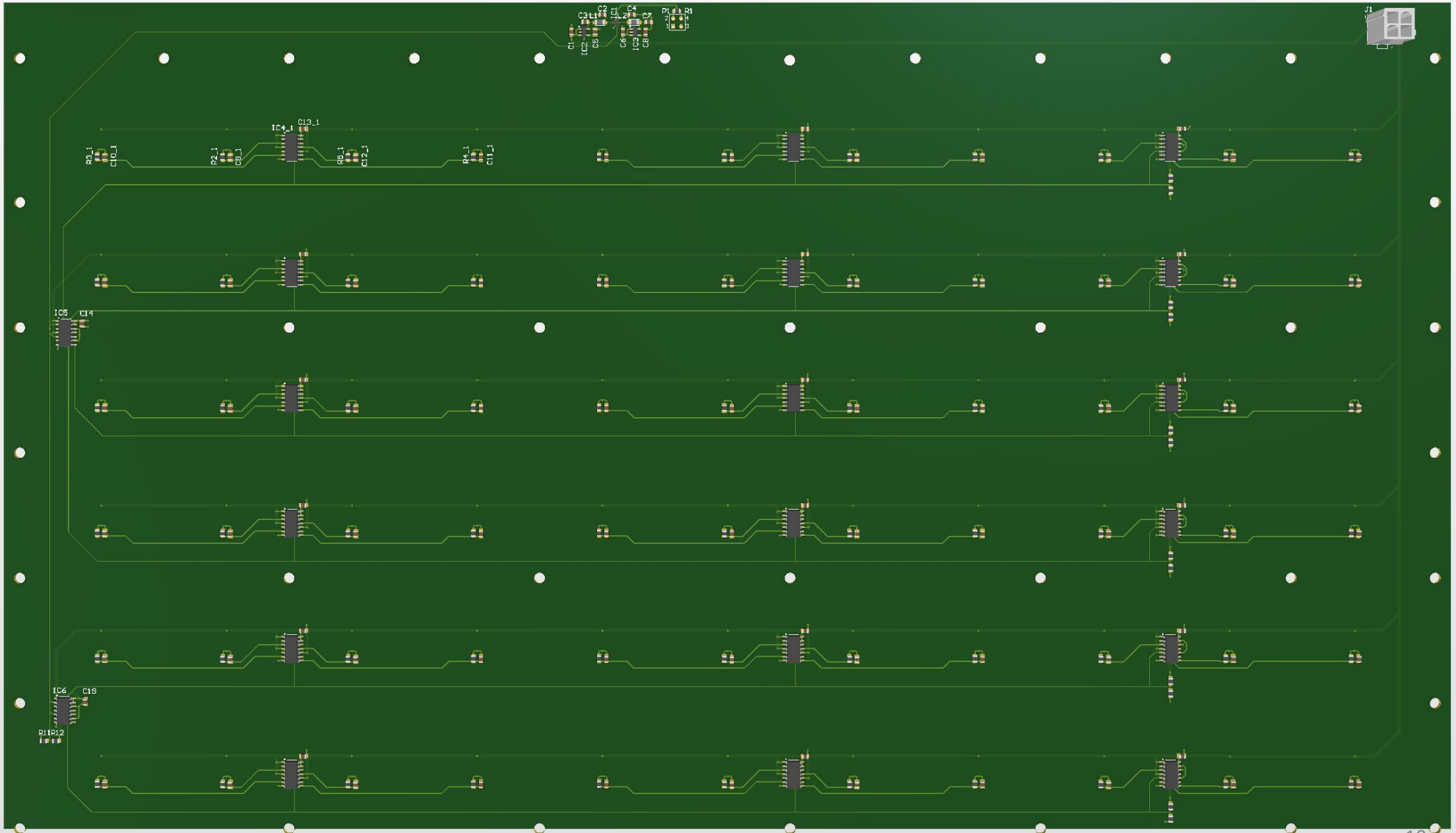

- 20dB amplification
- 2.2 nV/$\sqrt{Hz}$ noise level
- Per-channel supplies
- Variable threshold (common for the half-layer)
- LVDS output


Y
X
Z

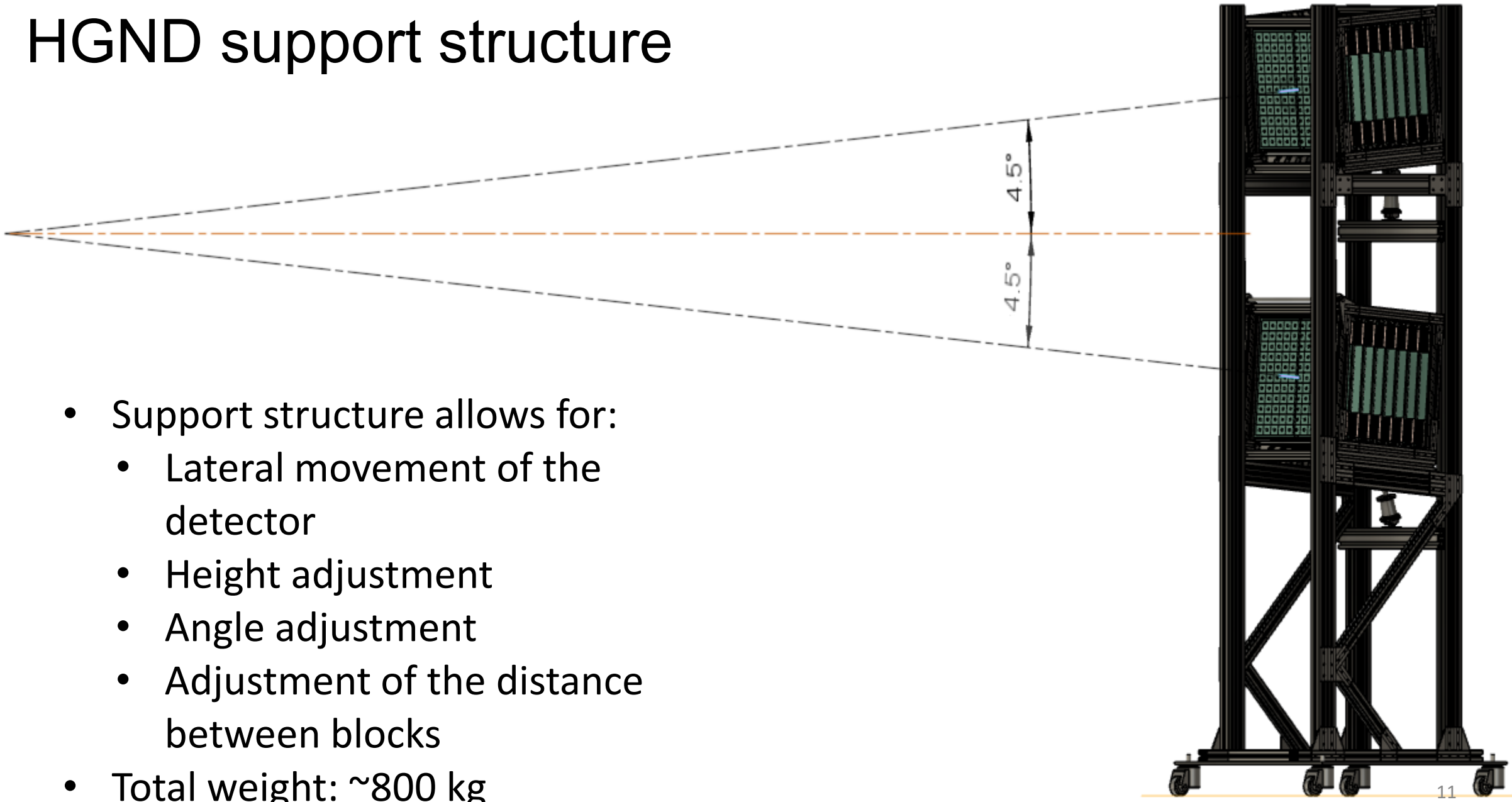
# LED pulser




- LVDS-driven
- Buffer network with terminated impedance-matched traces
- Simultaneous illumination of all 66 channels

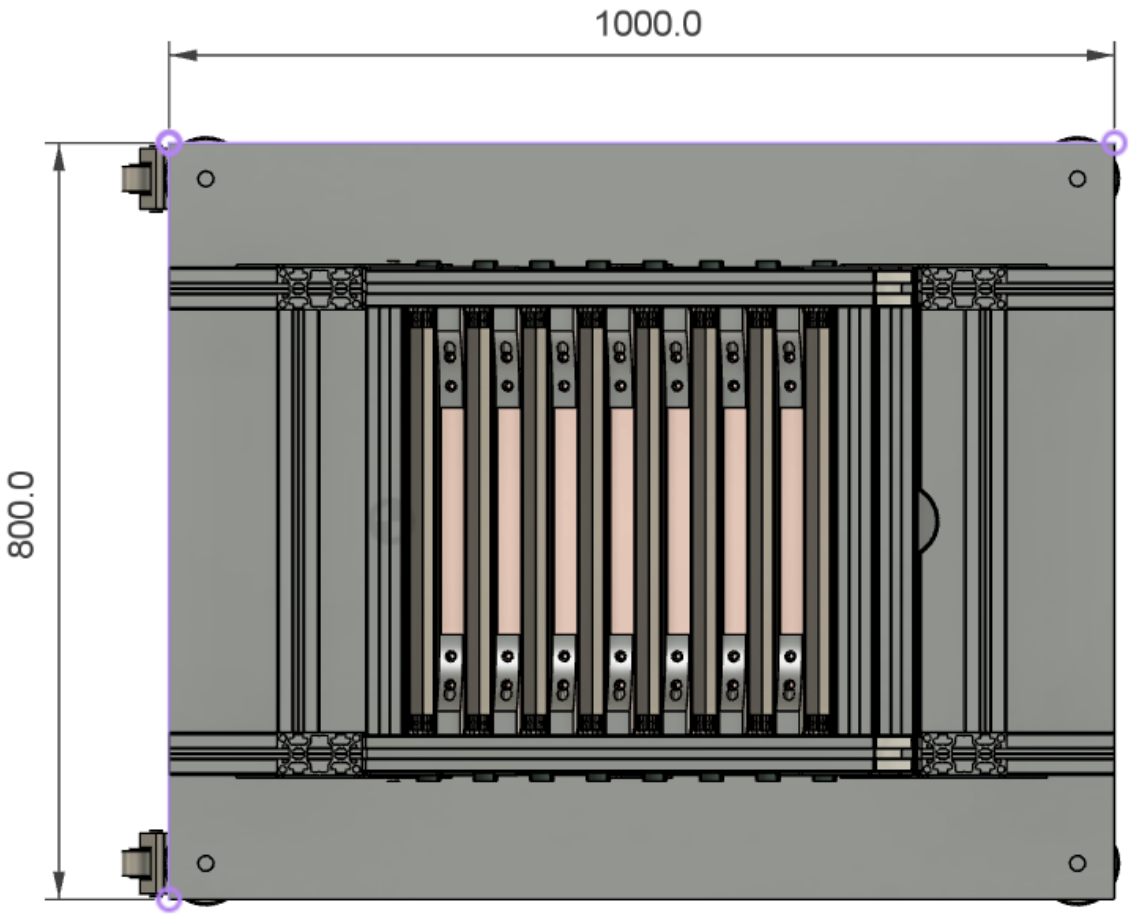

C3
L1
C2
IC1
L2
C4
C2
P1
R1
C1
IC2
C5
C6
C7
C8
J1
IC4_1
C13_1
R3_1
C10_1
R2_1
C8_1
R6_1
C12_1
R4_1
C11_1
IC5
C14
IC6
C19
R11
R12

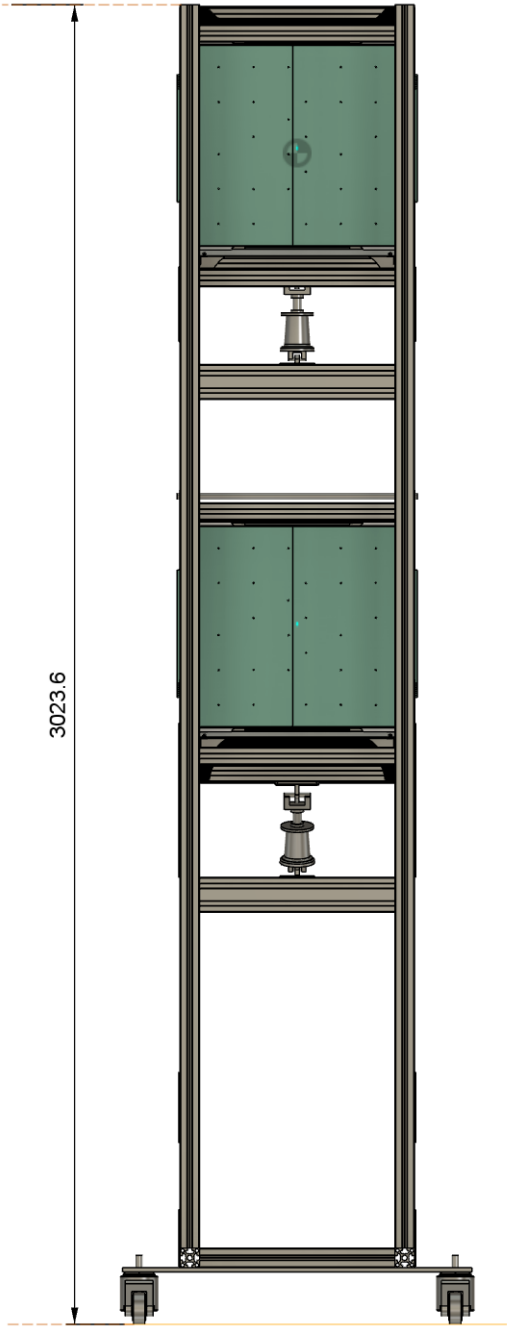
# HGND support structure

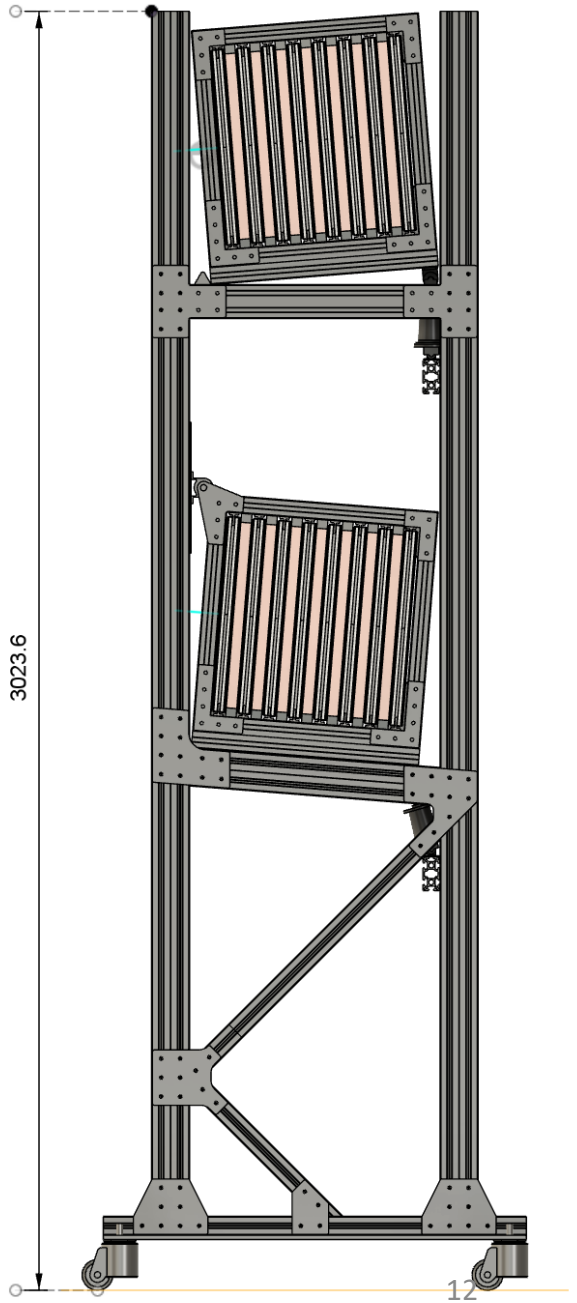



- Support structure allows for:
  - Lateral movement of the detector
  - Height adjustment
  - Angle adjustment
  - Adjustment of the distance between blocks
- Total weight: ~800 kg

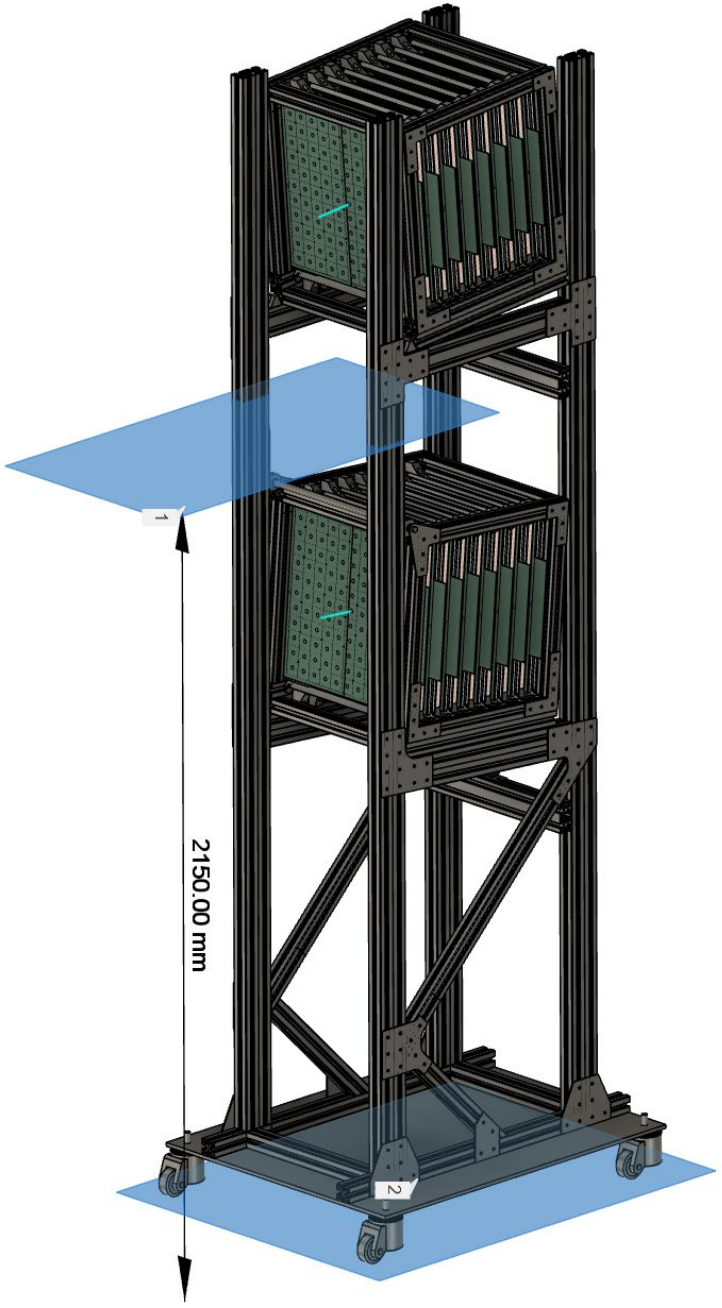
# HGND support structure



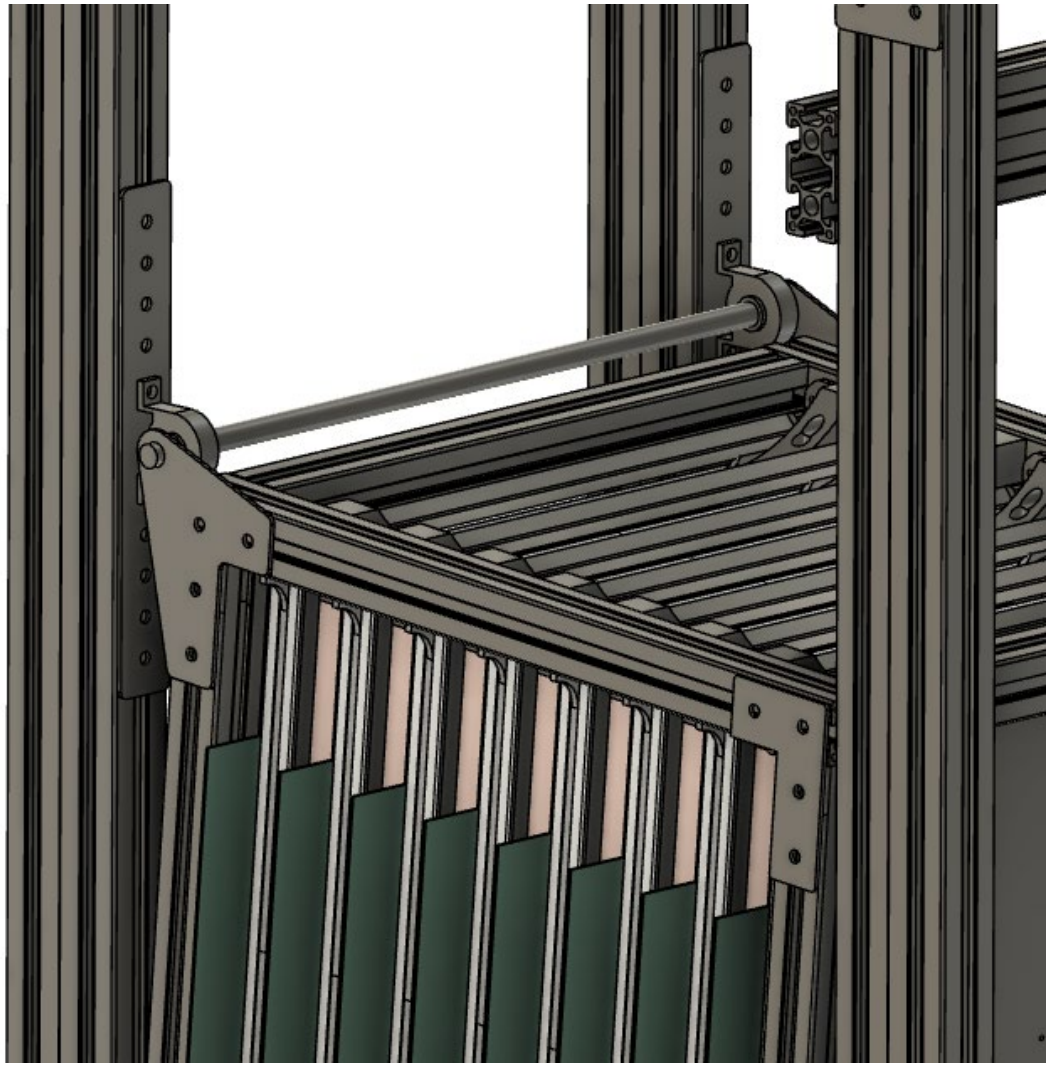



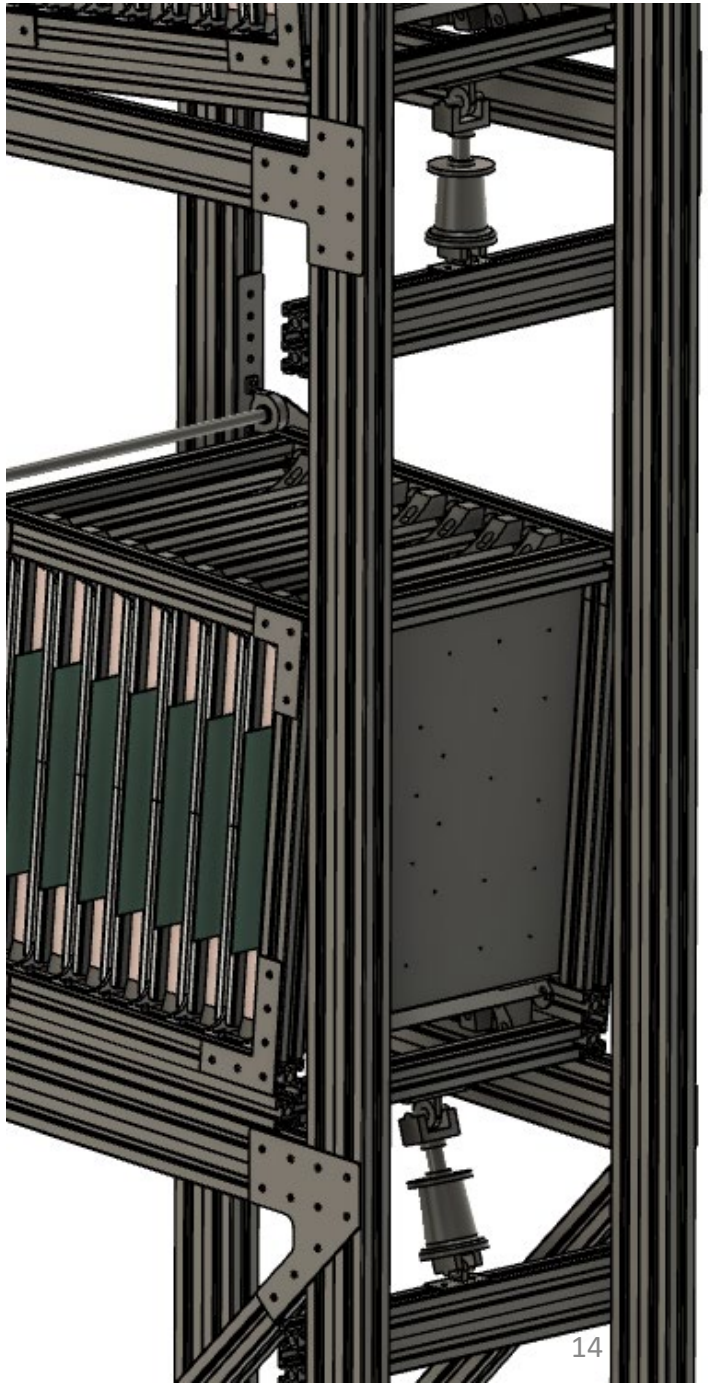



# HGND support structure



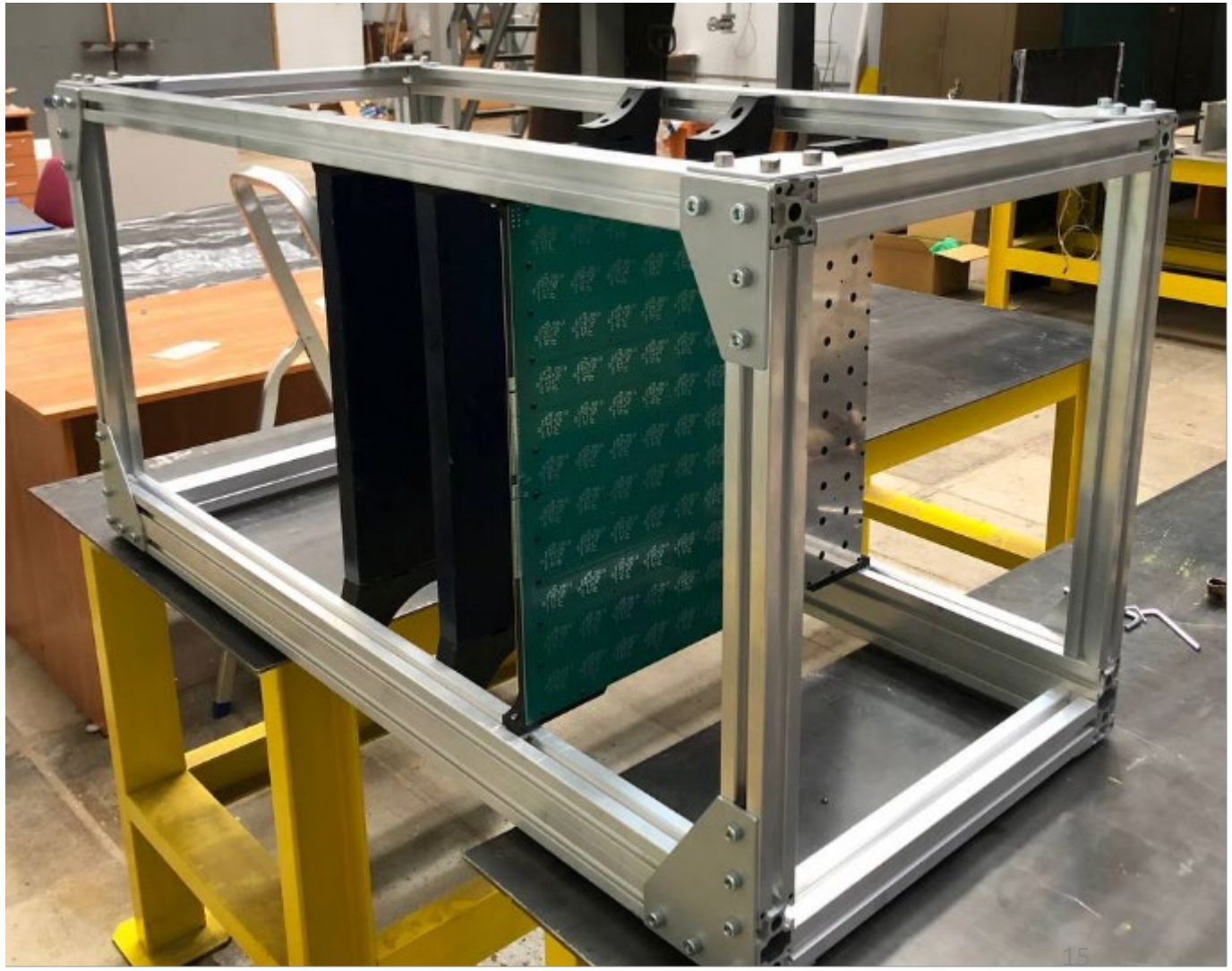
# HGND support structure





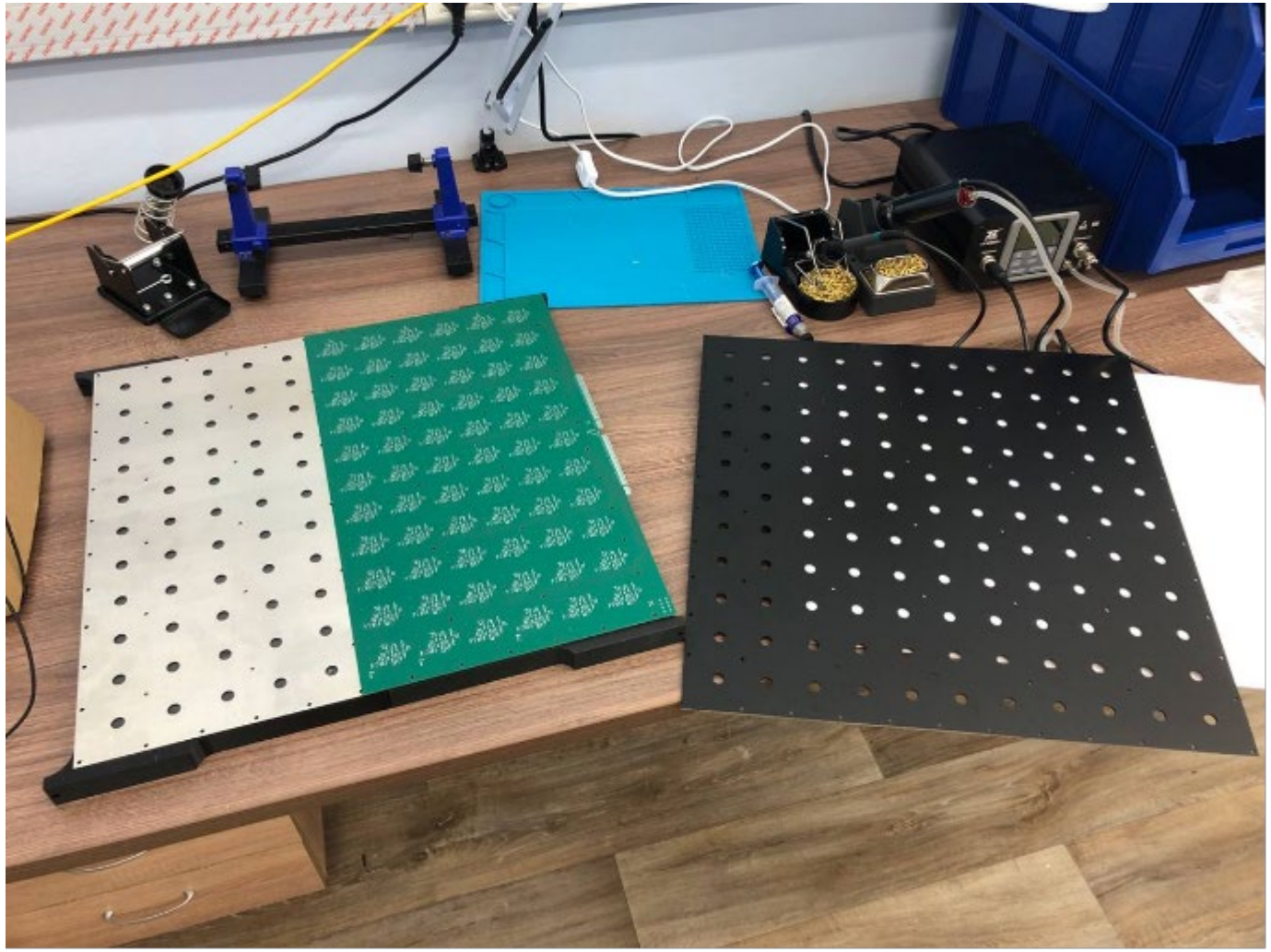
# HGND mechanical mock-up

- A mock-up of the HGND block has been assembled at INR
- Mock-up allows to test:
  - Loading-unloading of the converters using hoists
  - Mounting-unmounting of the detector layers
  - Framing deformation and sag under load



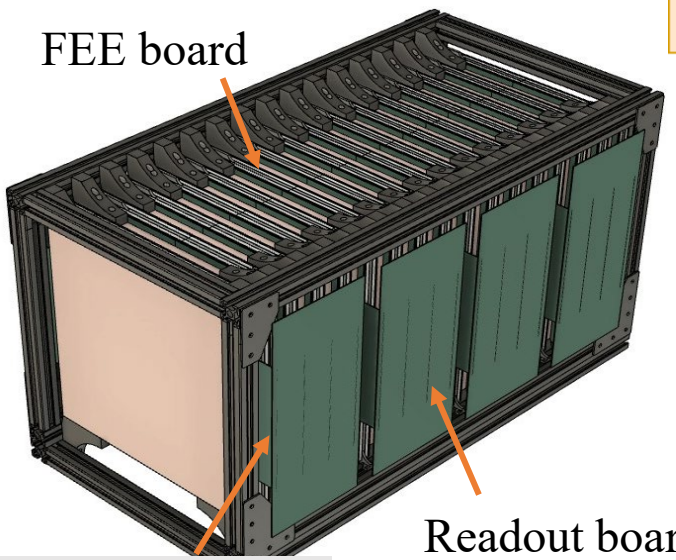
# HGND test assembly

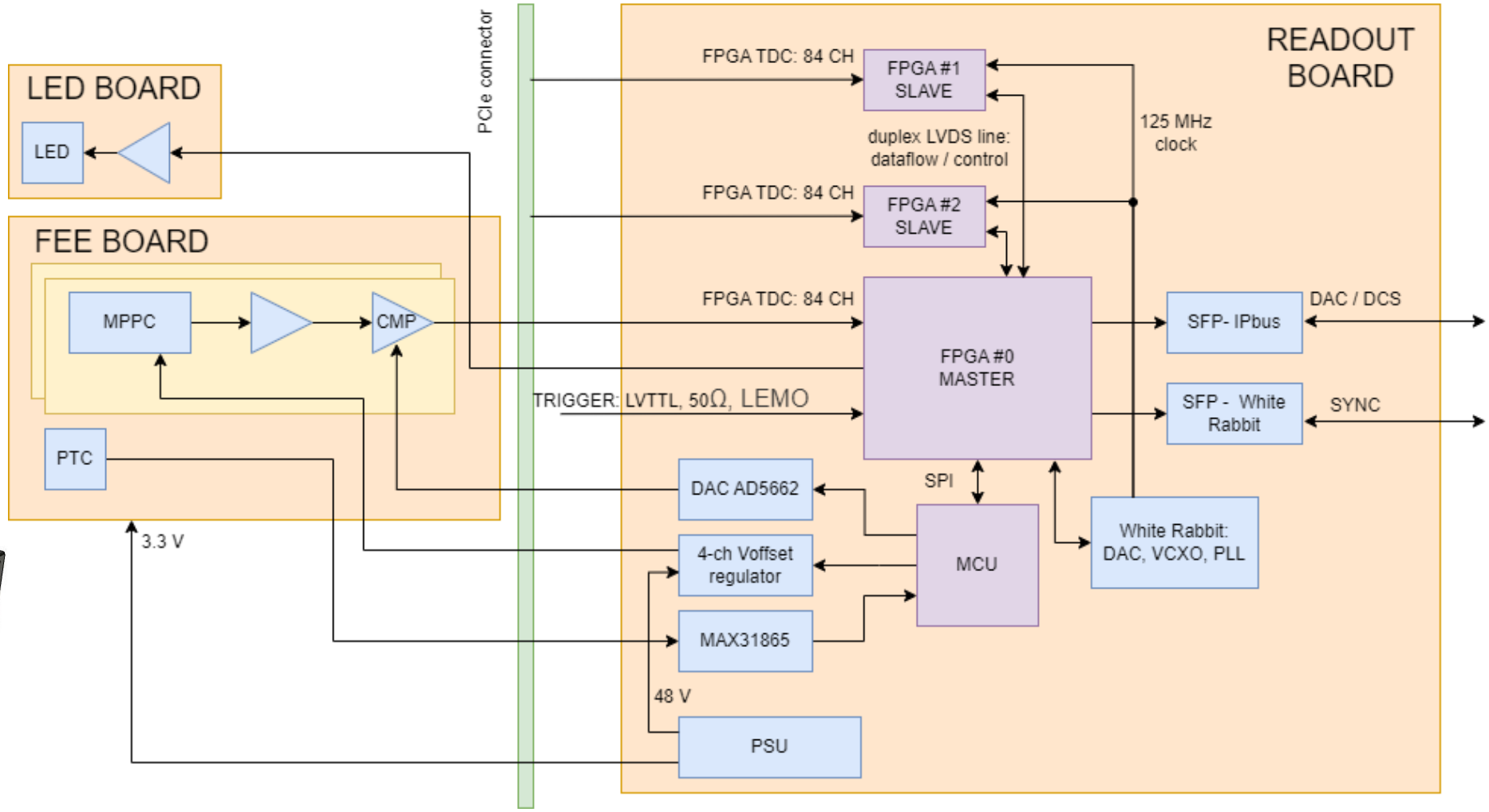
- A prototype of the FEE board is under assembly
- A prototype of the LED board is under assembly
- A prototype case for the detector layer is completed
- The mockup is ready and all assembly operations have been checked.
- The support structure is in production.



# FEE & readout architecture

- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total



# Readout & trigger

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip (2000 total)
- ***White Rabbit*** (WR) is used for event's time synchronization (8 links total):
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events

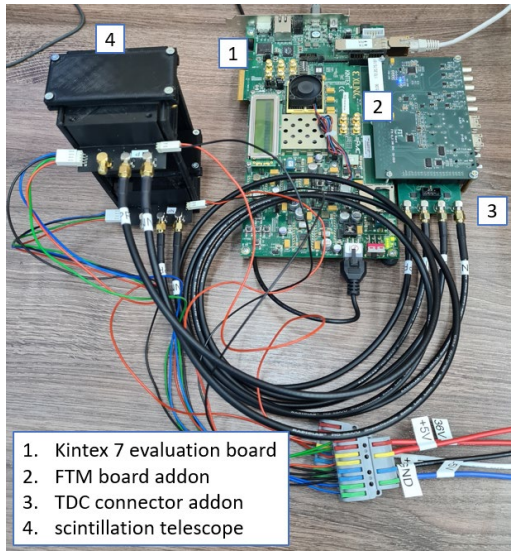
- Ethernet UDP protocol (***IPbus*** [1]) is used for data forwarding and board control
- Local network connect readout boards (8 ethernet links) with FLP

- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit per link is not exceed ***100 Mbit/s***. ***The continuous readout*** is implemented without busy signal.

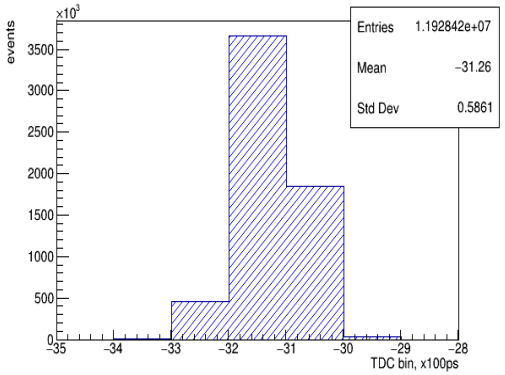
- The trigger is processed on FLP site:
  - Trigger signal is connected to TDC channel and digitized with WR timestamp in FPGA
  - Message trigger accompanied by a timestamp is transmitted to FLP for event selection

[1] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, ***IPbus: a flexible Ethernet-based control system for xTCA hardware***, *JINST 10 (2015) no.02, C02019.*

# HGND readout proto_v2



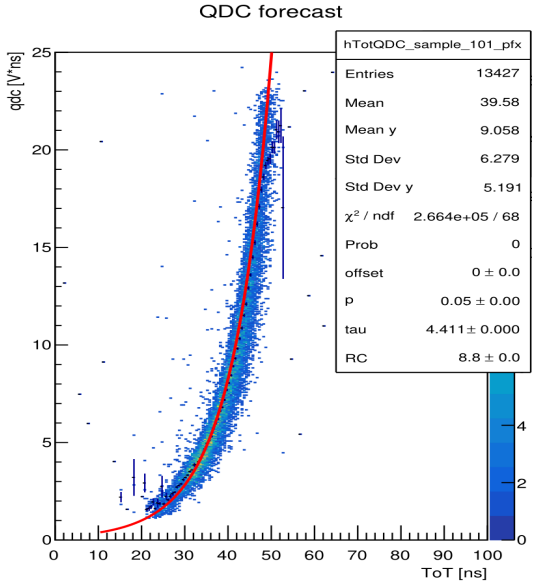

The 2-channels TDC prototype V1 connected to HGND scintillator cells telescope



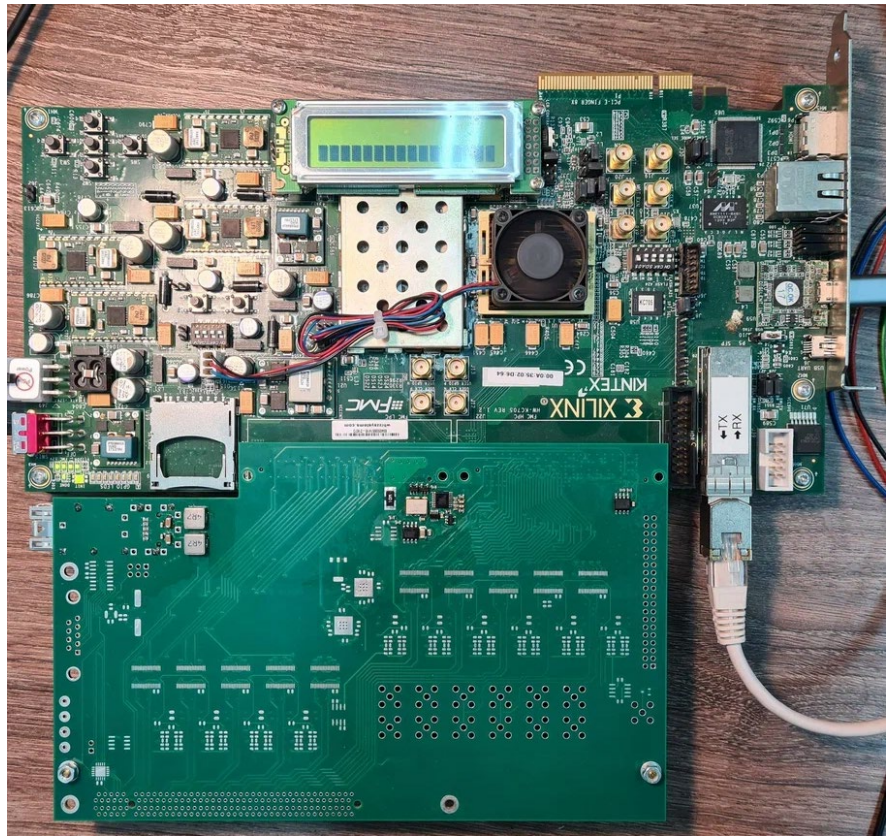

The RMS of single TDC channel is 42ps. Measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).

- The 100 ps FPGA TDC is designed and tested with pulse generator, cosmic muons and e⁻ test beam [2].
- The readout bord prototype V2 is designed and assembled (White Rabbit)

- 33 channels via PCIe + 6 channels via SMA (LEMO)
- 20 GPIO pins (debug + trigger)
- White Rabbit facility
- MCU functional: threshold comparator control, PTC sensor.




TOT amplitude resolution is in range 14 - 22%



The readout board prototype V2:
** The only setup currently soldered on the board is the White Rabbit configuration.*

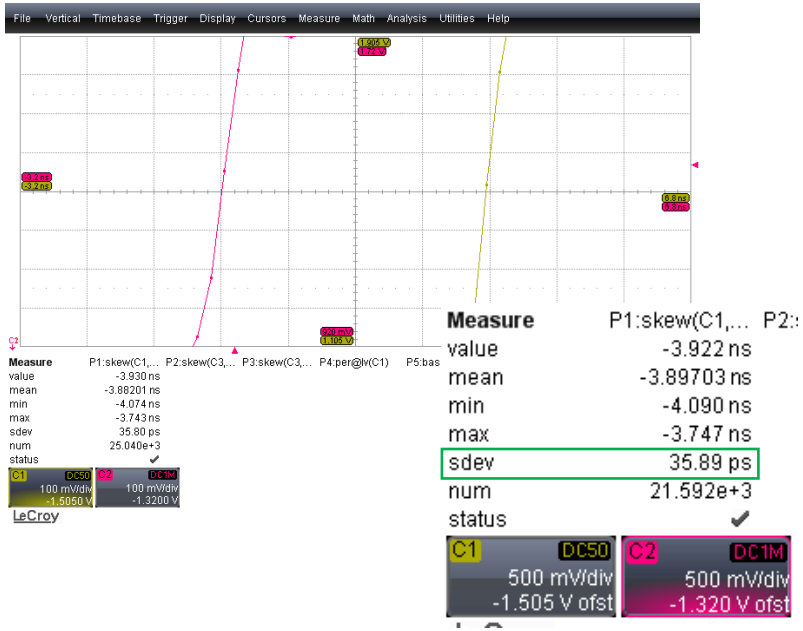

[2] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutro Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.16895.*

# HGND readout proto_v2 WR tests at JINR (16 – 17 of April)

HGND readout proto_v2 connected to WR master at JINR

WR TX clocks 62.5 MHz:
orange – WR master; pink – WR slave (hgnd)


Clock sync jitter ~35ps (measure on FPGA output buffers)



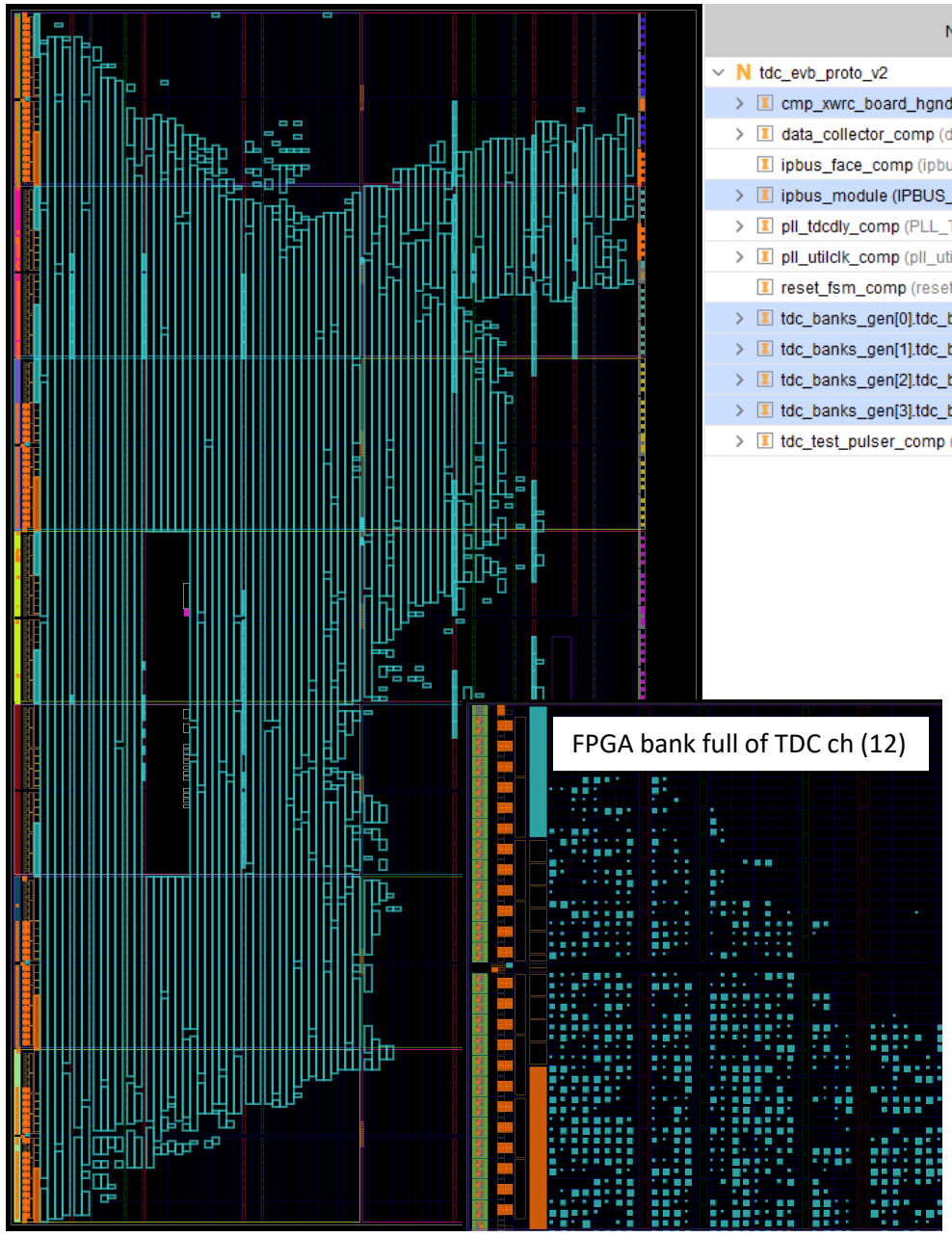

WR tests at JINR conclusions:

- WR synchronization works
- Tx timestamp error (reason found: generic fifo synthesis bug)
- EEPROM not works (fixed – I2C wires swapped)

Next steps June - July:

- WR error fix +  project modification (mmcm replacement with pll)
- Combining WR + Ipbus + TDC FPGA modules
- 33 channels TDC tests
- Next round of WR tests at JINR

# 39 TDC + WR + IPbus FPGA design




| Name | Slice LUTs (203800) | Slice Registers (407600) | Block RAM Tile (445) | Slice (50950) | LUT as Logic (203800) | LUT as Memory (64000) | IBUFDS (480) | GTXE2_CHANNEL (16) | BUFGCTRL (32) | BUFHCE (168) |
|---|---|---|---|---|---|---|---|---|---|---|
| tdc_evb_proto_v2 | 51768 | 71169 | 106 | 23849 | 51676 | 92 | 157 | 2 | 23 | 5 |
| cmp_xwrc_board_hgnd (xwrc_board_afi_hgnd) | 4776 | 4838 | 39.5 | 2015 | 4768 | 8 | 0 | 1 | 6 | 0 |
| data_collector_comp (data_collector) | 678 | 194 | 30 | 343 | 678 | 0 | 0 | 0 | 0 | 0 |
| ipbus_face_comp (ipbus_interface) | 3204 | 10681 | 0 | 4037 | 3204 | 0 | 0 | 0 | 0 | 0 |
| ipbus_module (IPBUS_basex_infra) | 12015 | 5023 | 17 | 4217 | 11931 | 84 | 0 | 1 | 3 | 5 |
| pll_tdcdly_comp (PLL_TDCDLY) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| pll_utilclk_comp (pll_utilclk) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| reset_fsm_comp (reset_fsm) | 49 | 52 | 0 | 28 | 49 | 0 | 0 | 0 | 0 | 0 |
| tdc_banks_gen[0].tdc_bank_comp (tdc_bank) | 7237 | 11617 | 4.5 | 4161 | 7237 | 0 | 36 | 0 | 2 | 0 |
| tdc_banks_gen[1].tdc_bank_comp (tdc_bank__parameterized1) | 7192 | 11617 | 4.5 | 3693 | 7192 | 0 | 36 | 0 | 2 | 0 |
| tdc_banks_gen[2].tdc_bank_comp (tdc_bank__parameterized3) | 7067 | 11617 | 4.5 | 3955 | 7067 | 0 | 36 | 0 | 2 | 0 |
| tdc_banks_gen[3].tdc_bank_comp (tdc_bank__parameterized5) | 9477 | 15442 | 6 | 5398 | 9477 | 0 | 48 | 0 | 2 | 0 |
| tdc_test_pulser_comp (tdc_test_pulser) | 71 | 70 | 0 | 47 | 71 | 0 | 0 | 0 | 1 | 0 |

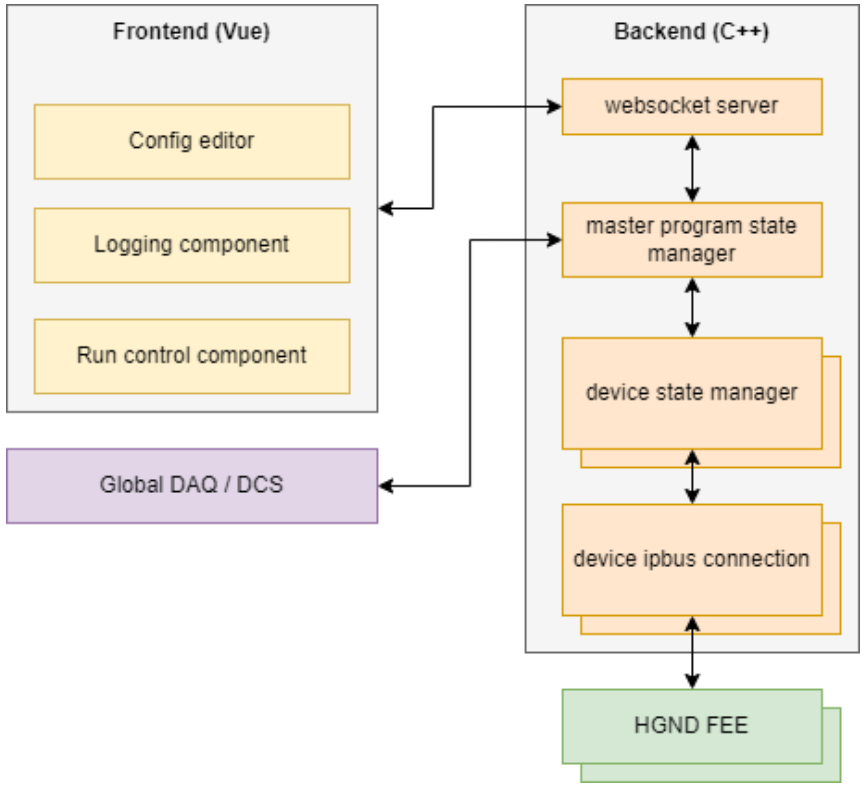
- 39 TDC FPGA design was prepared
- Now xc7k325 is used (EvB – 10 banks), xc7k160 will be used on readout board
- xc7k160 has 8 banks: 7 * 12 = 84 TDC channels + 1 bank for utilities

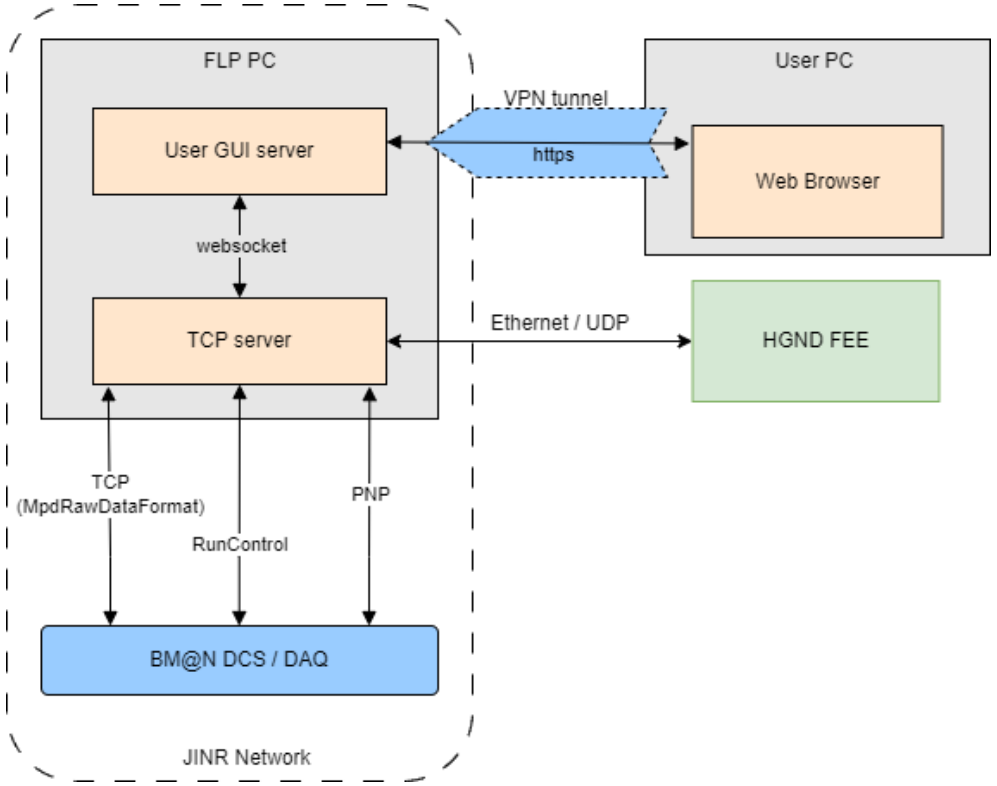
- TDC pairs routing per bank in sequential and mixed pattern will be tested
- TDC + WR + IPbus design prove of the concept will be shown

# HGND readout board routing status:

- ✓ Front-End connectors pinout and schematic
- ✓ White Rabbit periphery schematic
- ➢ Board geometry and connector positions (May 2024)
- ❑ Power supply schematic (June-July 2024)
- ❑ TDC tests with prototype v2 (June – July 2024)
- ❑ FPGA pinout and schematic (June-July 2024)
- ❑ Board routing (August-September 2024)

# The topology of the DCS & readout software

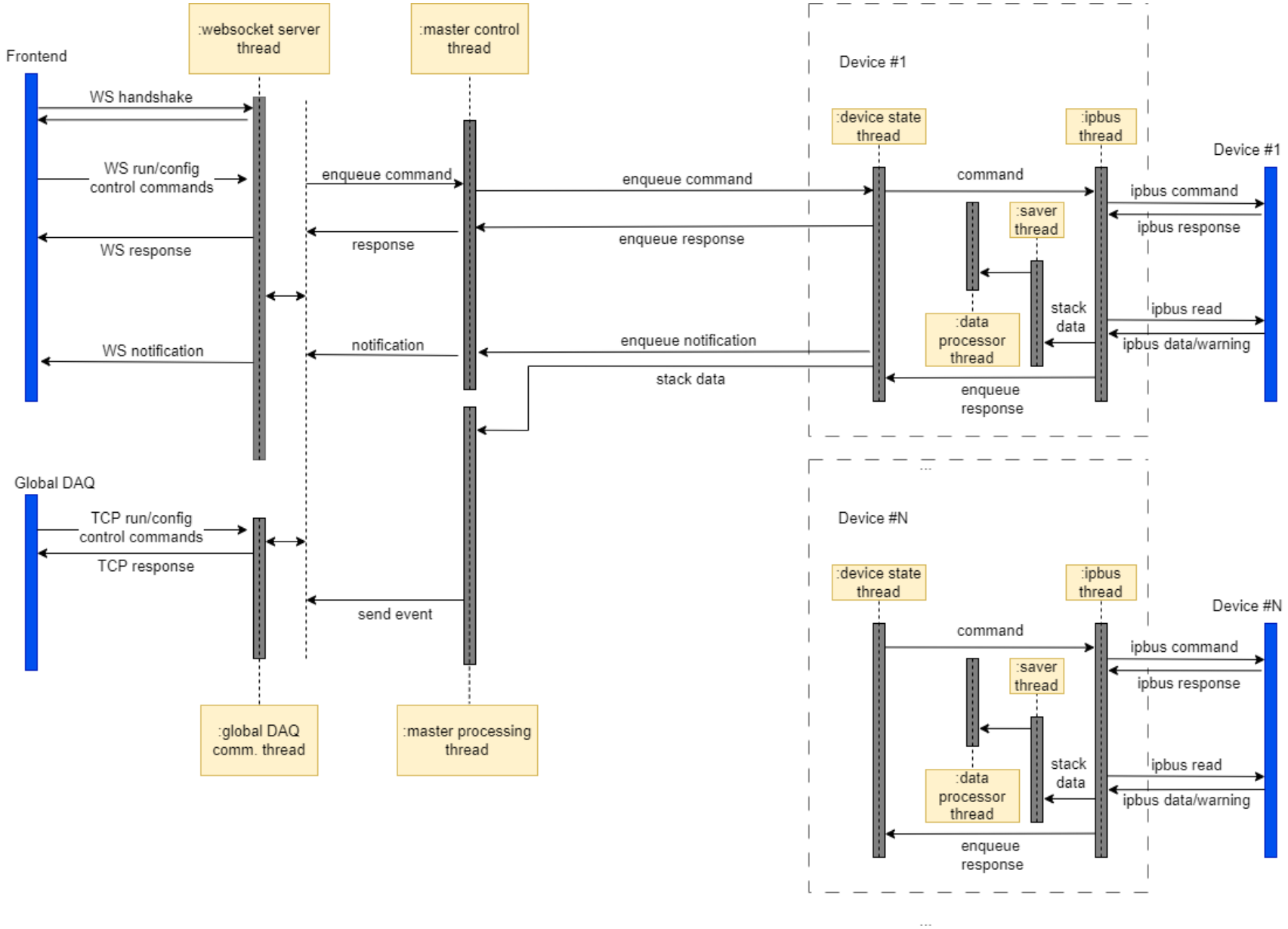



- The detector control system consists of 2 independent modules: frontend and backend
- The backend is a C++ server running on a DCS computer in the same network with detectors.
- The server part provides write/read operations to the detectors via an IPBus connection to the control and data acquisition board.

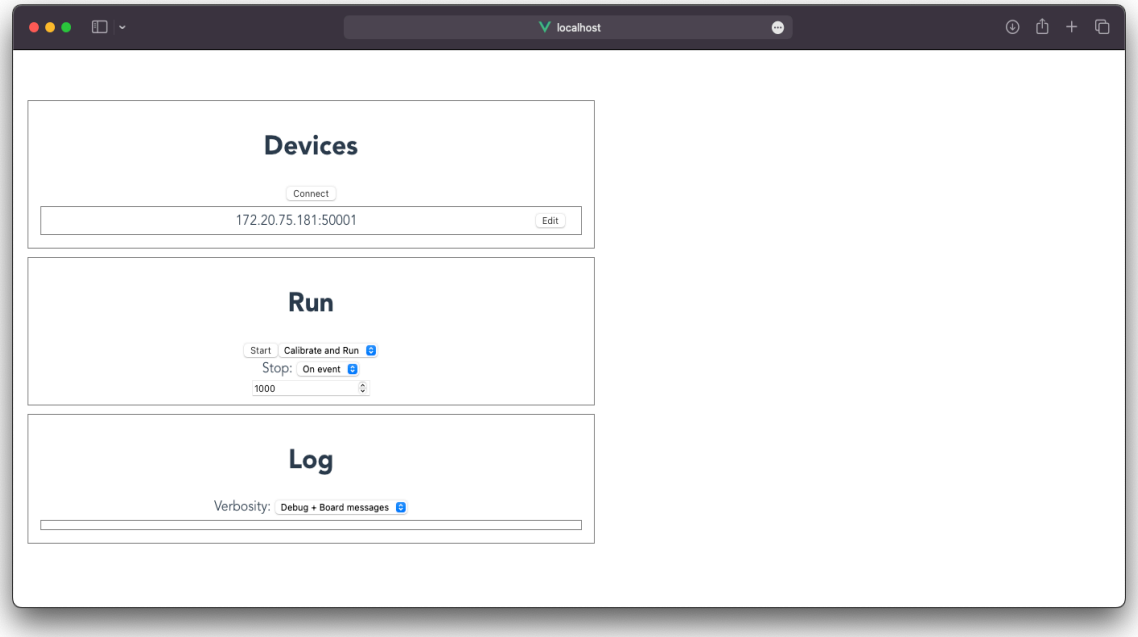
- Frontend is the user interface for this backend. It can be implemented in various ways; the key parameters are reactivity and an ability to establish a connection via websocket with the server part.
- The current version is the Vue web application (open-source JavaScript framework).
- The interface can be run either on the DCS computer or on the operator's computer, provided that the port is available.

# The threading scheme of a C++ backend



# HGND readout & DCS readout test setup

HGND proto_v2 and EvB connected to gigabit switch for readout tests




HGND DAQ & DCS GUI current view

**Synthetic tests for proving the concept of developed software architecture**

- ✓ Data & trigger FPGA emulator
- ✓ 400 Mbit/s data readout per board (100 Mbit is required)
- ✓ 800 Mbit/s readout rate with 2 boards was achieved (is the estimated rate for HGND with 8 links)
- ✓ Data sorting by trigger selection with two links readout: data rate 2.6 MHz (10 kHz/channel), trigger rate 10kHz.
- ➢ Data flow (soft emu) & DCS commands test on BM@N FLP
- ❑ Next: Preparing software for TDC tests

# Conclusions

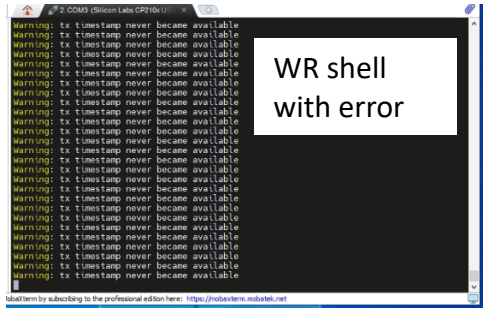
- Status of the FEE & support structure
  - A prototype of the FEE board is under assembly
  - A prototype of the LED board is under assembly
  - A prototype case for the detector layer is completed
  - The mockup is ready and all assembly operations have been checked.
  - The support structure is in production.

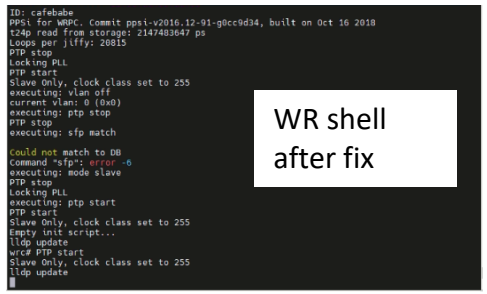
- Status of the readout board development:
  - The White Rabbit setup was tested at JINR: Clock synchronization works but the timestamp synchronization failed, reason found, required new test
  - June – July 2024: TDC tests with 33 channels (time scan, pulser, cosmic)
  - Working on the design of the full scale readout board: board routing (August -September 2024)

- The DCS & readout software:
  - Required throughput was achieved
  - Data sorting tests was performed
  - Working on software integration tests (FLP at BM@N)
  - June – July: Using software readout & control for TDC tests

Thank you for your attention!

# BACKUP



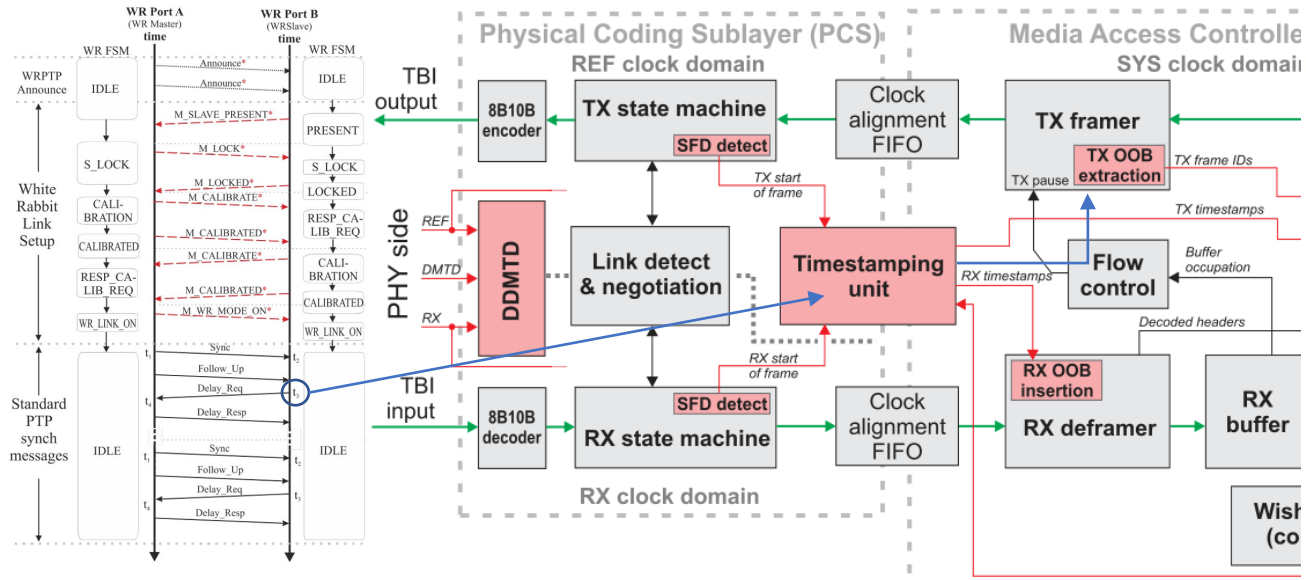




Figure 21: White Rabbit PTP extension

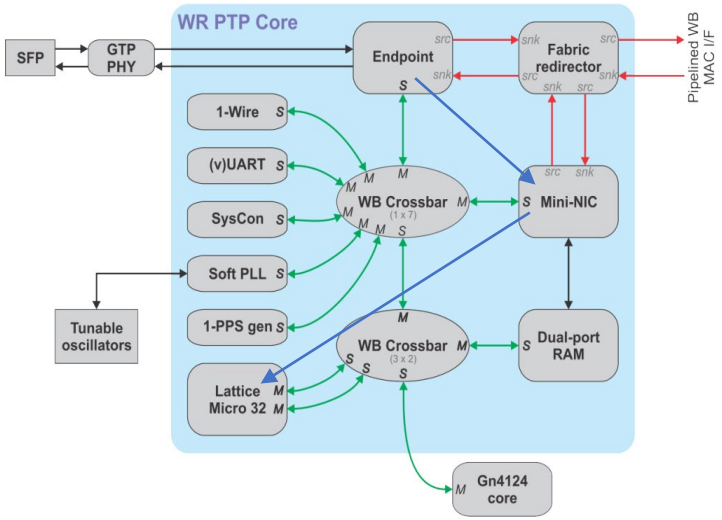
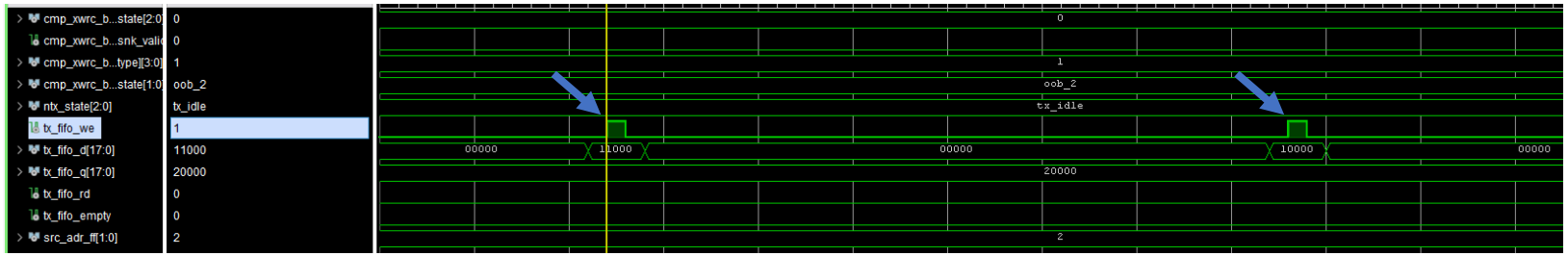
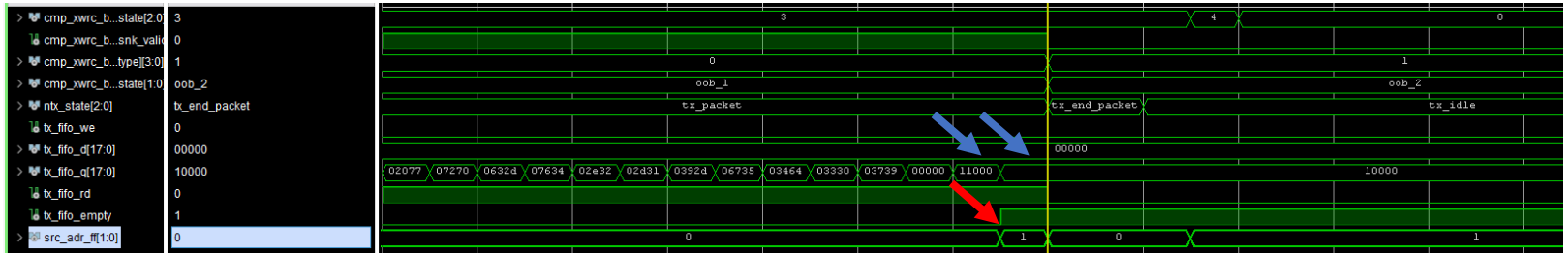



Figure 23: White Rabbit PTP Core block diagram

- TX timestamps is sent with two OOB packets
- LM32 request 2 OOB packets for reading TX timestamp: packets addr 11000 and 10000:

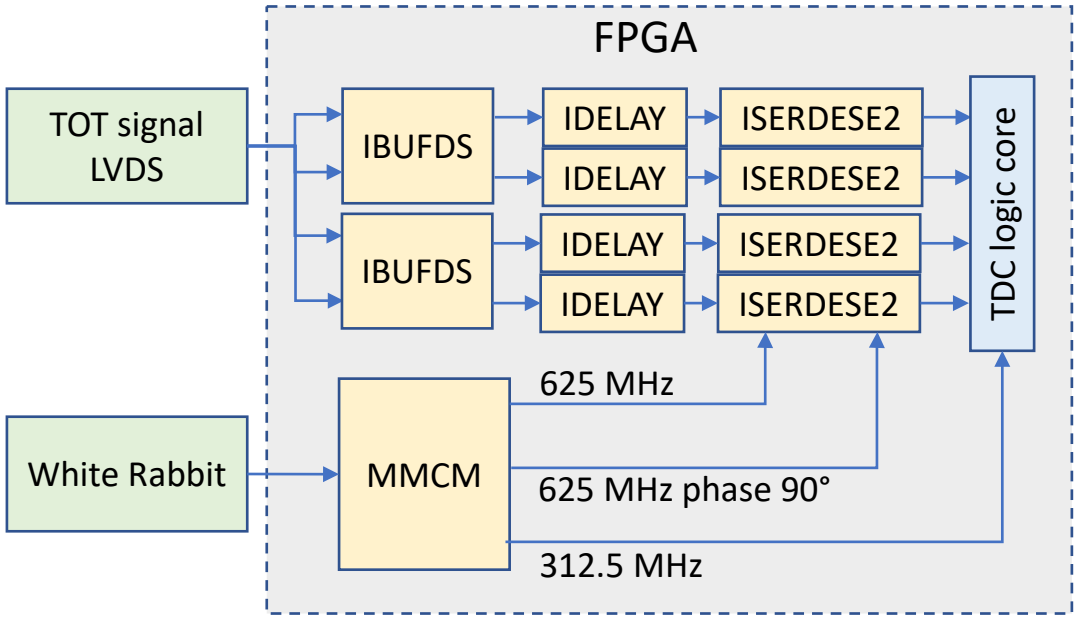



- While reading two OOB packets in 'TX framer' fifo rise empty one cycle early
- latching fifo_empty signal for one cycle mitigates the error

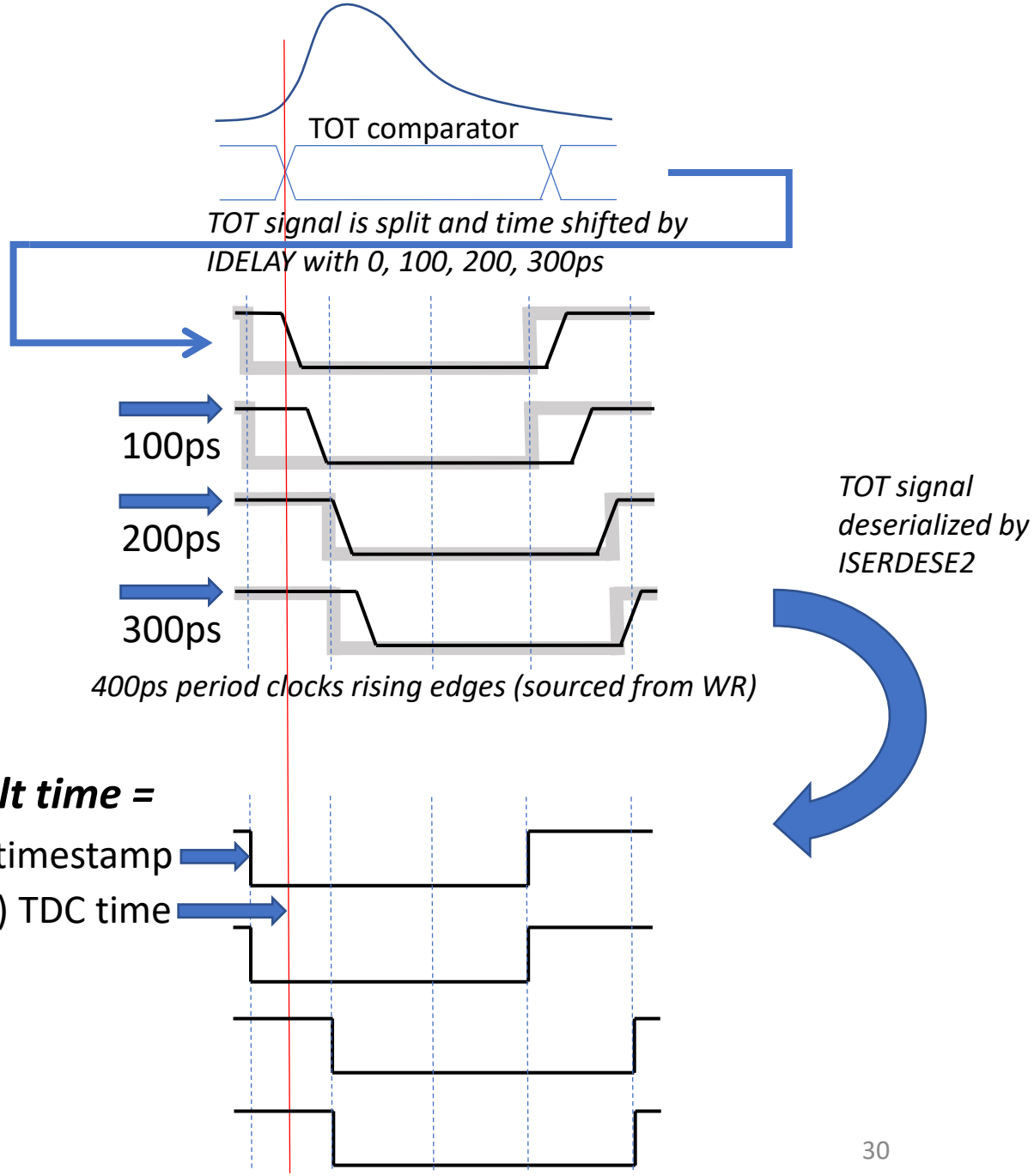



- Module wr-cores\modules\wr_endpoint\ep_tx_header_processor.vhd (line 341) send tx timestamp while processing two OOB packets
- OOB packets are requested by LM32. Request is processed by wr-cores\modules\wr_mini_nic\wr_mini_nic.vhd with pushing data to 'TX_FIFO: generic_sync_fifo'.
- This fifo is read in wr_mini_nic while sending packets in ep_tx_header_processor.
- While reading the fifo the empty flag is raised one cycle earlier
- This move FSM to tx_end_packet state and second OOB is not sent
- Tx timestamp is missed because of single OOB packet
- By delaying (latching) fifo_empty by single cycle, mitigates the error "tx timestamp never became available".

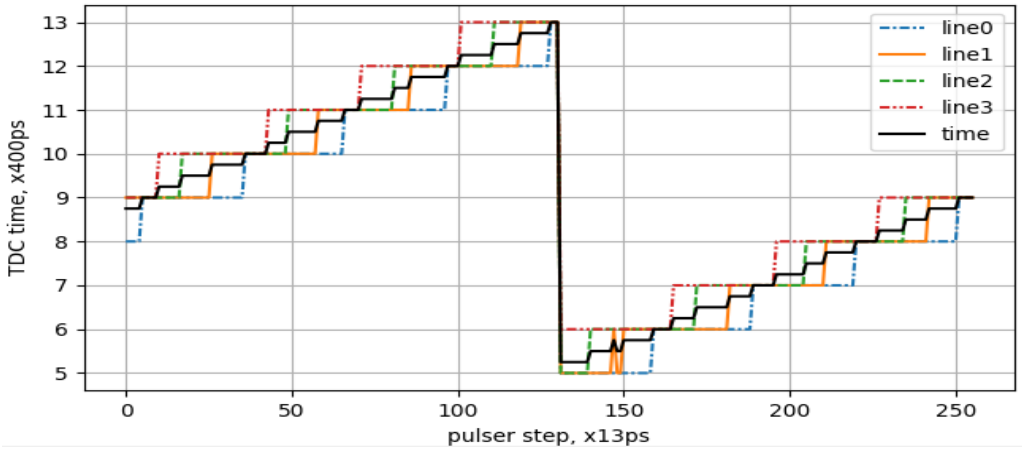
# The 100ps FPGA TDC principle of operation



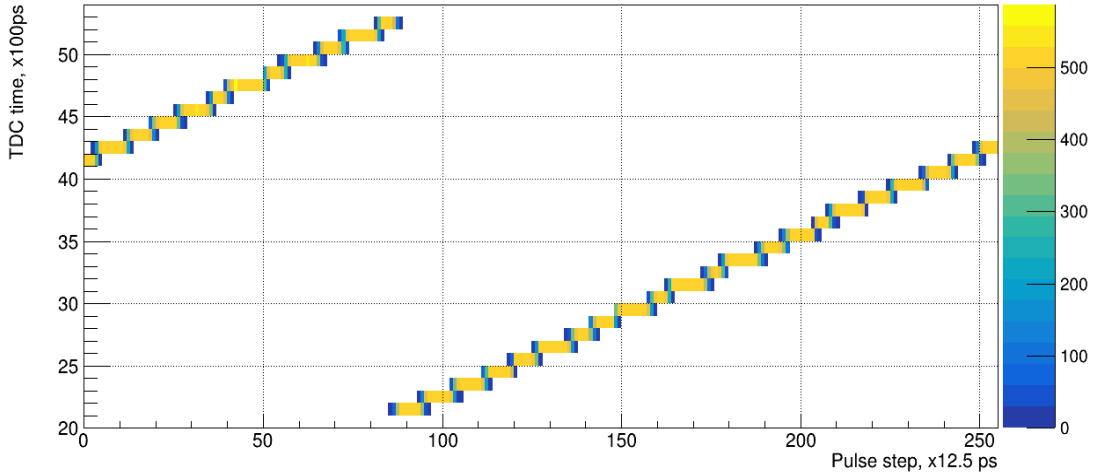

The TDC is based on the Kintex-7 input serial-to-parallel converter with oversampling capability and programmable delay. The design is based on Xilinx recommendations, and uses only documented features of the FPGA within its specifications.



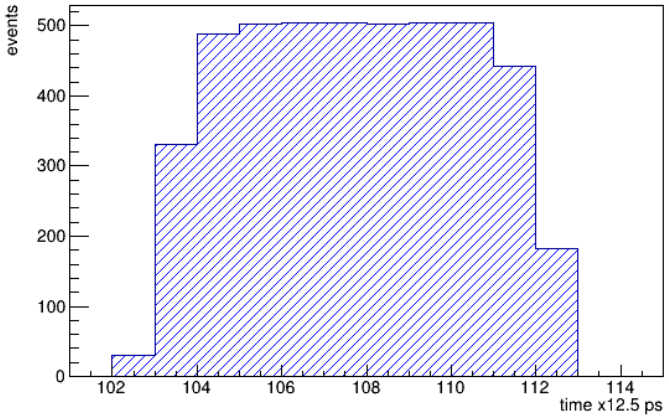
# The FPGA TDC time scan results

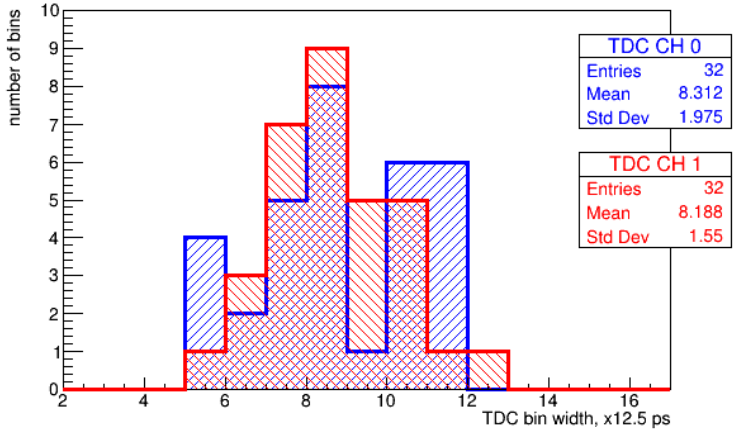



Four TDC lines and the resulting time dependence on the pulse time shift are shown. Pulses are generated by FPGA MMCM synchronously to the TDC clock with a phase step of 12.5ps. The single scan pass was taken with a digital FPGA logic analyzer.

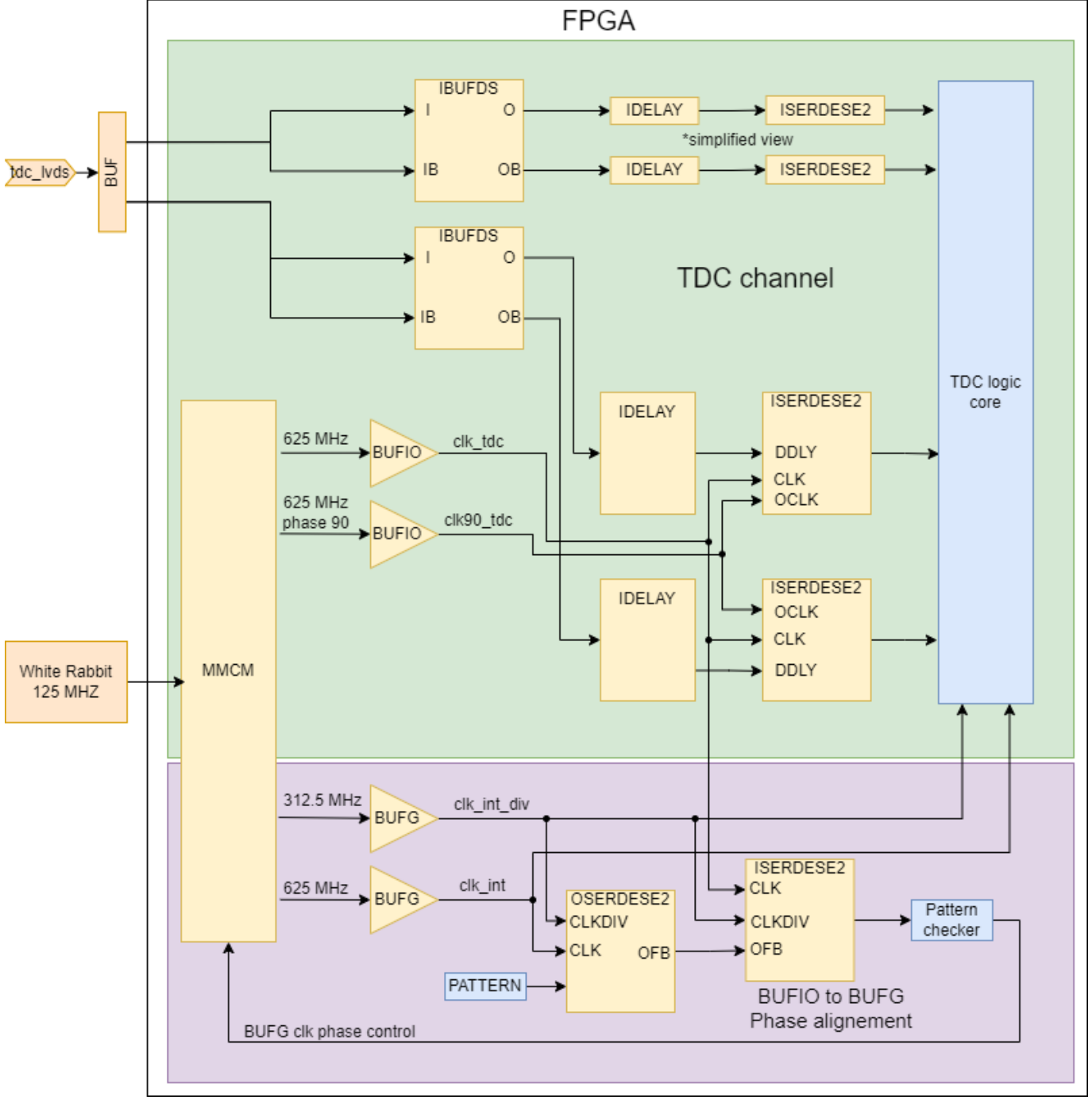


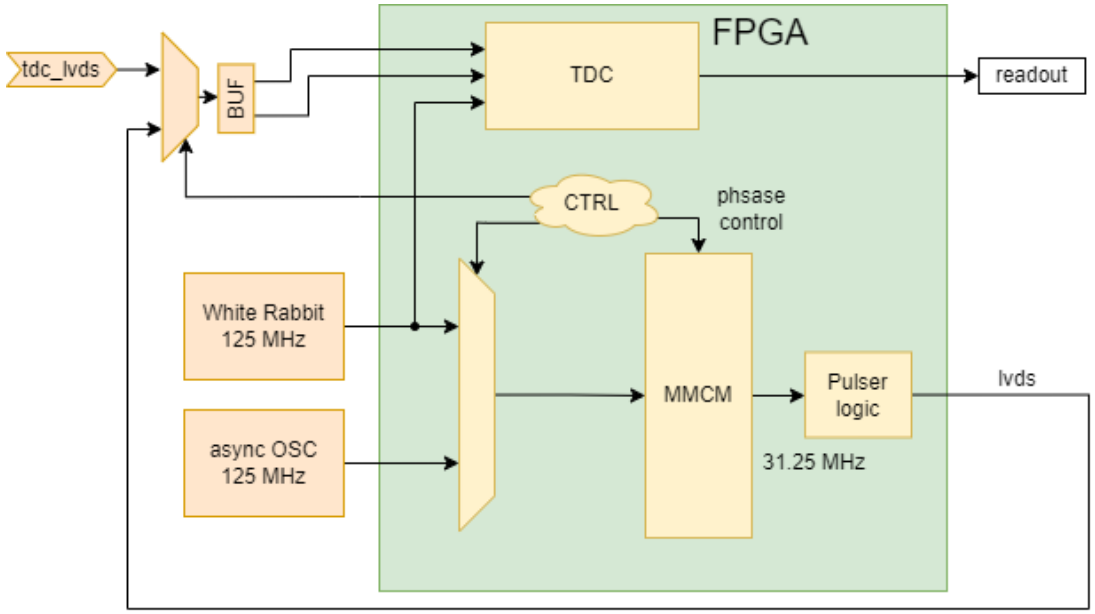

The TDC time dependence on pulse time shift. Pulses are generated by FPGA MMCM synchronous to TDC clock, and the time step is 12.5 ps. Data was taken with PC readout, 1000 events per single time shift step.



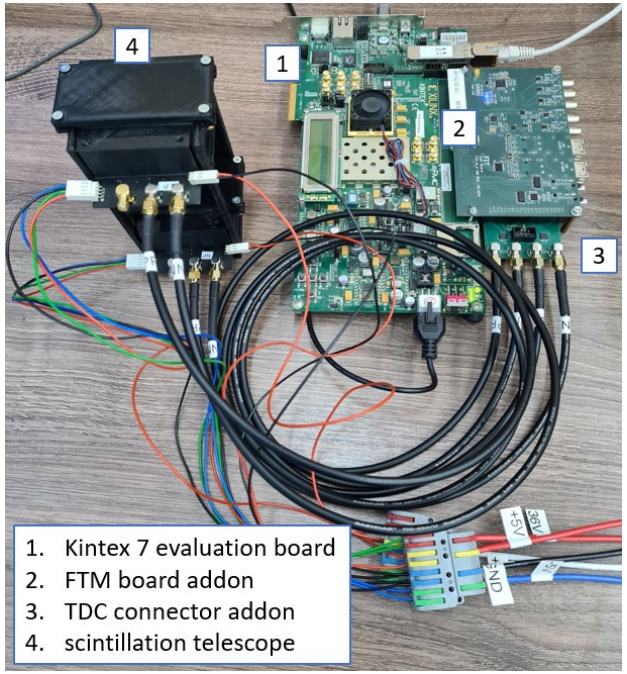




The TDC bin width measured with pulses synchronous to the TDC clock. Left: Typical TDC bin profile taken with a synchronous time scan. Right: The TDC bin width distribution for both TDC channels. The bin width value taken at the amplitude level is 30% in the bin profile. The TDC bin width distribution RMS is ***20 ps***. The main contribution to the TDC bin width distribution is the TDC line delay alignment step of 38.8 ps.


FPGA
tdc_lvds
BUF
IBUFDS
I
O
IB
OB
IDELAY
ISERDESE2
*simplified view
TDC channel
TDC logic core
625 MHz
BUFIO
clk_tdc
625 MHz
phase 90
clk90_tdc
DDLY
CLK
OCLK
White Rabbit
125 MHZ
MMCM
312.5 MHz
BUFG
clk_int_div
clk_int
OSERDESE2
CLKDIV
PATTERN
Pattern
checker
BUFIO to BUFG
Phase alignement
BUFG clk phase control

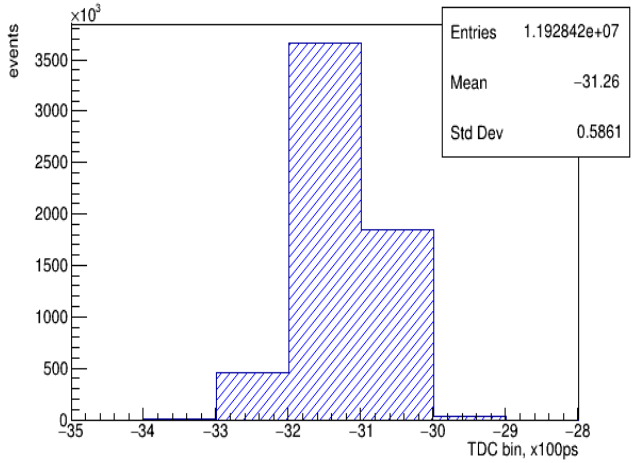

tdc_lvds
BUF
FPGA
TDC
readout
CTRL
phsase
control
White Rabbit
125 MHz
async OSC
125 MHz
MMCM
Pulser
logic
lvds
31.25 MHz

# The FPGA TDC test results



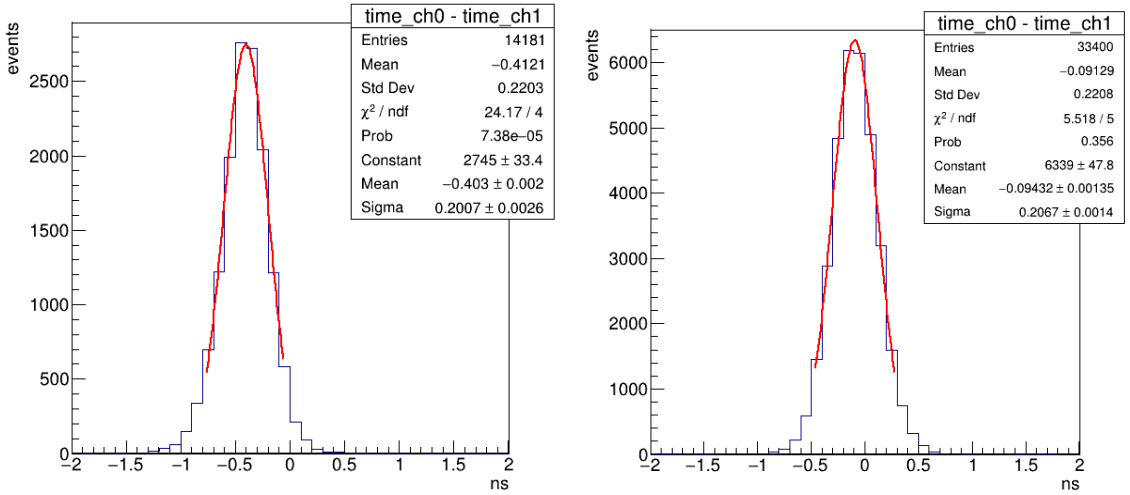

HGND scintillator cells telescope is connected to 2-channels TDC prototype based on KC705 evaluation board

The time difference distribution between two FPGA TDC channels measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).




The RMS of single TDC channel is 42ps.

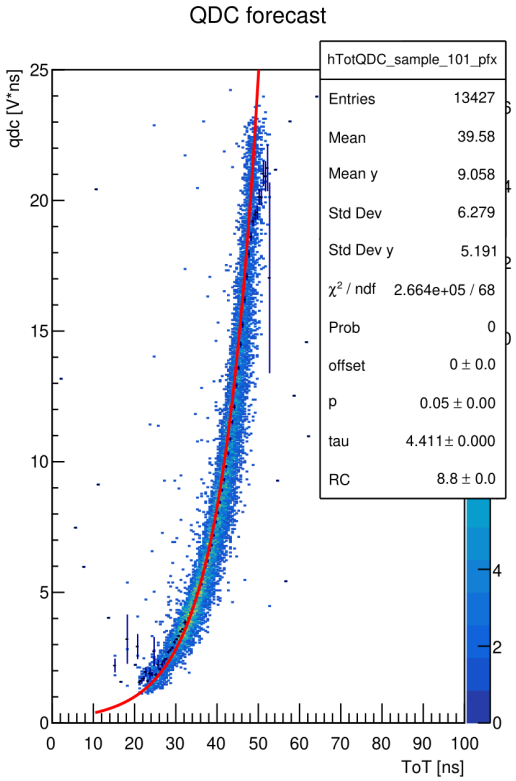
The time resolution measurements with the FPGA TDC prototype board were performed with the 280 MeV electron beam on the “Pakhra” synchrotron in LPI (Moscow, Russia).

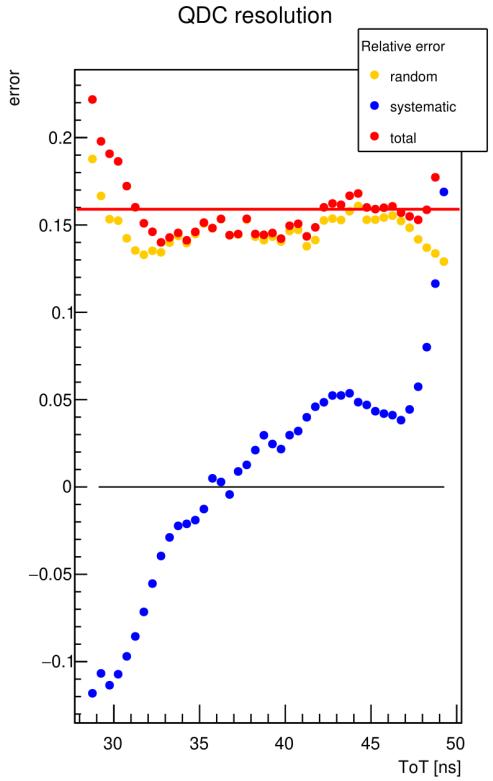


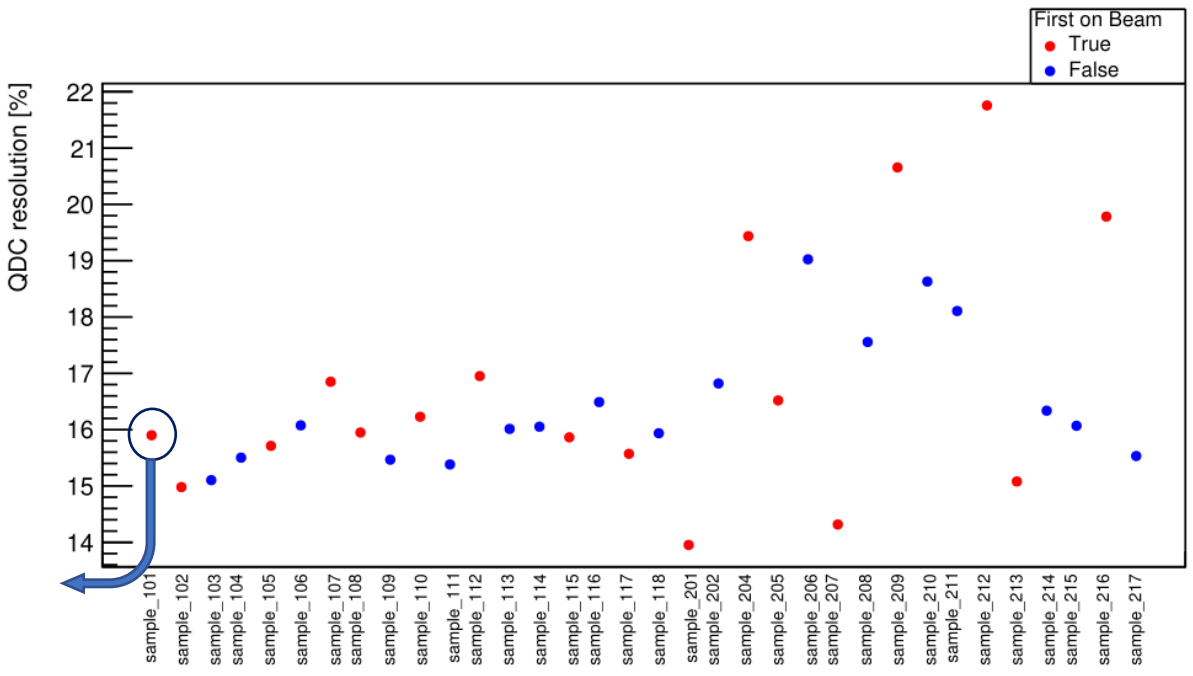

The time difference distributions of two cells of the telescope measured with the CAEN digitizer (left) and the FPGA TDC prototype board (right). Time resolution is ***146 ps*** per single HGND channel.

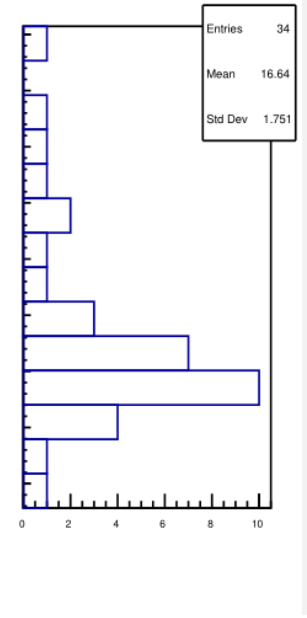

[2] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

# TOT amplitude resolution is in range 14 - 22%

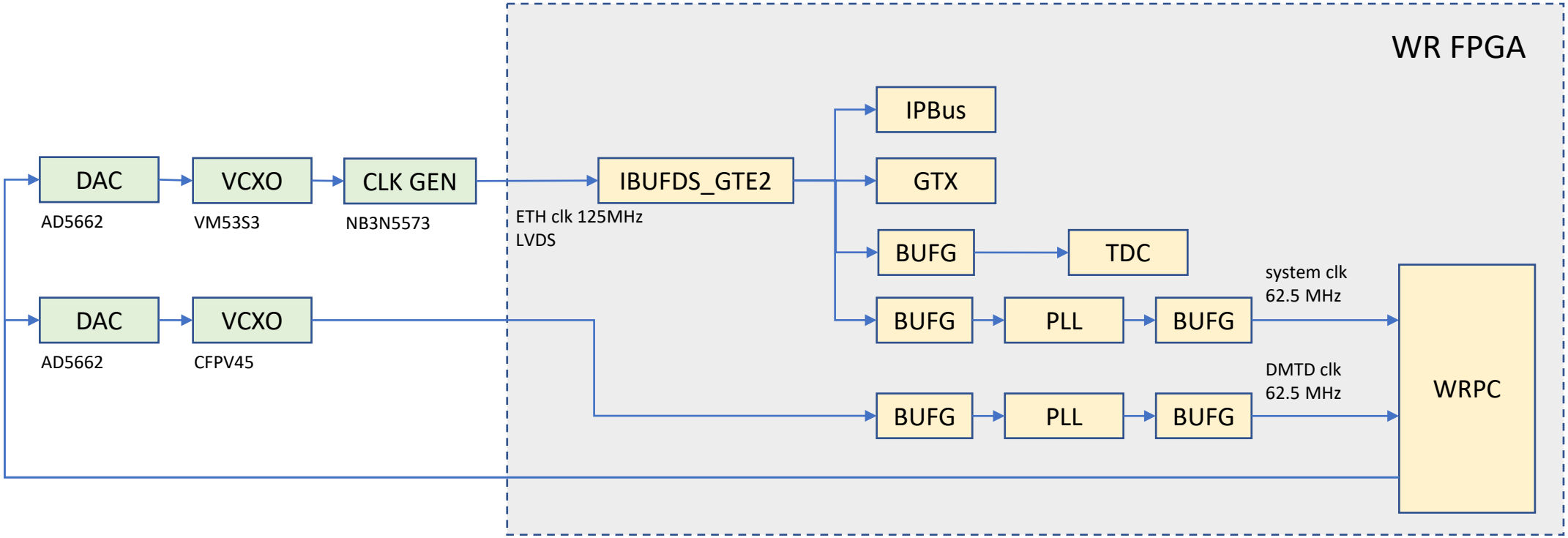


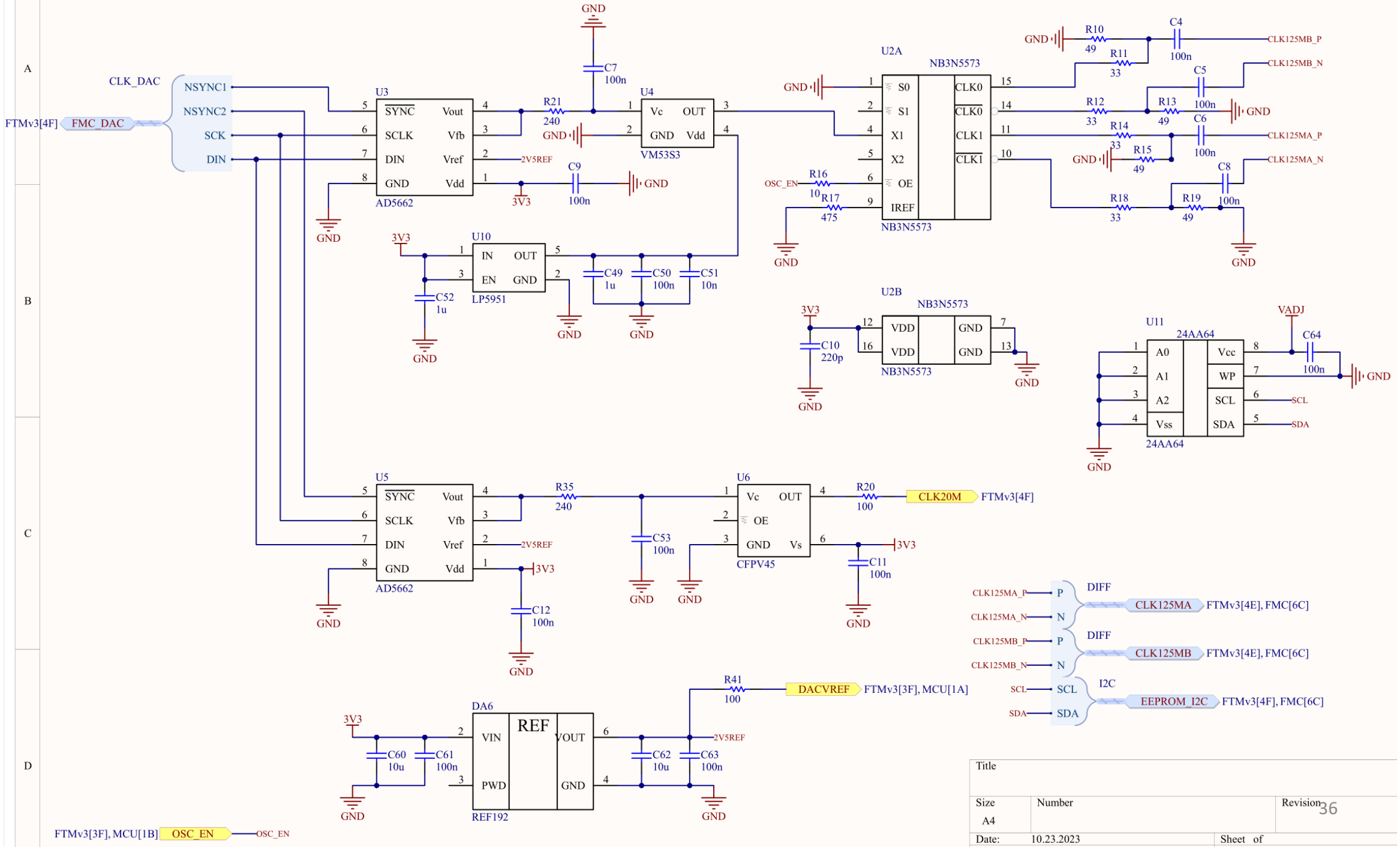



# The White Rabbit implementation




CLK_DAC
FTMv3[4F]
FMC_DAC
NSYNC1
NSYNC2
SCK
DIN
U3
AD5662
SYNC
SCLK
DIN
GND
Vout
Vfb
Vref
Vdd
2V5REF
3V3
R21
240
C7
100n
C9
100n
U4
VM53S3
Vc
GND
OUT
Vdd
U10
LP5951
IN
EN
OUT
GND
C52
1u
C49
1u
C50
100n
C51
10n
U2A
NB3N5573
S0
S1
X1
X2
OE
IREF
CLK0
CLK0
CLK1
CLK1
OSC_EN
R16
10
R17
475
R10
49
R11
33
R12
33
R13
49
R14
33
R15
49
R18
33
R19
49
C4
100n
C5
100n
C6
100n
C8
100n
CLK125MB_P
CLK125MB_N
CLK125MA_P
CLK125MA_N
U2B
NB3N5573
VDD
VDD
GND
GND
C10
220p
U11
24AA64
A0
A1
A2
Vss
Vcc
WP
SCL
SDA
VADJ
C64
100n
SCL
SDA
U5
AD5662
R35
240
C53
100n
C12
100n
U6
CFPV45
Vc
OE
GND
Vs
OUT
R20
100
CLK20M
FTMv3[4F]
C11
100n
DA6
REF192
REF
VIN
PWD
VOUT
GND
C60
10u
C61
100n
C62
10u
C63
100n
R41
100
DACVREF
FTMv3[3F], MCU[1A]
FTMv3[3F], MCU[1B]
OSC_EN
DIFF
CLK125MA
FTMv3[4E], FMC[6C]
DIFF
CLK125MB
FTMv3[4E], FMC[6C]
I2C
EEPROM_I2C
FTMv3[4F], FMC[6C]
Title
Size
A4
Number
Revision
Date:
10.23.2023
Sheet of