Status of the HGND FEE development and integration in the BM@N DAQ

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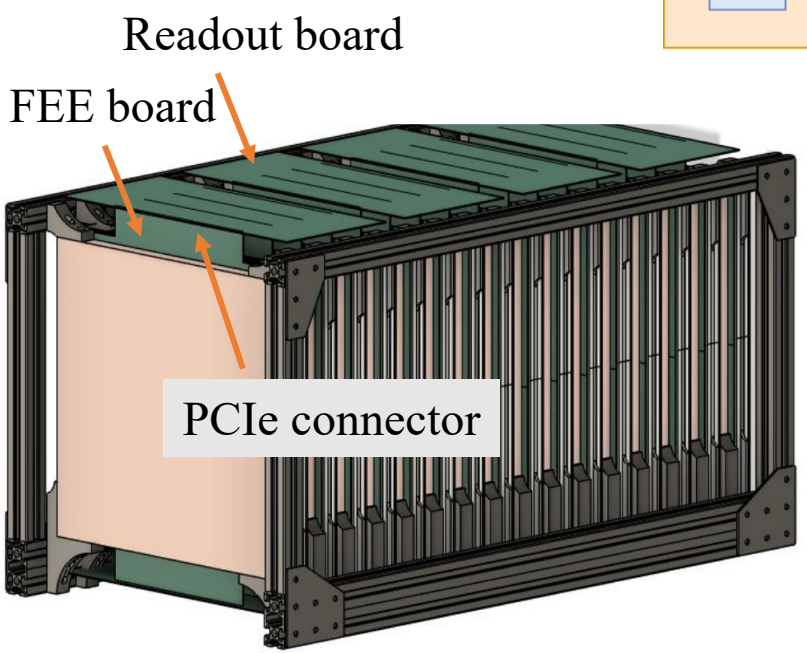
Outline

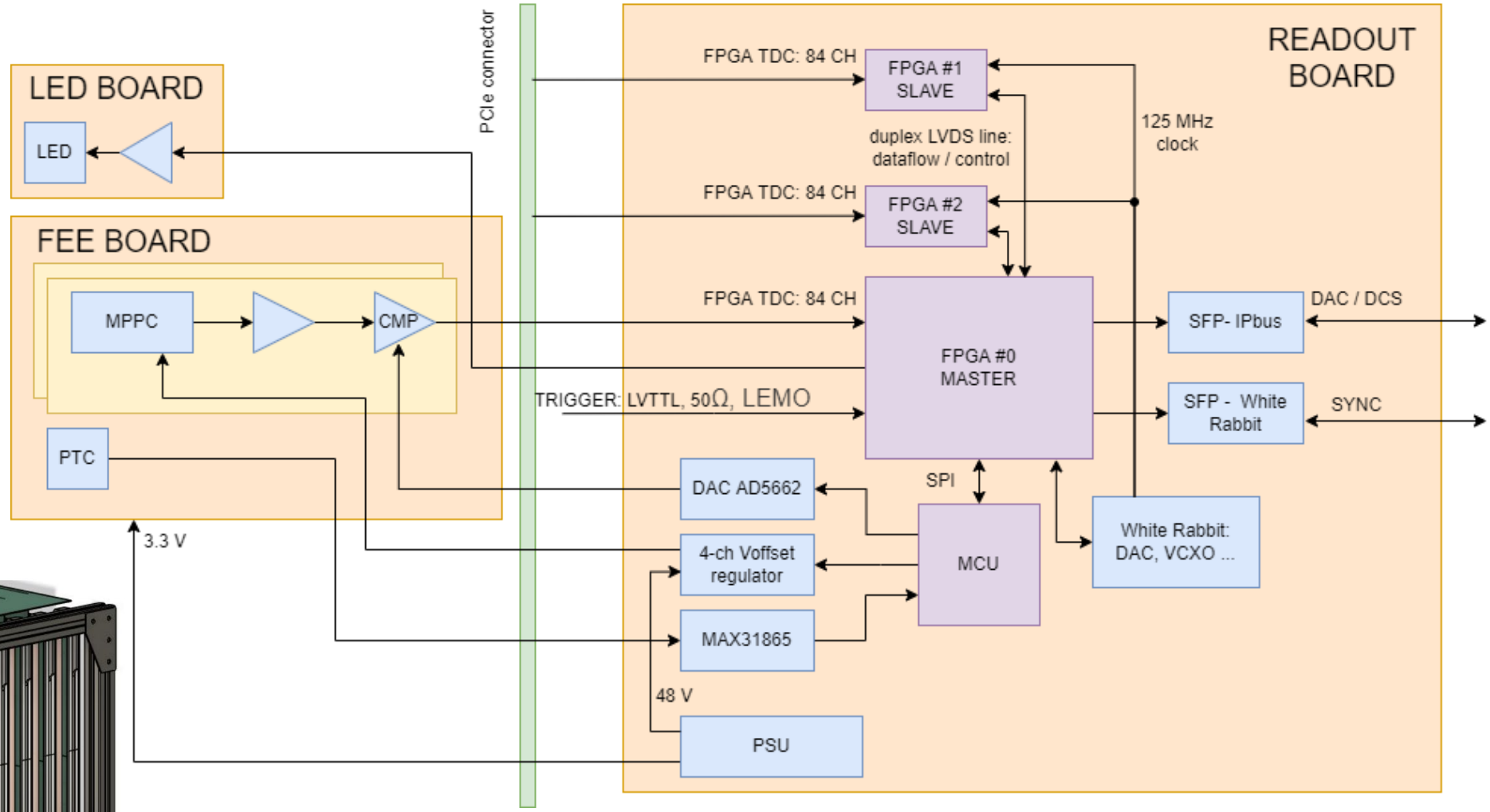
Architecture, prototyping, status and schedule:

- Front-End electronics
- Readout and control software

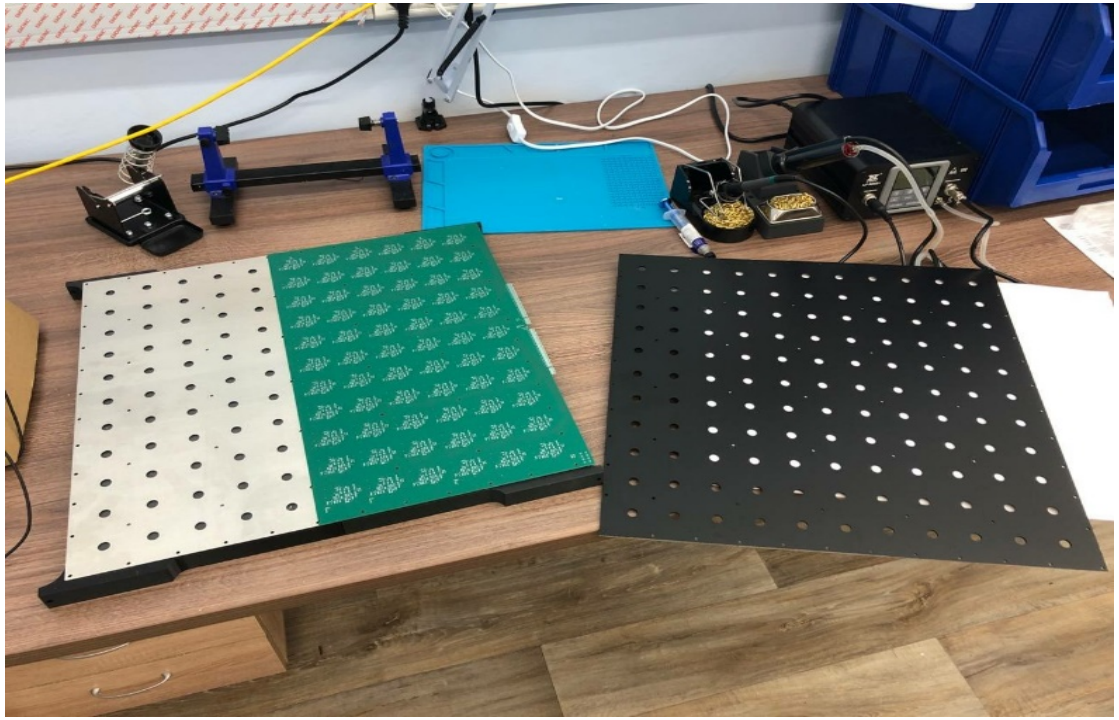
FEE & readout architecture

- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total





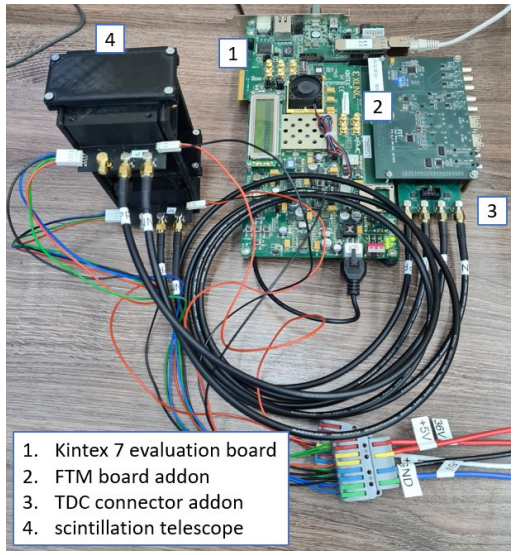
Status of the FEE board assembling



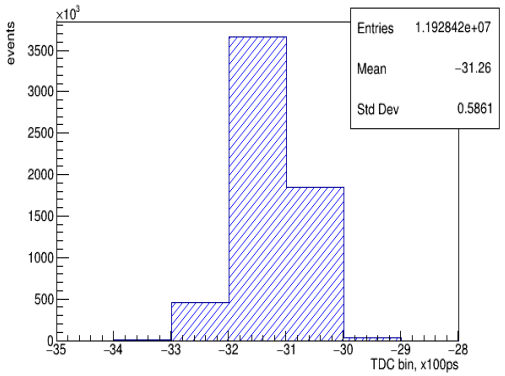
The FEE board assembled with scintillation matrix

The manufactured LED board

Status of the readout board assembling

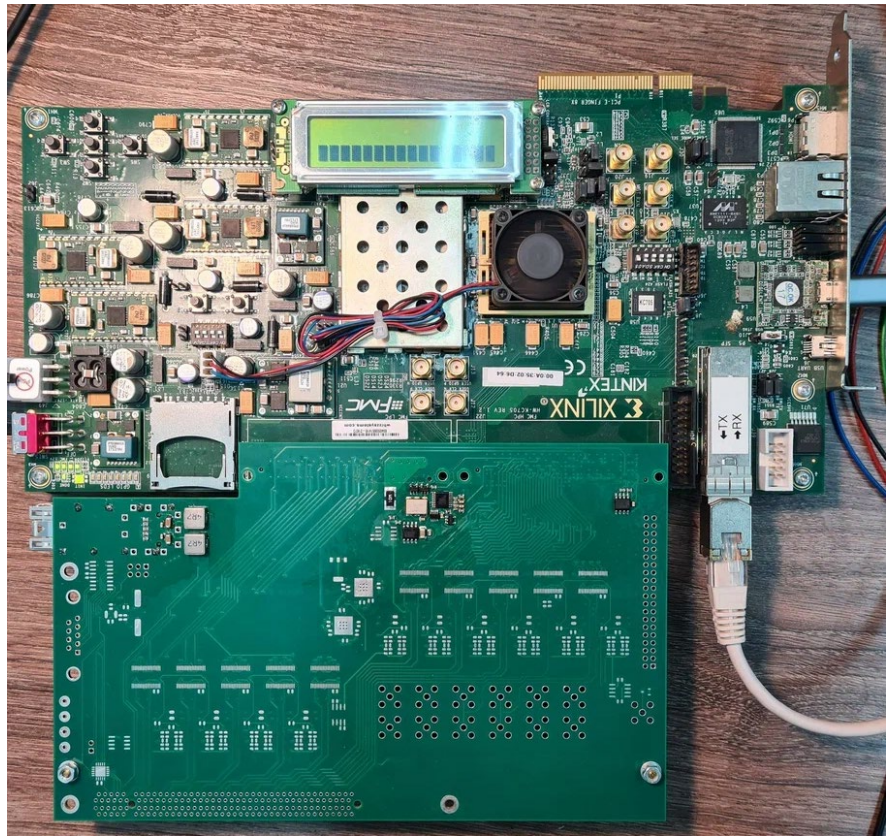


The 2-channels TDC prototype V1 connected to HGND scintillator cells telescope



The RMS of single TDC channel is 42ps. Measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).

- ✓ The 100 ps FPGA TDC is designed and tested with pulse generator, cosmic muons and e- test beam [2].
- ✓ The readout bord prototype V2 is designed and assembled (White Rabbit)
- ➢ Testing the White Rabbit firmware
- ➢ Developing the MCU firmware
- ➢ Working on the full scale readout board in parallel
- ❑ 33 channels readout test with coupled FEE board with PCIe (LED, cosmic, test beam)
- ❑ Integration to BM@N DAQ (time synchronization, DCS, data processing)
- ❑ Assembling the full scale readout board



The readout board prototype V2:

- 33 channels via PCIe + 6 channels via SMA (LEMO)
- 20 GPIO pins (debug + trigger)
- White Rabbit facility
- MCU functional: threshold comparator control, PTC sensor.

** The only setup currently soldered on the board is the White Rabbit configuration.*

Readout & trigger

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip
- ***White Rabbit*** (WR) is used for event's time synchronization (8 links total):
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events

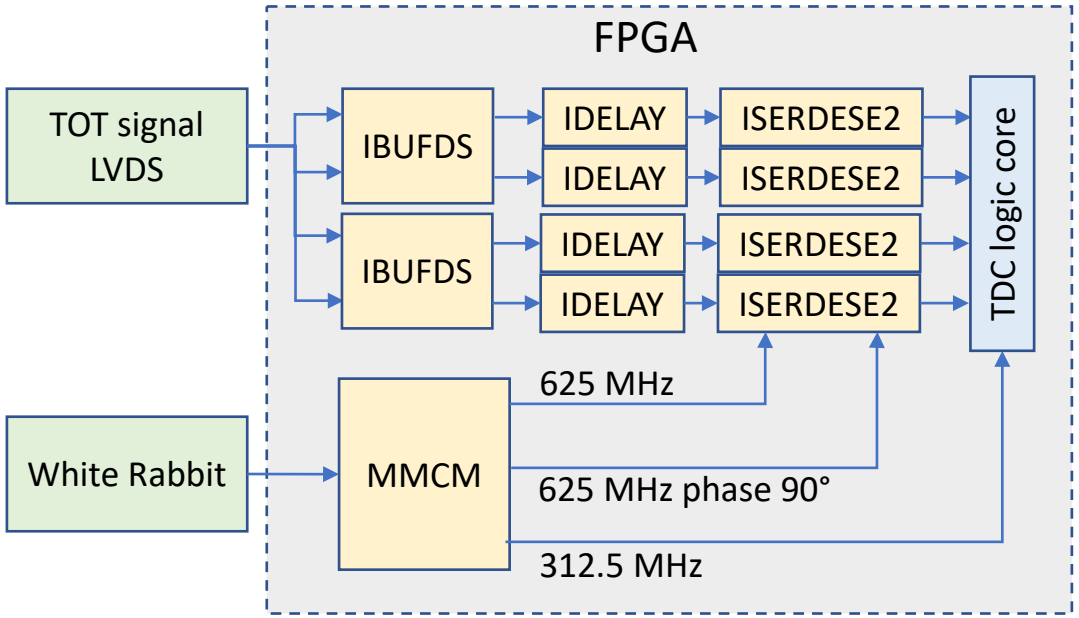
- Ethernet UDP protocol (***IPbus*** [1]) is used for data forwarding and board control
- Local network connect readout boards (8 ethernet links) with FLP

- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit per link is not exceed ***100 Mbit/s***. ***The continuous readout*** is implemented without busy signal.

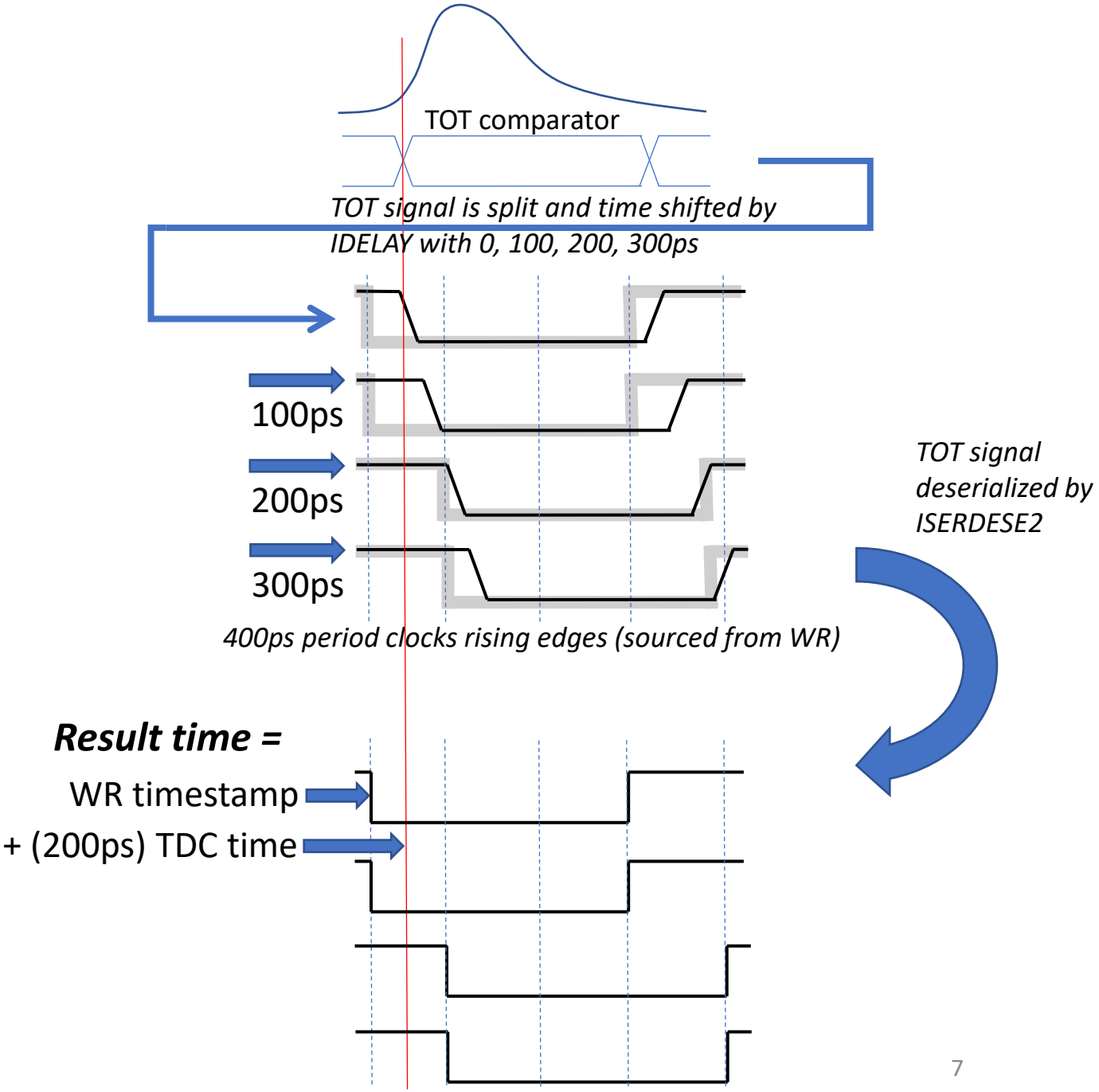
- The trigger is processed on FLP site:
  - Trigger signal is digitized with WR timestamp in FPGA
  - Message trigger accompanied by a timestamp is transmitted via IPbus for the ***trigger flags assignment to hits on the FLP site.***

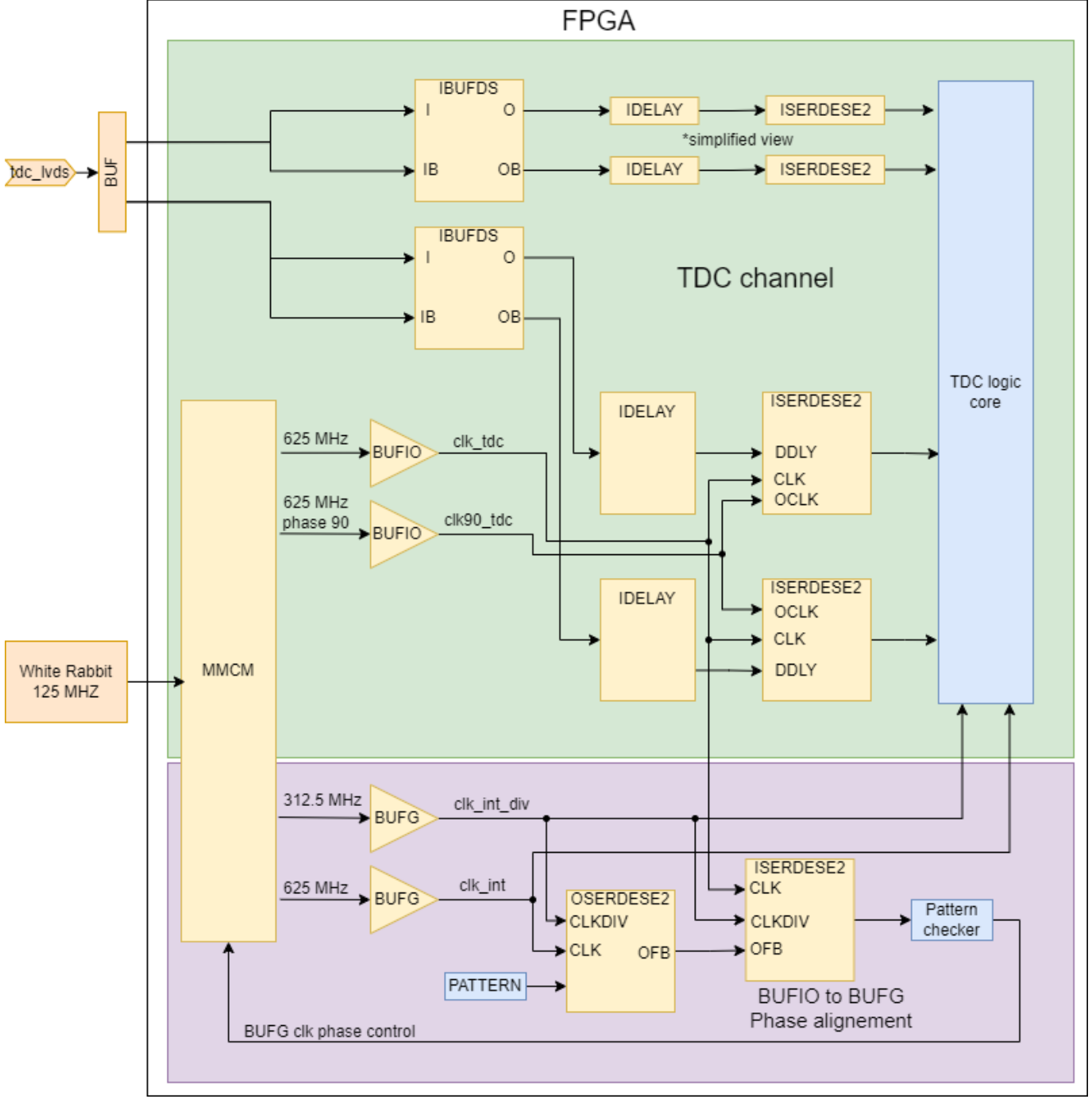
[1] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, ***IPbus: a flexible Ethernet-based control system for xTCA hardware****, JINST 10 (2015) no.02, C02019.*

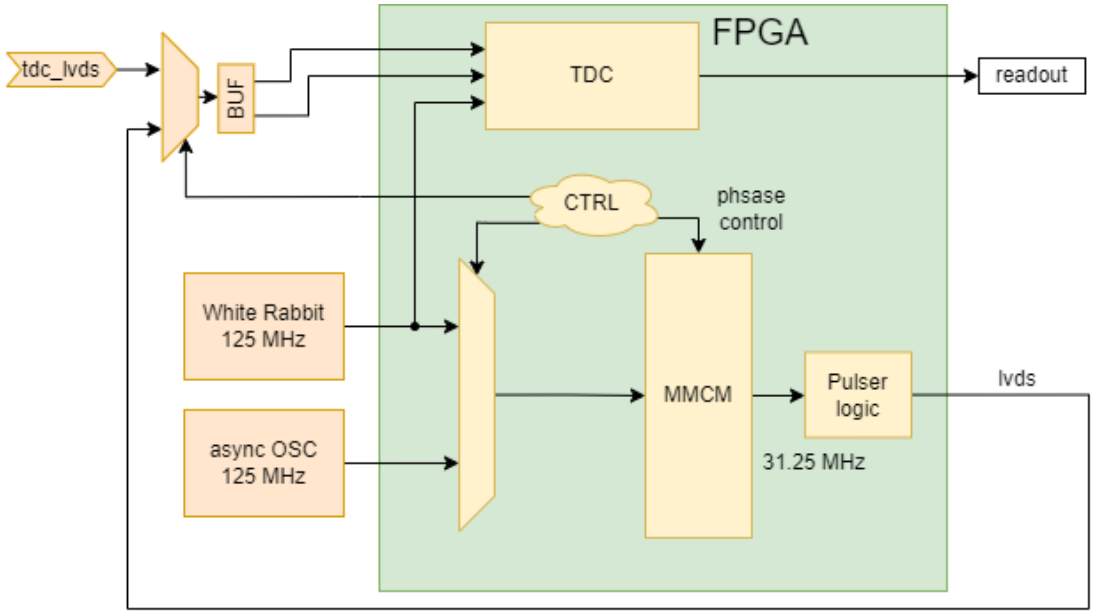
The 100ps FPGA TDC principle of operation



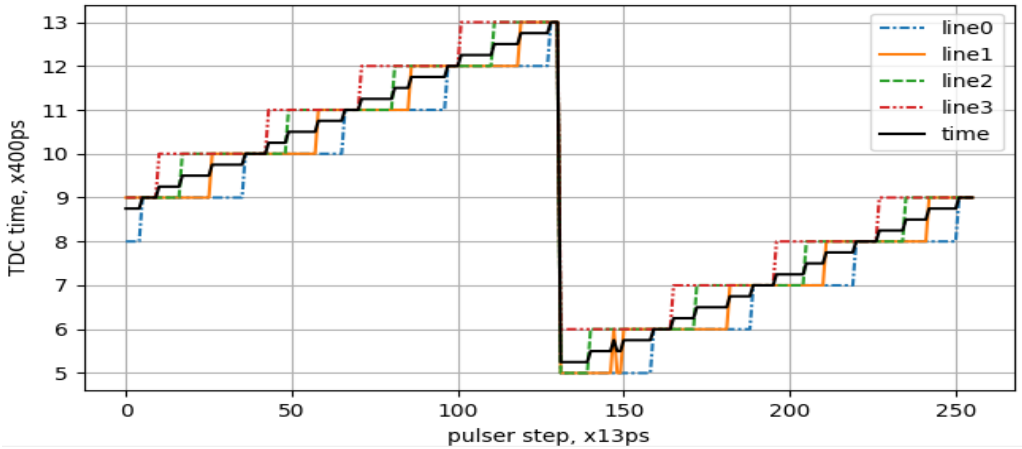
The TDC is based on the Kintex-7 input serial-to-parallel converter with oversampling capability and programmable delay. The design is based on Xilinx recommendations, and uses only documented features of the FPGA within its specifications.



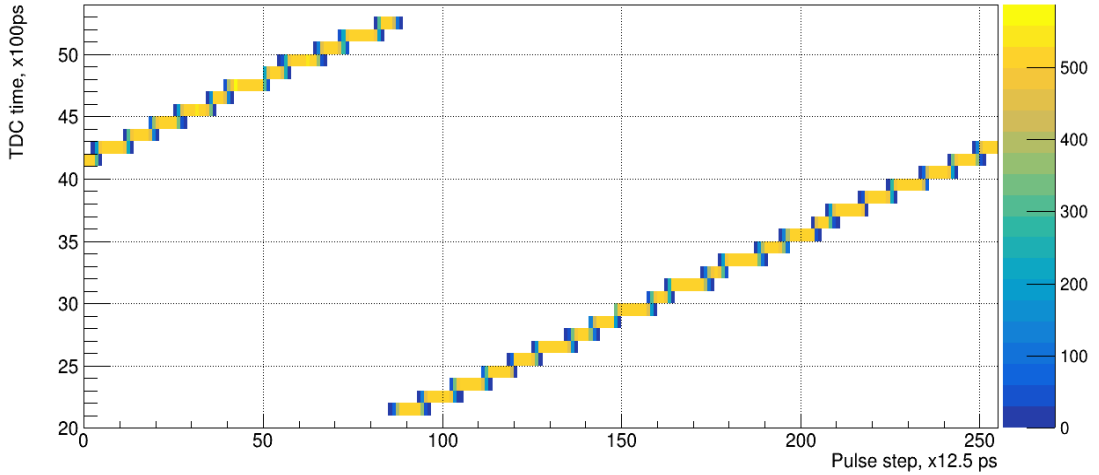

FPGA
tdc_lvds
BUF
IBUFDS
I
O
IB
OB
IDELAY
ISERDESE2
*simplified view
TDC channel
TDC logic core
625 MHz
BUFIO
clk_tdc
625 MHz
phase 90
clk90_tdc
DDLY
CLK
OCLK
White Rabbit
125 MHZ
MMCM
312.5 MHz
BUFG
clk_int_div
clk_int
OSERDESE2
CLKDIV
PATTERN
Pattern
checker
BUFIO to BUFG
Phase alignement
BUFG clk phase control


tdc_lvds
BUF
FPGA
TDC
readout
CTRL
phsase
control
White Rabbit
125 MHz
async OSC
125 MHz
MMCM
Pulser
logic
lvds
31.25 MHz

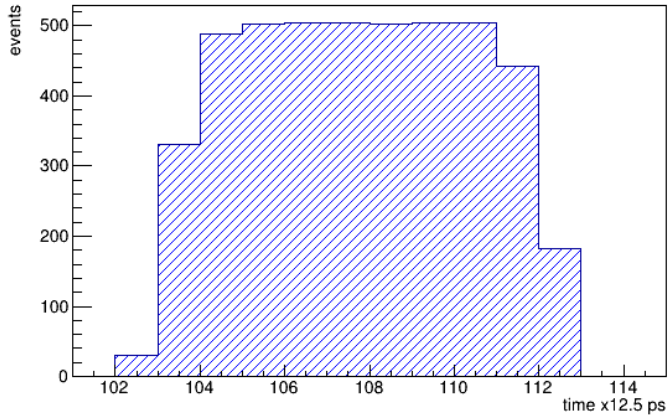
The FPGA TDC time scan results

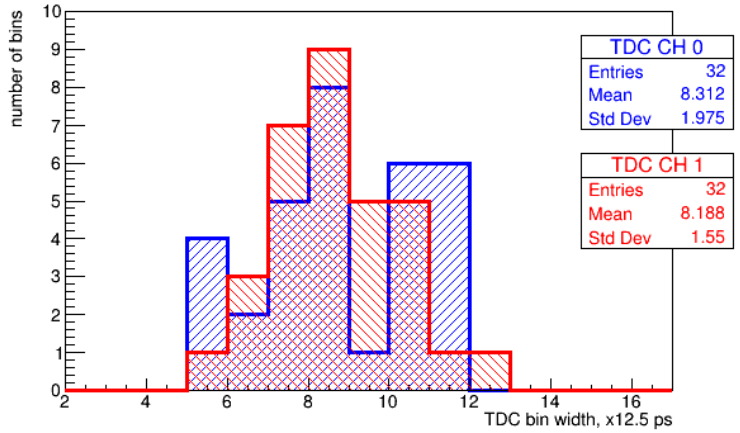


Four TDC lines and the resulting time dependence on the pulse time shift are shown. Pulses are generated by FPGA MMCM synchronously to the TDC clock with a phase step of 12.5ps. The single scan pass was taken with a digital FPGA logic analyzer.



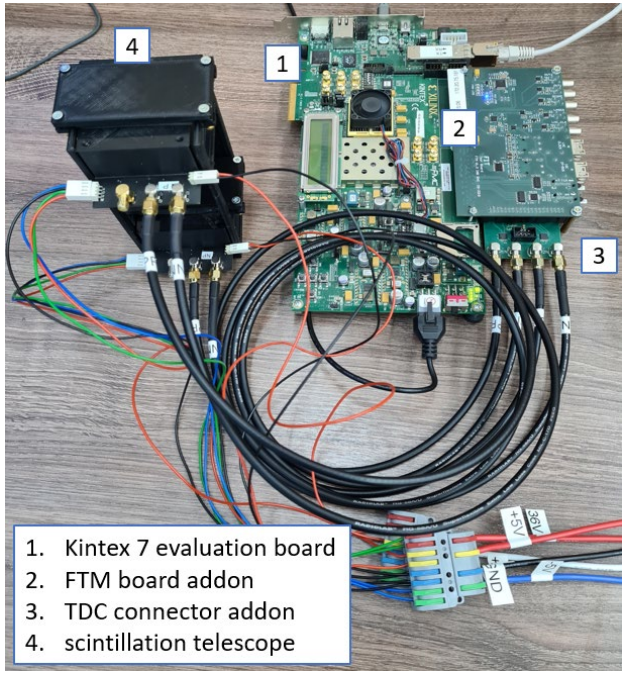
The TDC time dependence on pulse time shift. Pulses are generated by FPGA MMCM synchronous to TDC clock, and the time step is 12.5 ps. Data was taken with PC readout, 1000 events per single time shift step.





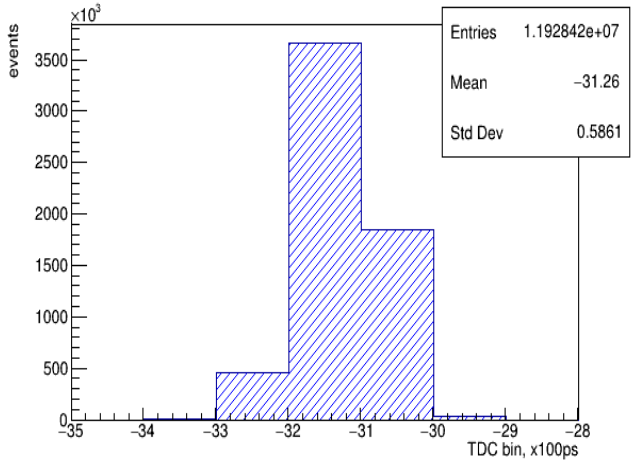
The TDC bin width measured with pulses synchronous to the TDC clock. Left: Typical TDC bin profile taken with a synchronous time scan. Right: The TDC bin width distribution for both TDC channels. The bin width value taken at the amplitude level is 30% in the bin profile. The TDC bin width distribution RMS is ***20 ps***. The main contribution to the TDC bin width distribution is the TDC line delay alignment step of 38.8 ps.

The FPGA TDC test results



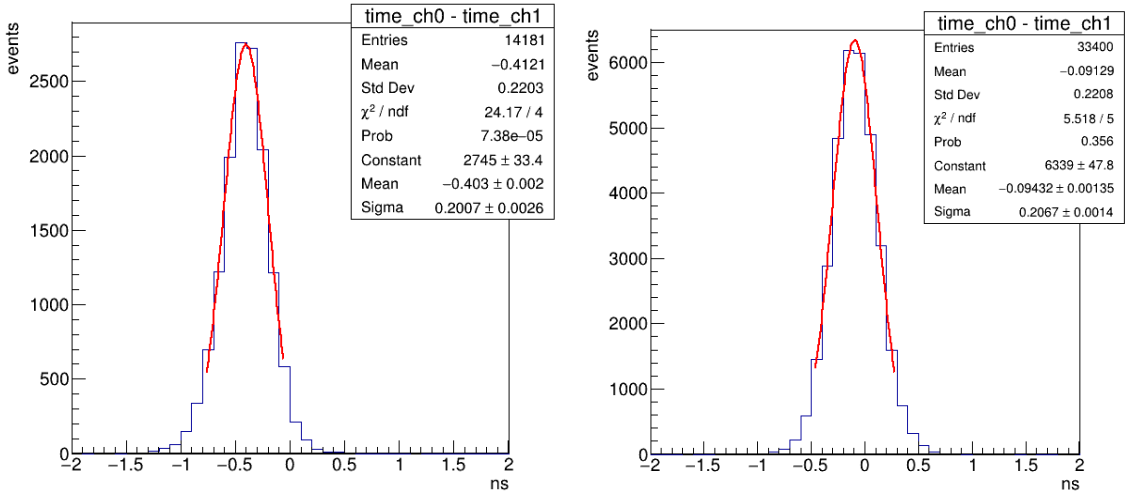
HGND scintillator cells telescope is connected to 2-channels TDC prototype based on KC705 evaluation board

The time difference distribution between two FPGA TDC channels measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).



The RMS of single TDC channel is 42ps.

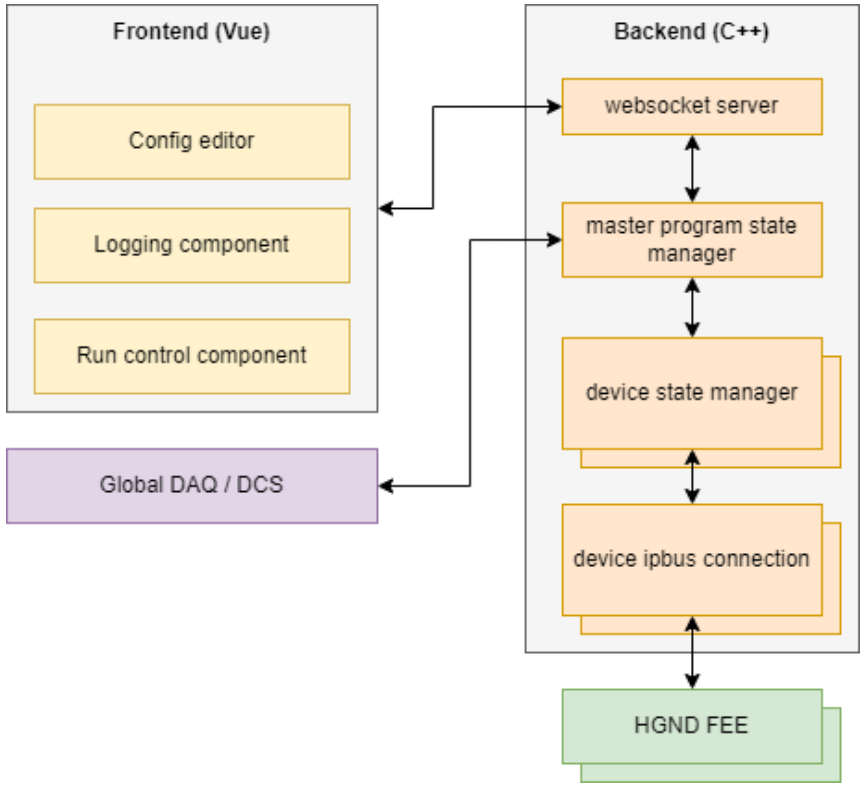
The time resolution measurements with the FPGA TDC prototype board were performed with the 280 MeV electron beam on the “Pakhra” synchrotron in LPI (Moscow, Russia).

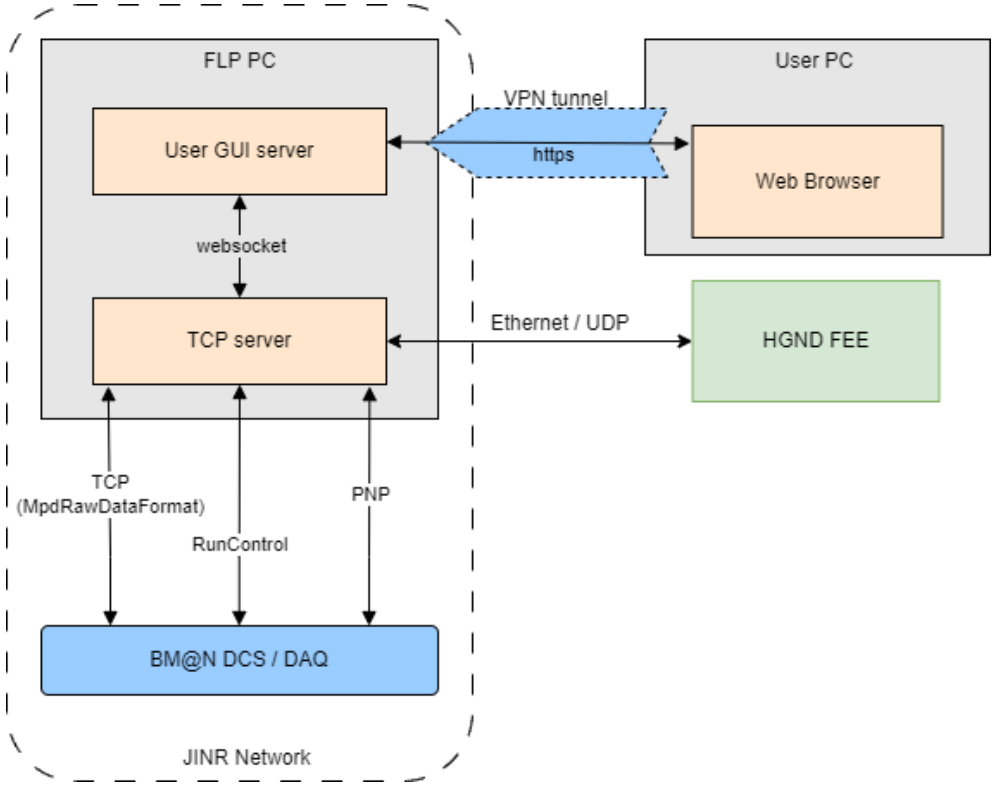


The time difference distributions of two cells of the telescope measured with the CAEN digitizer (left) and the FPGA TDC prototype board (right). Time resolution is ***146 ps*** per single HGND channel.

[2] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

The topology of the DCS & readout software

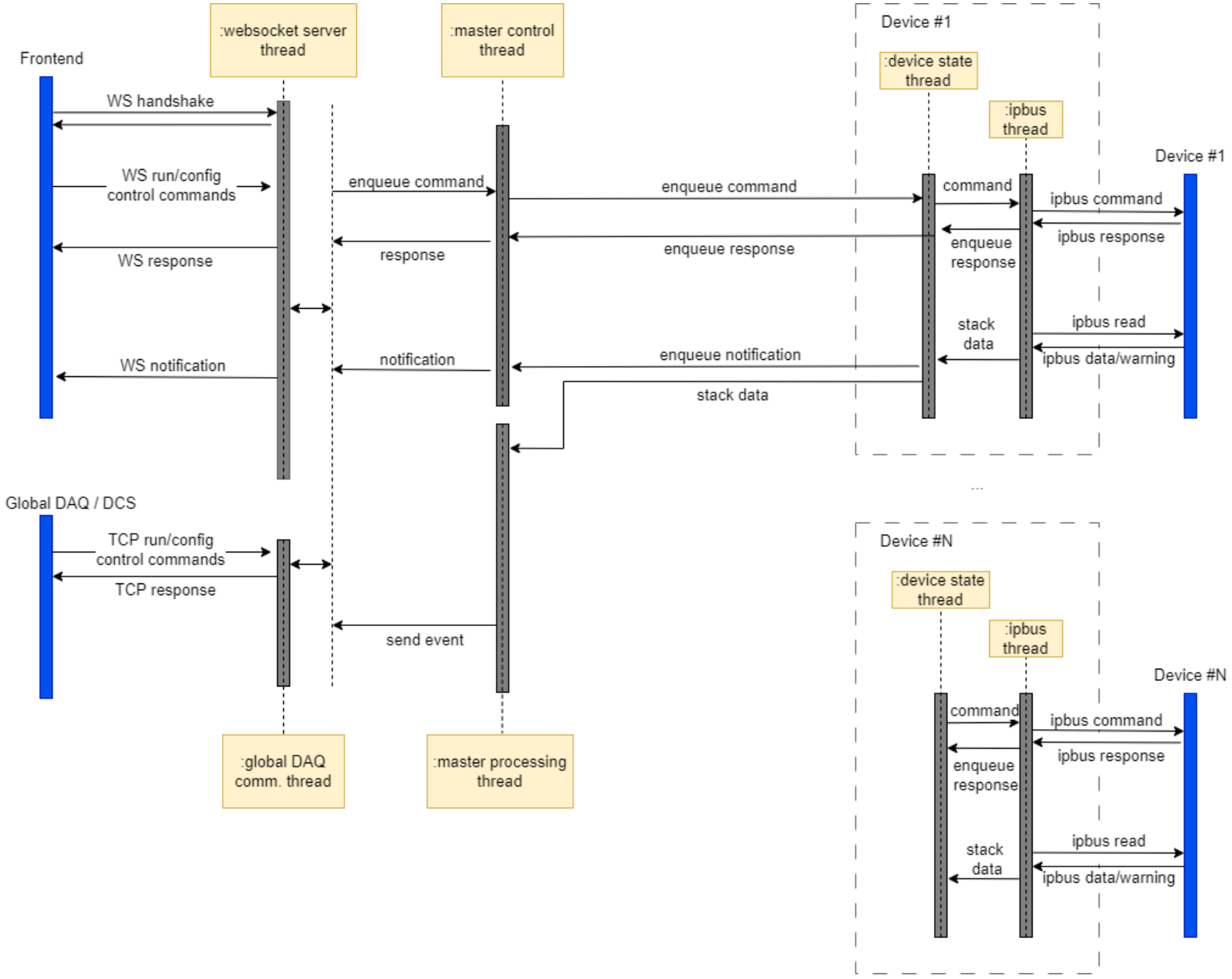




- The detector control system consists of 2 independent modules: frontend and backend
- The backend is a C++ server running on a DCS computer in the same network with detectors.
- The server part provides write/read operations to the detectors via an IPBus connection to the control and data acquisition board.

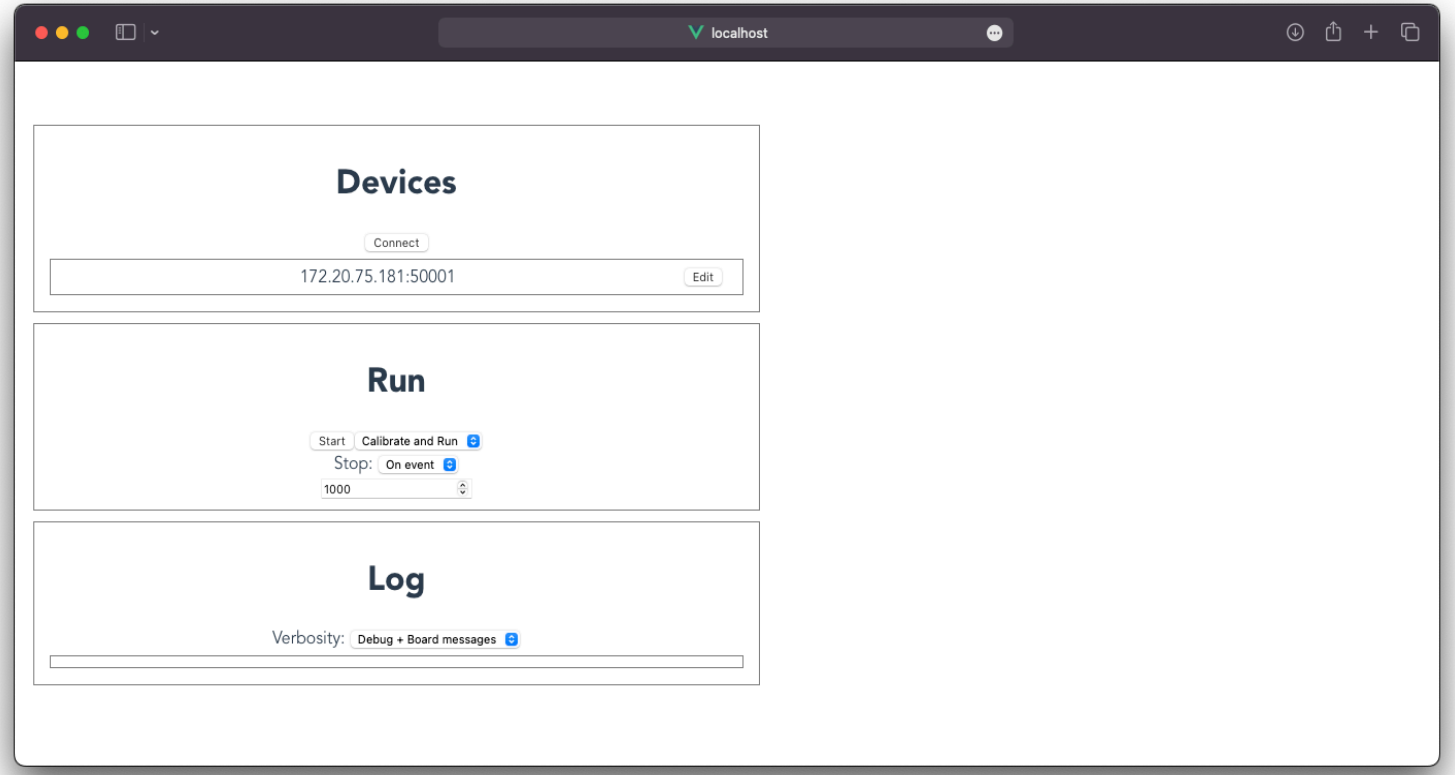
- Frontend is the user interface for this backend. It can be implemented in various ways; the key parameters are reactivity and an ability to establish a connection via websocket with the server part.
- The current version is the Vue web application (open-source JavaScript framework).
- The interface can be run either on the DCS computer or on the operator's computer, provided that the port is available.

The threading scheme of a C++ backend



Status of the software development

- ✓ The DCS server is implemented for local operation (data is collected and stored locally)
- ✓ Data can be transmitted over TCP in MpdRawDataFormat
- ✓ The interface allows one to perform the necessary operations for reading data and controlling detector parameters
- ➢ Implementation of additional functions in the GUI (including functions for quick viewing of calibration data; editing the configuration of detectors)
- ❑ March 2024: Local testing of management and data collection from multiple boards
- ❑ March – April 2024: Implementation of PNP and RunControl protocols for control from BM@N DCS



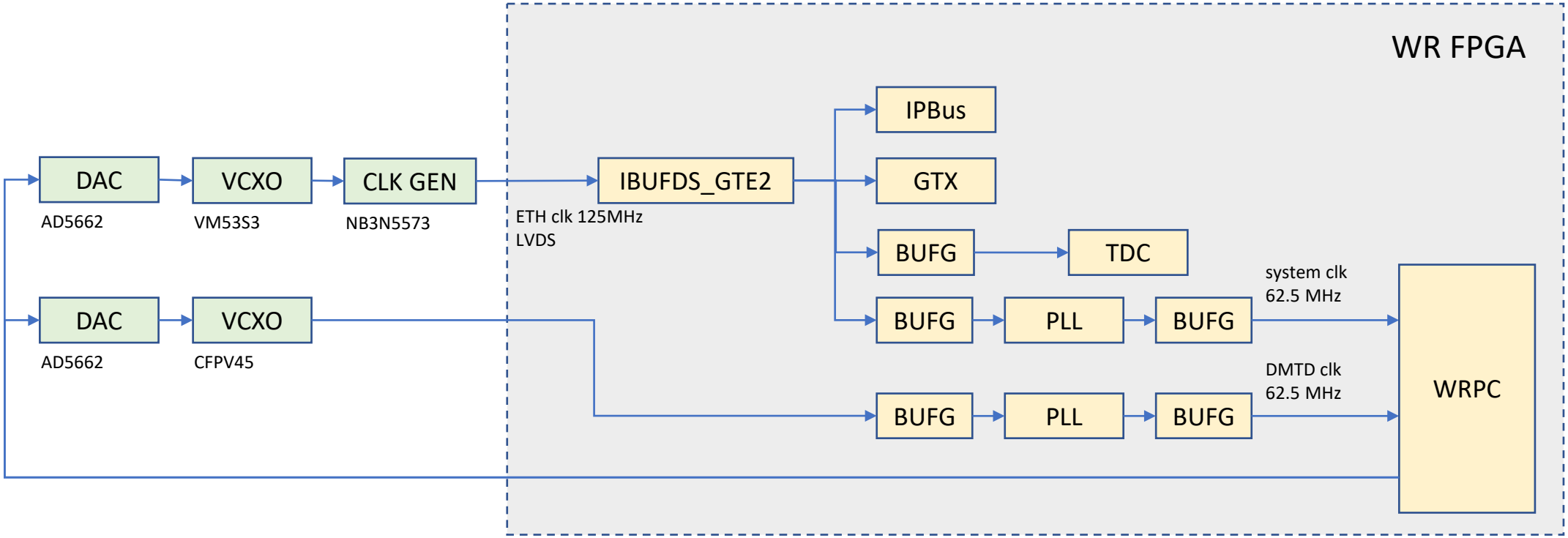
HGND DAQ & DCS GUI current view

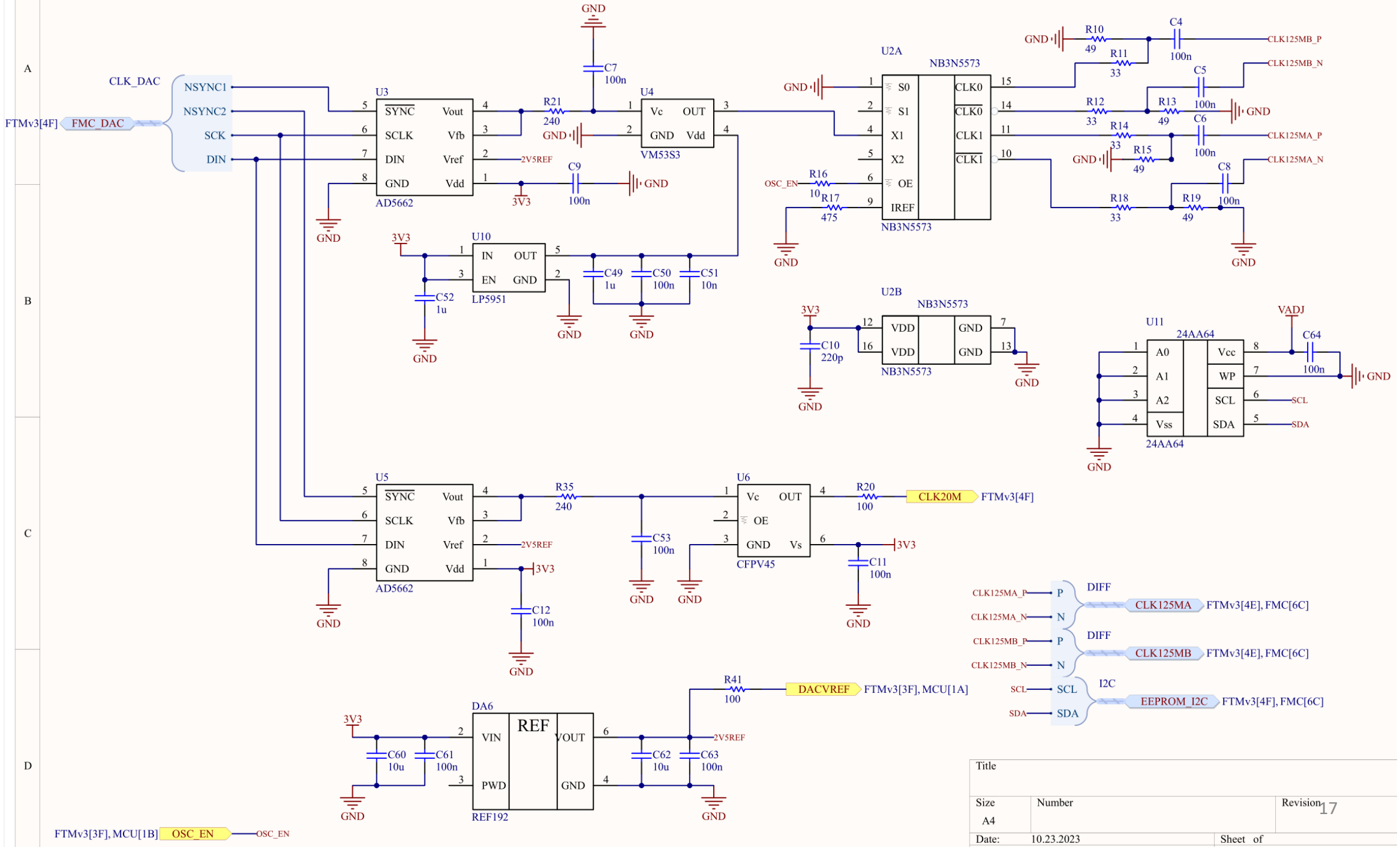
Conclusions

- The FEE board is assembled with scintillator board.
- The 100 ps TDC based on Kintex 7 FPGA was designed and tested
- The fully functional readout board prototype V2 was assembled (based on Kintex Evaluation board, single FPGA, 39 channels)
- Testing the White Rabbit setup
- The DCS & readout software: the backend server is implemented; next: tests with HW, integration tests
- Working on the design of the full scale readout board

BACKUP

The White Rabbit implementation




CLK_DAC
NSYNC1
NSYNC2
SCK
DIN
FTMv3[4F]
FMC_DAC
U3
SYNC
SCLK
DIN
GND
Vout
Vfb
Vref
Vdd
AD5662
R21
240
2V5REF
3V3
C7
100n
C9
100n
U4
Vc
GND
OUT
Vdd
VM53S3
U10
IN
EN
OUT
GND
LP5951
C52
1u
C49
1u
C50
100n
C51
10n
U2A
NB3N5573
S0
S1
X1
X2
OE
IREF
CLK0
CLK0
CLK1
CLK1
OSC_EN
R16
10
R17
475
R10
49
R11
33
R12
33
R13
49
R14
33
R15
49
R18
33
R19
49
C4
100n
C5
100n
C6
100n
C8
100n
CLK125MB_P
CLK125MB_N
CLK125MA_P
CLK125MA_N
U2B
NB3N5573
VDD
VDD
GND
GND
C10
220p
U11
24AA64
A0
A1
A2
Vss
Vcc
WP
SCL
SDA
C64
100n
VADJ
SCL
SDA
U5
AD5662
R35
240
U6
CFPV45
Vc
OE
GND
OUT
Vs
R20
100
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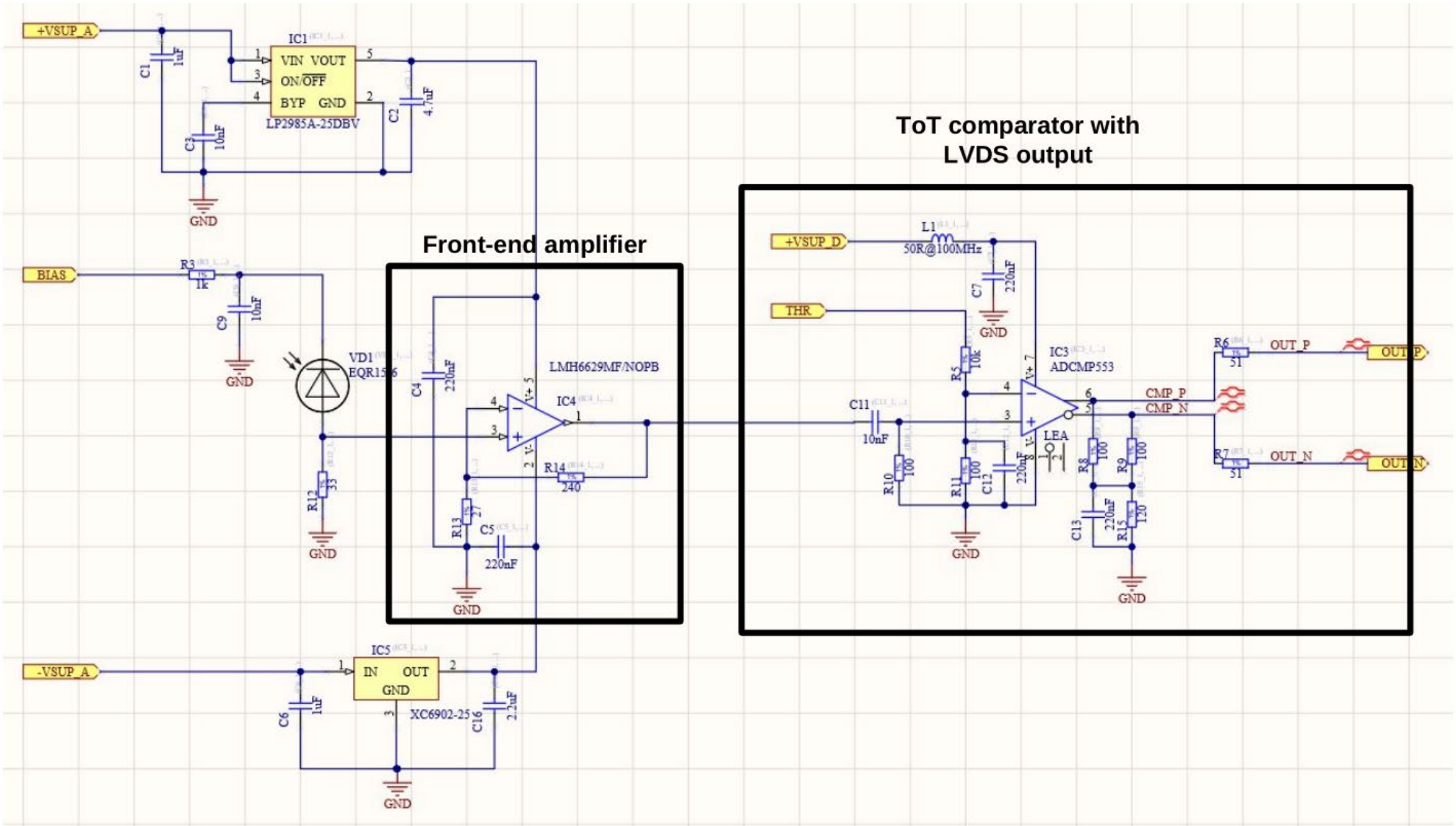
100n
C11
100n
C12
100n
DA6
REF192
VIN
PWD
VOUT
GND
REF
C60
10u
C61
100n
C62
10u
C63
100n
R41
100
DACVREF
FTMv3[3F], MCU[1A]
CLK125MA_P
CLK125MA_N
CLK125MB_P
CLK125MB_N
SCL
SDA
P
N
DIFF
I2C
CLK125MA
CLK125MB
EEPROM_I2C
FTMv3[4E], FMC[6C]
FTMv3[4F], FMC[6C]
FTMv3[3F], MCU[1B]
OSC_EN
Title
Size
A4
Number
Revision
Date:
10.23.2023
Sheet of



- 20dB amplification
- 2.2 nV/$\sqrt{Hz}$ noise level
- Per-channel supplies
- Variable threshold (common for the half-layer)
- LVDS output