Design and test results for the first prototype version of ASIC for the tracking system

on behalf of NRNU MEPhI ASIC Lab

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Plan

Introduction

Modern (quite complex) application specific integrated circuits (ASICs) for experiments such as BM@N require at least 3-4 prototyping stages, each including the CAD chip design, manufacturing of few tens chips and their lab tests

Here presented are the results on the 1st prototype of an ASIC to be developed to read out signals of STS microstrip sensors

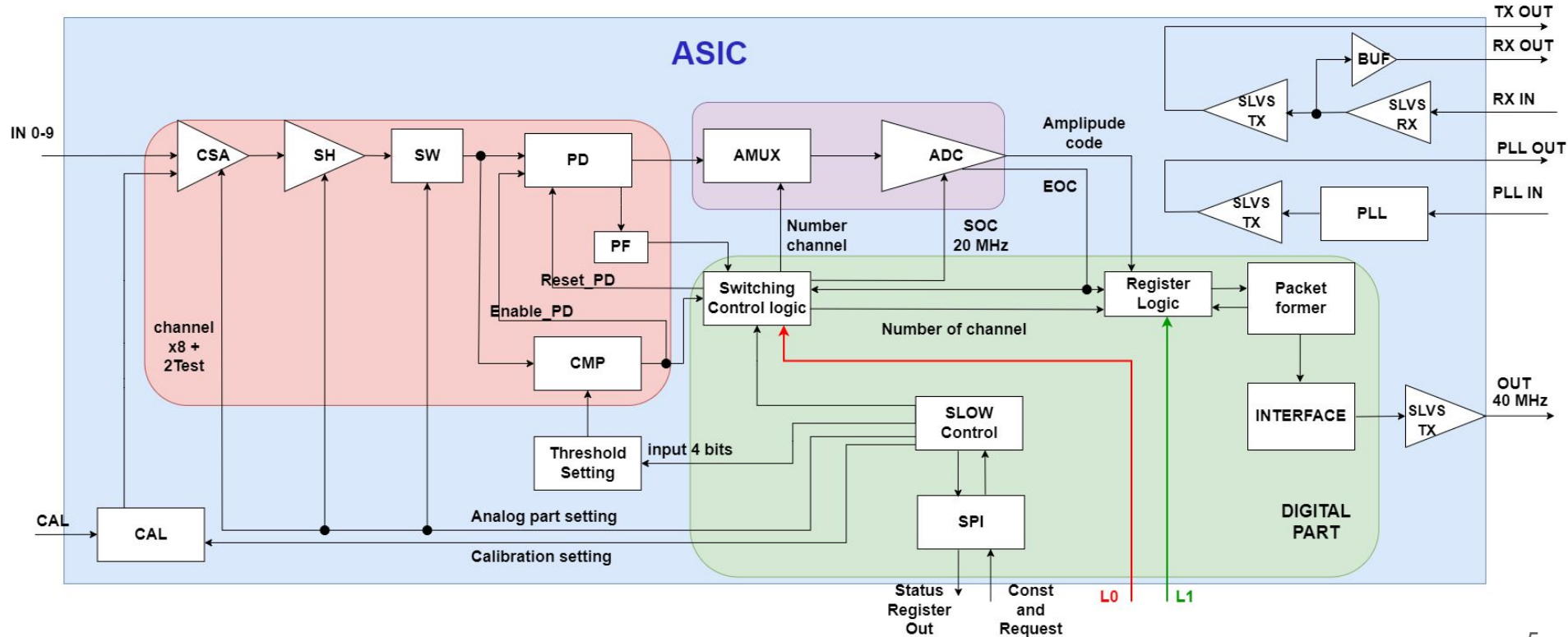The 1st version has aimed to the following goals:

– choose a structural diagram;

– design all the basic building analog blocks, being connected in the channel;

– design digital and interface blocks;

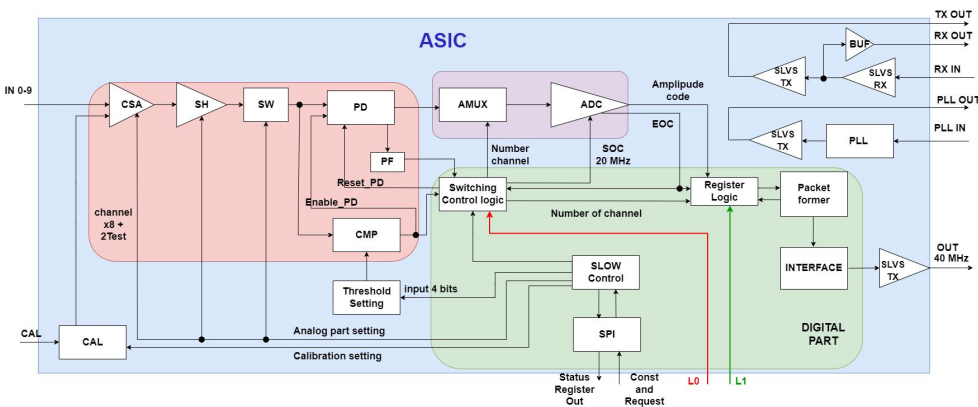– develop small-scaled version of final ASIC to test block connectivity

Key specifications of the 1ˢᵗ prototype

Parameter	Value
Number of analog channels	8 + 2 (outermost test channels)
Input signal range	3.6 fC (1 mip – the most typical signal) to 108 fC (30 mips)
Polarity	selectable (positive or negative)
ENC	< 1500 el at C_{det} up to 30 pF
Shaper peaking time	programmable: 200, 300 or 500 ns
Channel signal rate	< 1 khz
ADC	10 bit at 40 ns conversion time
Power consumption	100 mW (in total) = 70 mW (10x analog chains + ADC) + 20 mW (digital part) + 10 mW (test blocks)
Control interface	SPI
Additional test blocks	SLVS TX + RX, PLL, ADC

Block diagram (simplified)

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Structure and design team

Part	Designers
Analog: set of 10 analog chains type of ESD+CSA+SH+pol_SW+PD	E. Atkin, S. Yamaliev, Yu. Bocharov, V. Butuzov
Mixed signal: AMUX (incl. ADC driver), ADC	Yu. Bocharov, V. Butuzov
Digital and Digital on Top assembly of whole chip	D. Normanov, P. Ivanov, V. Yurovsky
Auxiliary (analog calibration system, emulator for digital part) and test blocks (SLVS TX+RX, PLL, stand alone ADC)	E. Atkin, S. Yamaliev, V. Yurovsky, D. Normanov, Yu. Bocharov, V. Butuzov

A design route was chosen as Digital On Top: the top level of the project was presented as predominantly digital due to the complexity of digital part and need to have a specialized interface in the future full-scaled version
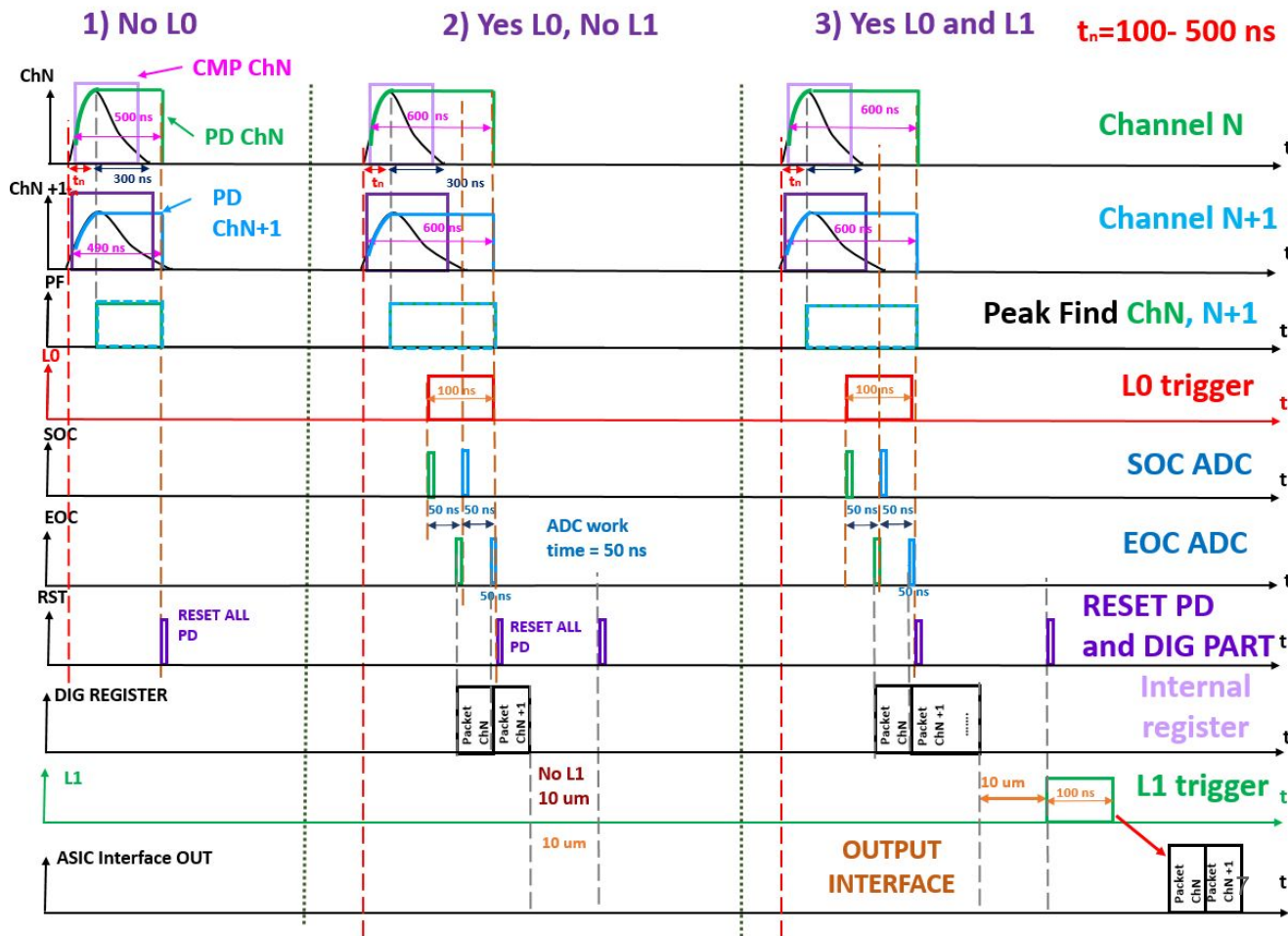
Typical chronograms versus L0 & L1 triggers

The synchronization of the BM@N setup is provided so that the chips process input signals with a maximum frequency of 100 kHz by 2 triggers:

L0 with a frequency of 10 kHz and a delay of up to 500 ns
and
L1 with a frequency of 50 kHz and a delay of up to 10 µs
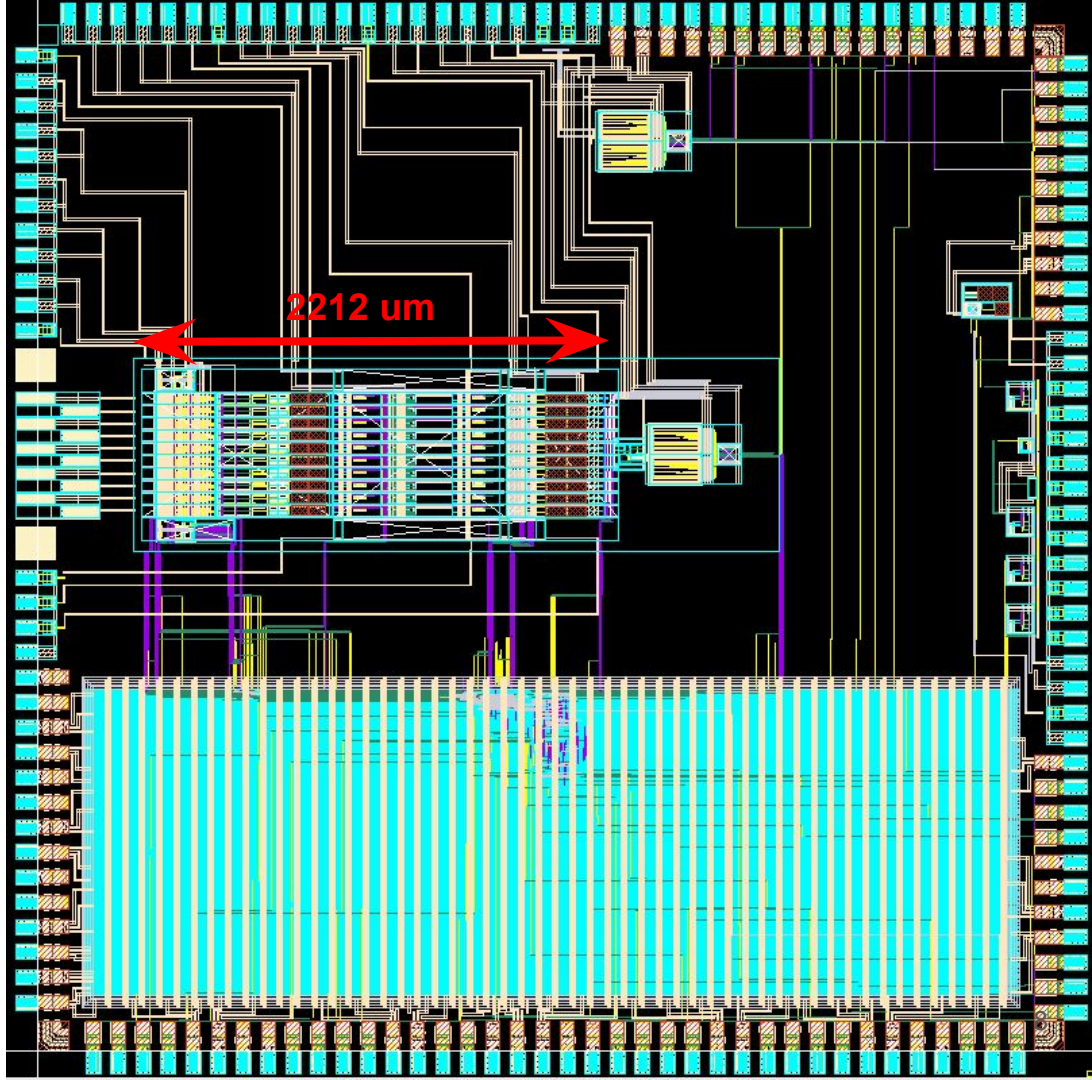
Layout

Process – 180 nm CMOS

Die size – 5000 x 5000 um

Nb. of analog channels – 8 + 2 (test)

Channel size – 2212 x 57 um

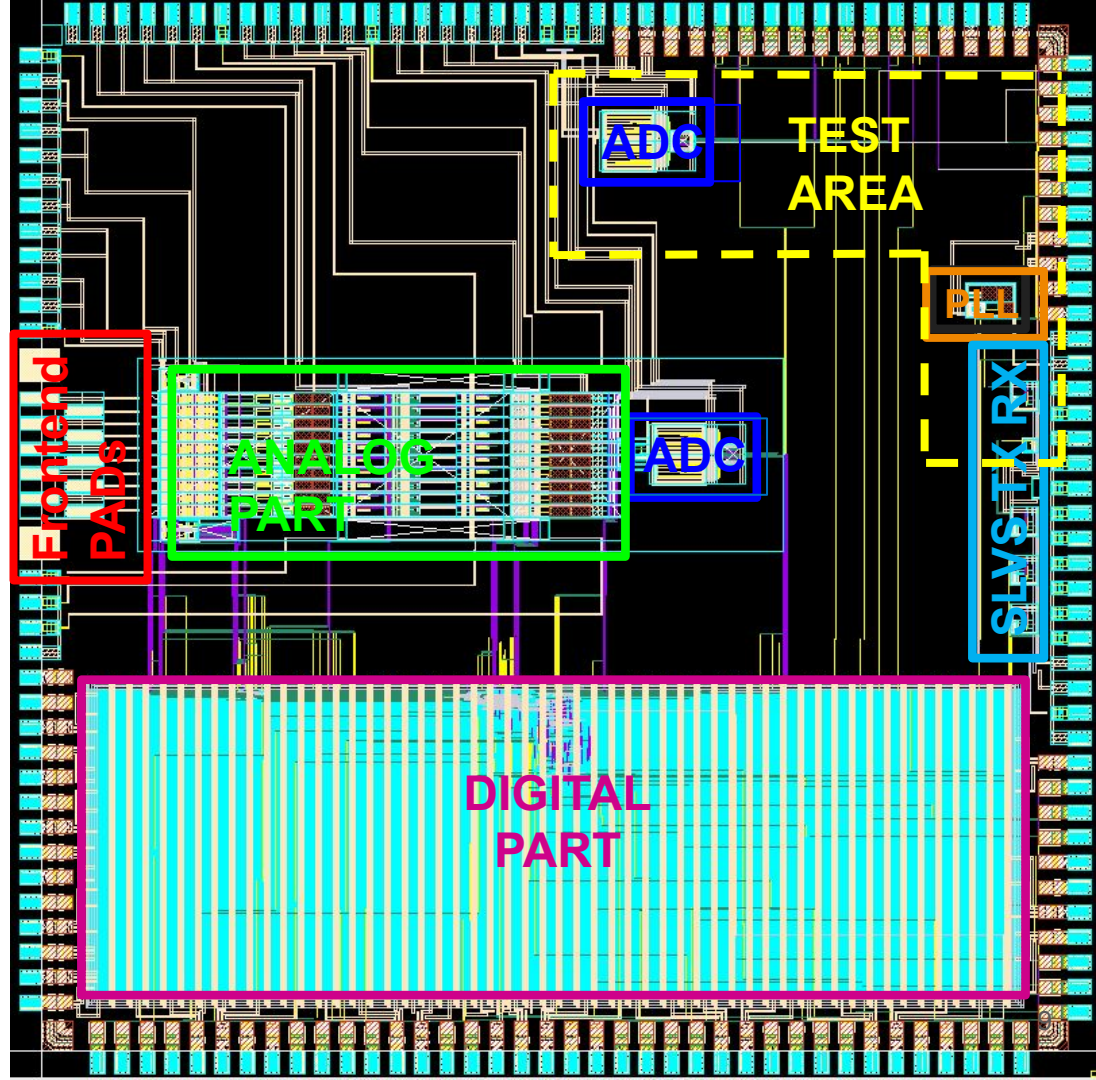Vertical size estimation for full-scaled ASIC (130 chs):

57*(128+2) = 7410 um

Total nb. of pads (IO cells) – 158, incl. 1) 10 frontend pads, sized by 180 um x 60 um; 2) 16 analog VSS pads, 16 analog VDD pads, 24 digital VSS pads, 24 digital VDD pads

Main building parts

- Mostly differential Analog front-end part, including 10 channels of the chain: ESD+CSA+SH+PD and MUX

- 10-bit ADC – one per whole set of analog channels

- Digital part, processing packet exchange under SPI control, and followed by SLVS TX

- Test block area, including stand-alone ADC, PLL, SLVS TX & RX

The design of both the analog and digital parts as well as operating protocols were carried out in such a way that they could be used in the subsequent upscaling to the full-scale version for 128 (+ 2 test) channels to be placed within area of **10 mm * 7 mm**

Lab test bench

UART over USB

Xilinx KC705

SPI

GPIOs

Serial 8b10b

USB LAN

USB LAN

Test Pulses

Testbench PCB

CSA

Shaper

Comparator

Programmable pulse/pattern generators

Digital oscilloscope

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Test results

- ADC works
- PLL works
- SLVS transmitter and SLVS receiver work
- SPI interface works
- Output interface works in static mode
- Switching control logic captures signal, but not captures L0 trigger, thus we can't test register logic and packet former
- CSA works
- Shaper works, but some instability is observed
- No way to test CMP & PD block (due to SH instability)

Further plans

1) Second prototype specs (32 + 2 chs., block optimization, add. I2C slow control interface, full version of output interface, extended design for test methodology) are to be defined in March 2024

2) CAD design stage for the 2nd prototype (up to GDSII-file) – 6 months

3) Submission for tape out – deadline in early October 2024

4) Chip batch (50+ pcs.) arrival in March-April 2025

5) Lab tests – June 2025

Month	Shuttle code	Fab	Reserved Deadline (TWN Time)	Window data Deadline (TWN Time)	GDS-In Deadline (TWN Time)	Shipping Date (TWN Time)
Year 2024						
Jul	M182407	8C	2024/6/17	2024/7/17	2024/7/22	By process option, Please contact your account manager for the
Oct	M182410	8S	2024/9/9	2024/10/9	2024/10/14	By process option,

Notes:

Ex.M182401 = M+18+24+01 = Mixed Mode process + 0.18um + 2024 + January

Summary

1) The prototype ASIC for STS has been designed (the first half 2023)

2) Submission for tape out was done late July 2023

3) Chips were arrived to JINR in December 2023

4) Test of chips were done in January and February 2024. Most of blocks works. Some problems exist in control digital part.

5) There were defined the list of reusable (IP) blocks as well as corrected plans and specs for the 2nd ASIC version

6) On behalf of the design team we gratitude to the staff of JINR and SINP MSU, who participated in the elaboration of the chip specifications and ASIC block diagram, as well as in a chip bonding and tests

Backup slides

Digital part