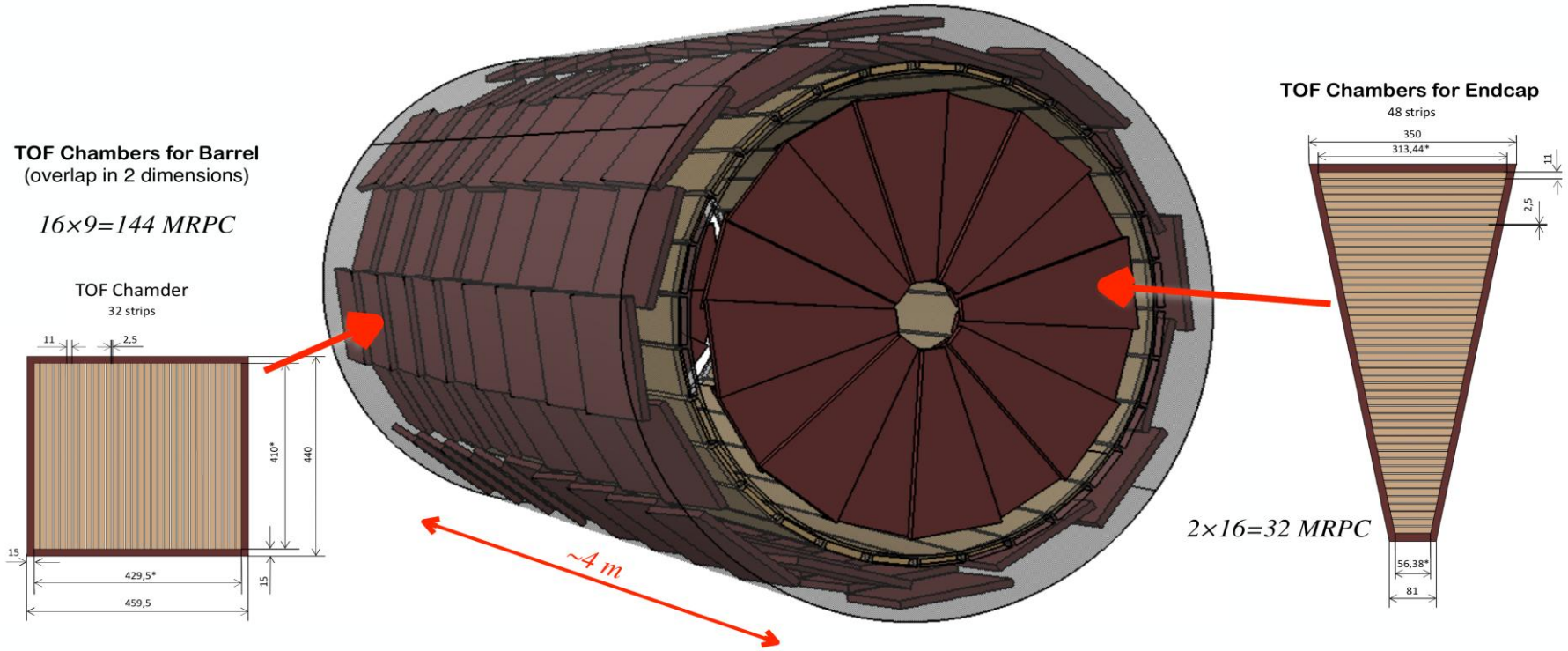
Time of Flight Detector
Status Report

Valery Chmill

Time of Flight (TOF) detector proposal

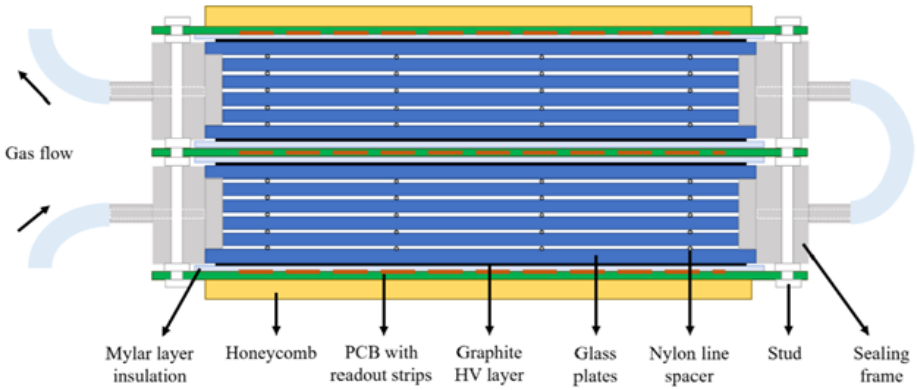


- π/K/p discrimination for momenta ≲2 GeV
- Determination of t0
- Time resolution requirement <60 ps.
- Sealed (MRPC) are the base option. B.Wang et al, JINST 15 (2020) 08, C08022

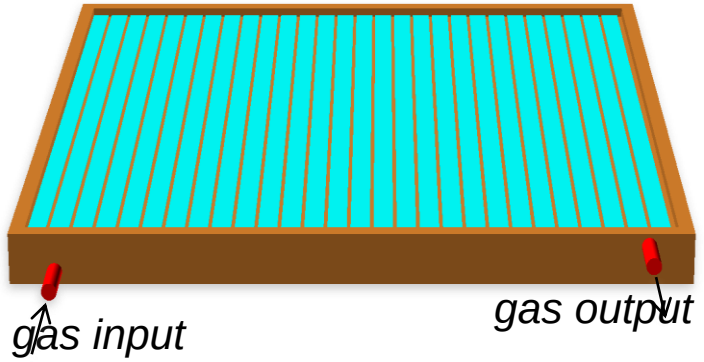
- Number of readout for Barrel is 144x2x32=9216 channels.
- Number of readout for Endcap is 32x2x48=3072 channels.
- Total amount is 12288 channels

Sealed MRPC for SPD TOF

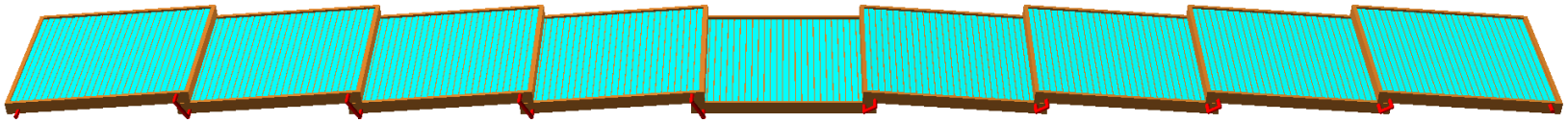
(B.Wang et al, JINST 15 (2020) 08, C08022)



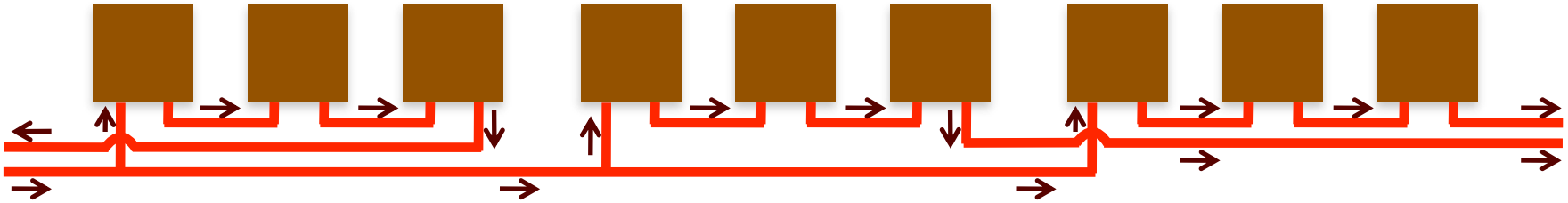
Sealed MRPC proposed for CBM-TOF



Sealed MRPC proposed for SPD-TOF

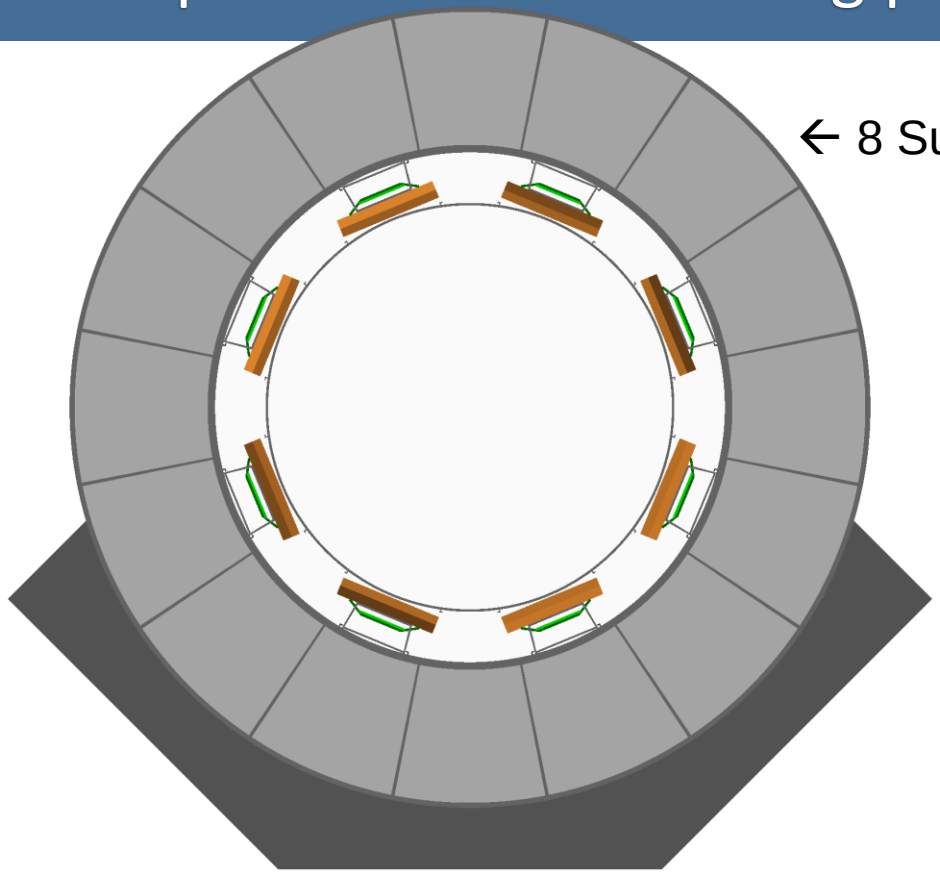


Serial gas connection of MRPCs in a single super module

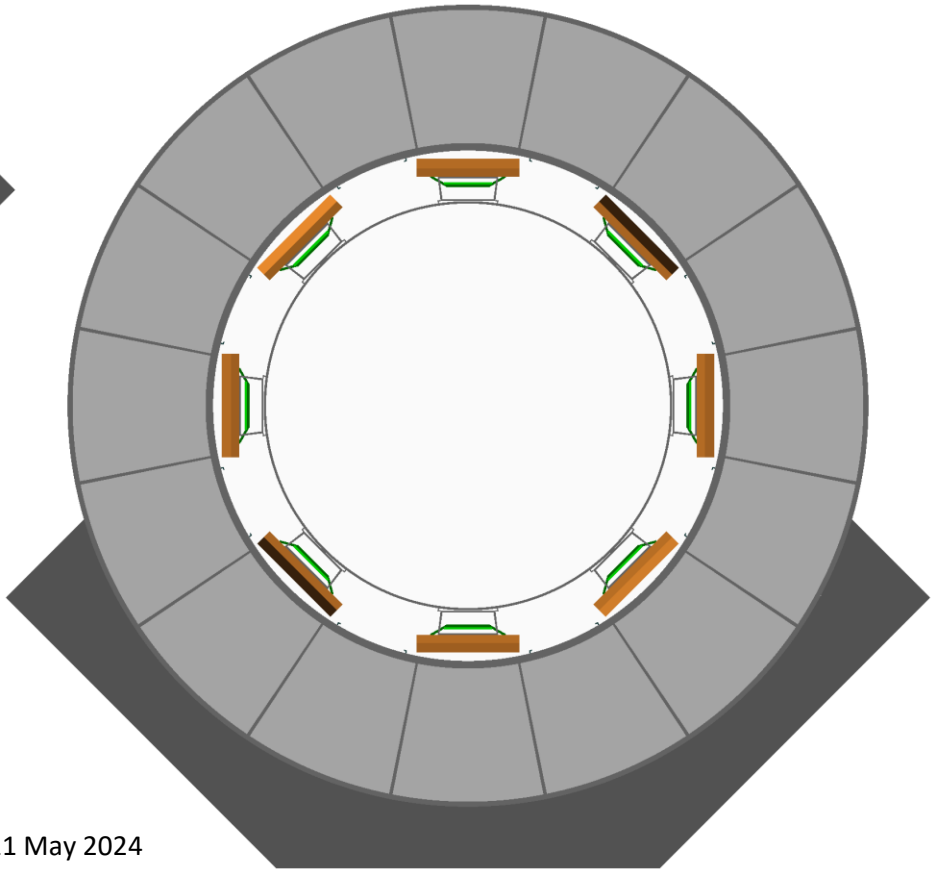


Super modules mounting proposal

← 8 Super modules mounting on e-Calorimeter

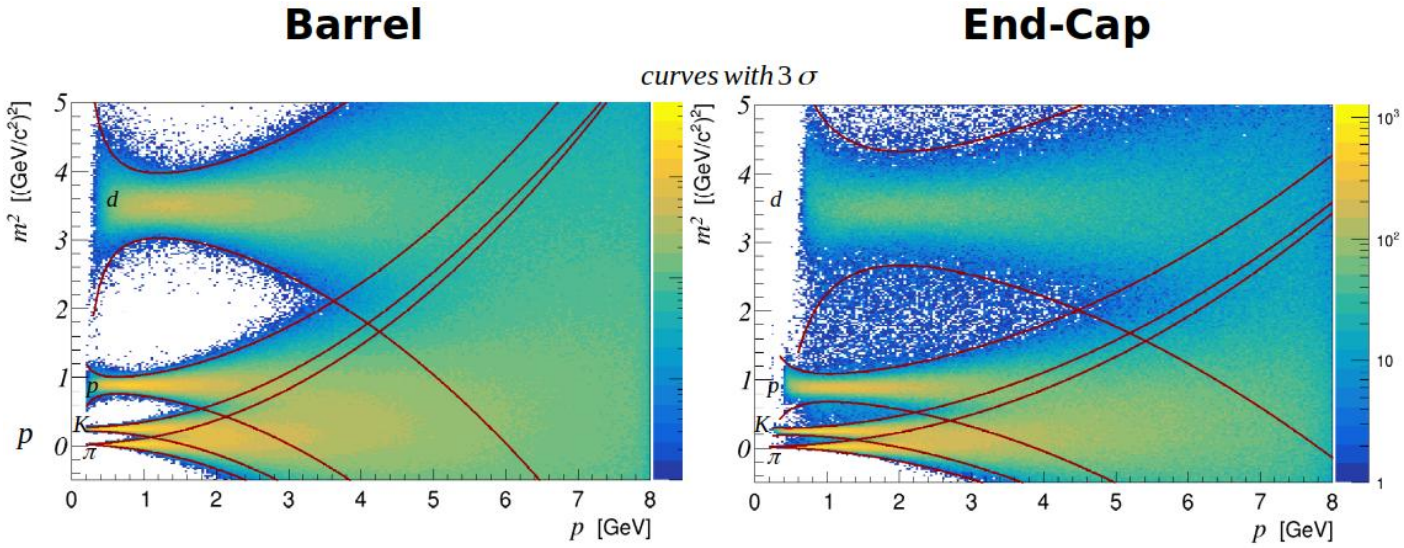


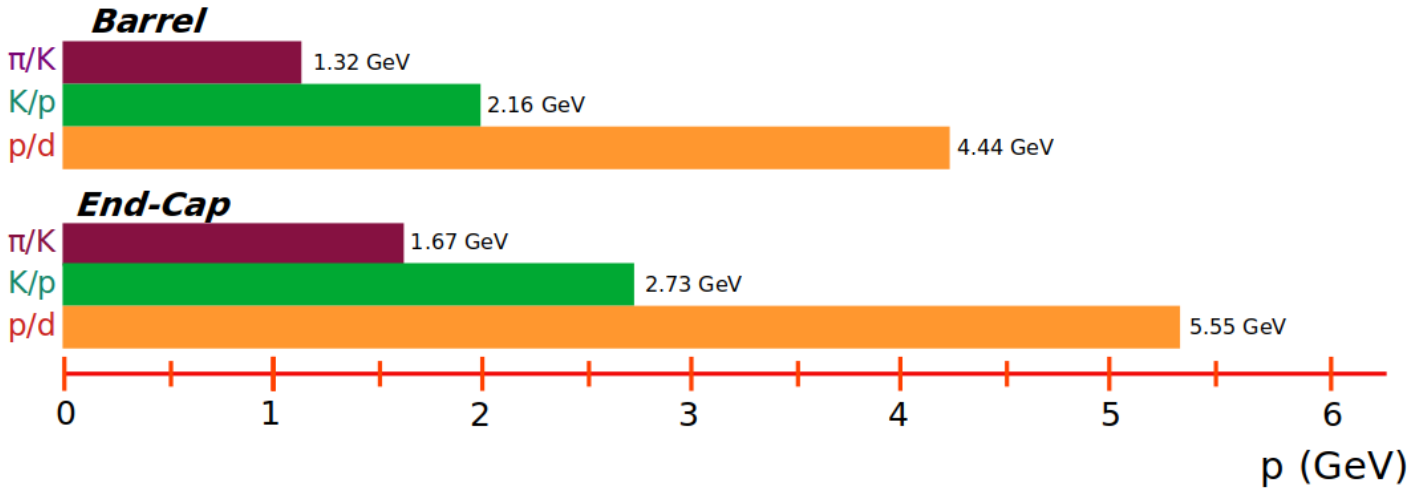
8 Super modules mounting on Straw crate →



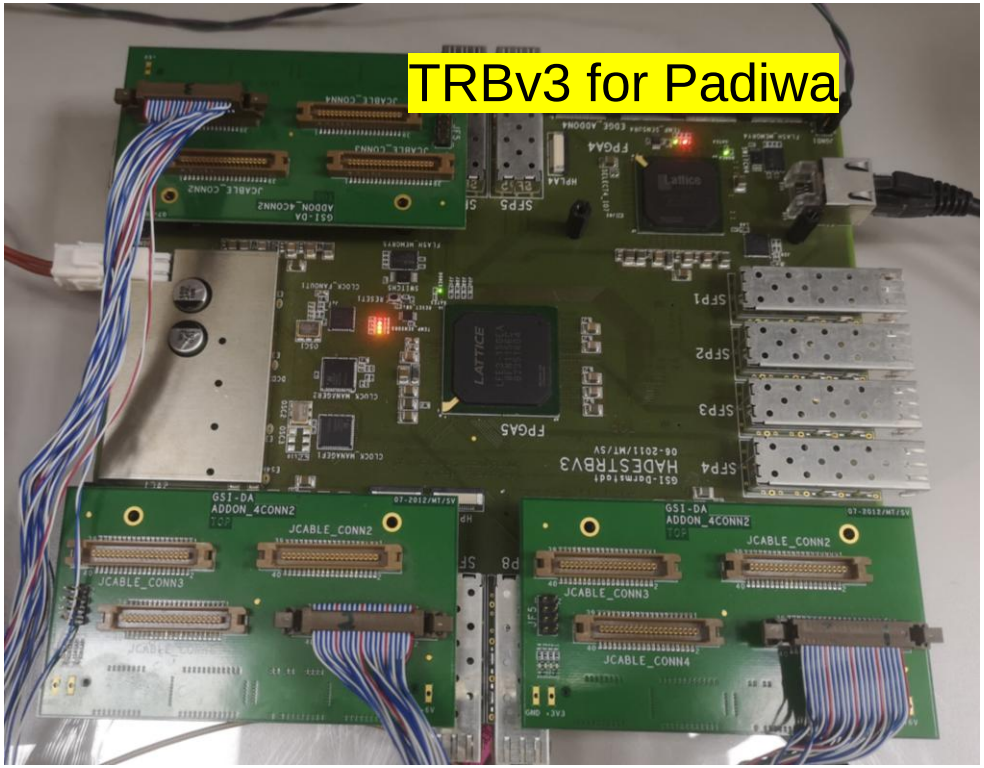
Particles ID for m^2 vs. p

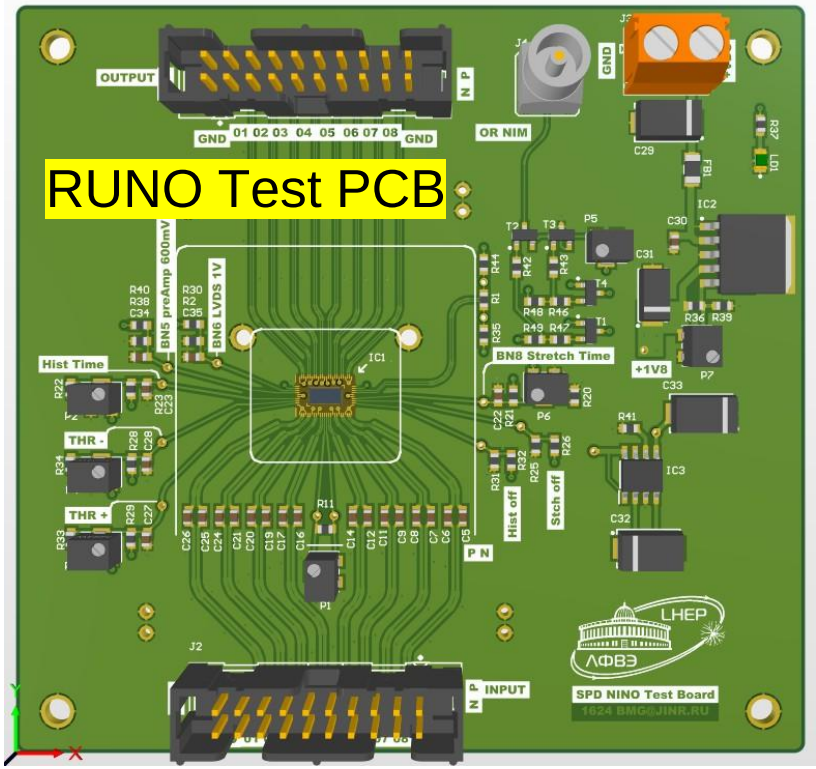
- π/K/p/d discrimination for momenta <2 GeV
- Determination of t0
- Time resolution requirement <60 ps.

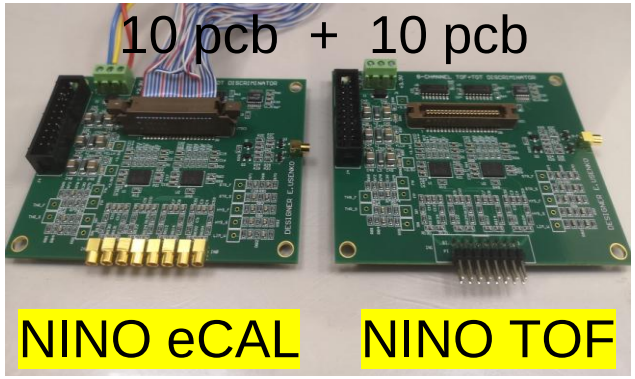




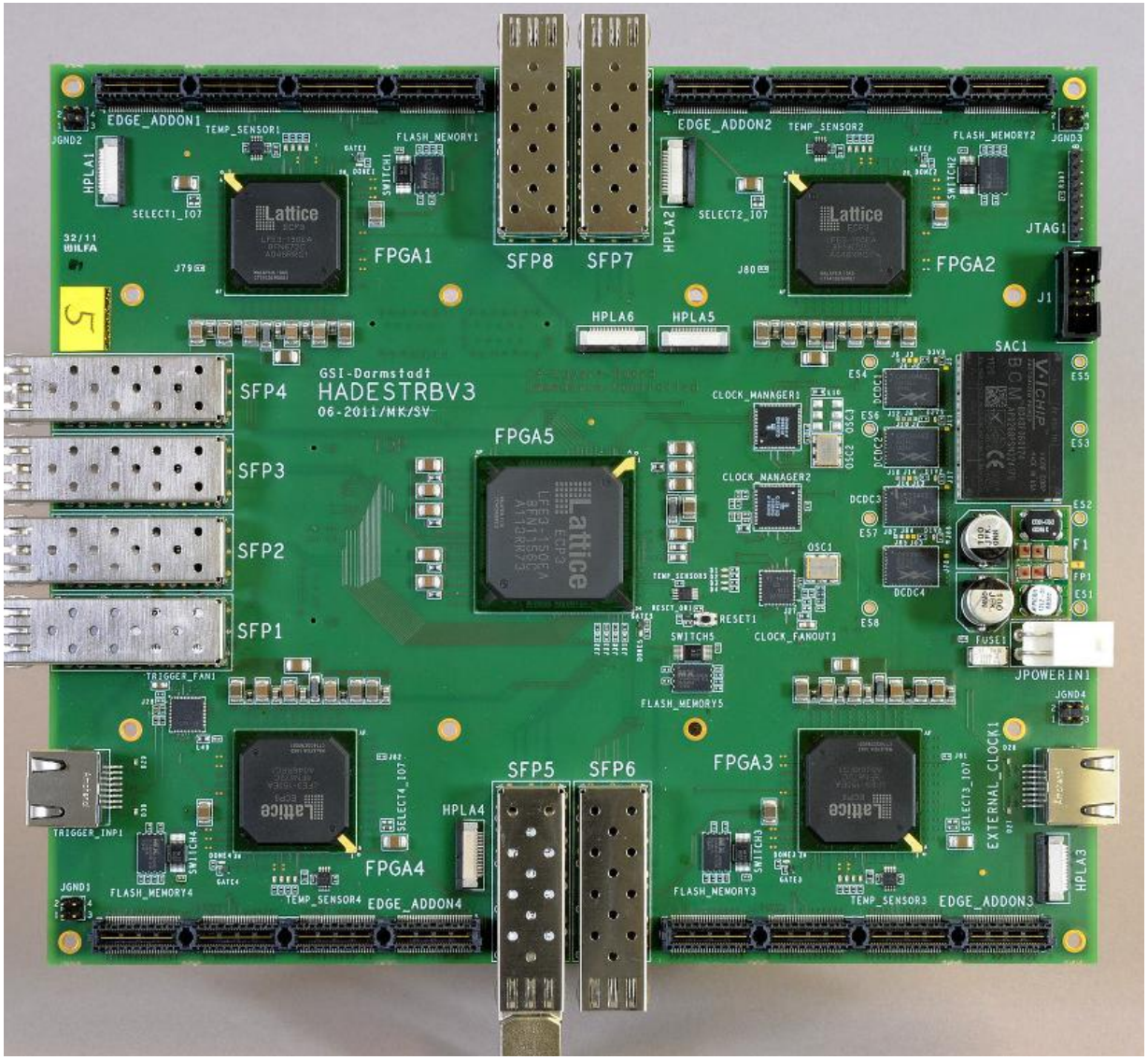
DAQ (TRBv3) preparation and FEE news

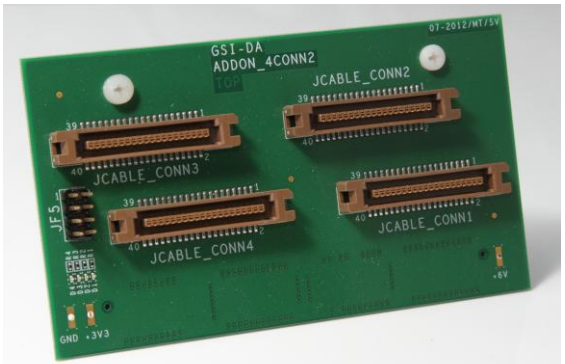




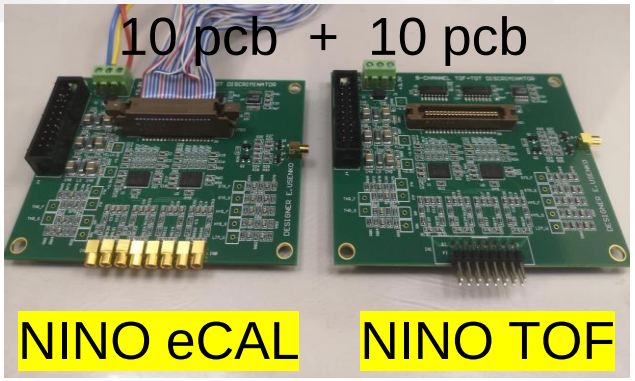


TRBv3


EDGE_ADDON1
EDGE_ADDON2
EDGE_ADDON3
EDGE_ADDON4
FPGA1
FPGA2
FPGA3
FPGA4
FPGA5
SFP1
SFP2
SFP3
SFP4
SFP5
SFP6
SFP7
SFP8
GSI-Darmstadt
HADESTRBV3
06-2011/MK/SV
JTAG1
SAC1
JPOWERIN1
TRIGGER_INP1
TRIGGER_FAN1
EXTERNAL_CLOCK1
CLOCK_MANAGER1
CLOCK_MANAGER2
CLOCK_FANOUT1
FLASH_MEMORY1
FLASH_MEMORY2
FLASH_MEMORY3
FLASH_MEMORY4
FLASH_MEMORY5
TEMP_SENSOR1
TEMP_SENSOR2
TEMP_SENSOR3
TEMP_SENSOR4


GSI-DA
ADDON_4CONN2
JCABLE_CONN2
JCABLE_CONN3
JCABLE_CONN4
JCABLE_CONN1


GSI-DA
JECL1
GPTN_ADDON1


10 pcb + 10 pcb
NINO eCAL
NINO TOF

TDC-Readout-Board, Triggered/Triggerless-Readout-Board

Item	Value
Supply Voltage	48 V (40-50V), galvanically isolated on board
Power Supply Current	0.5A minimum without AddOns
GbE-connectivity	max. 95 MBytes/s transfer per link
GbE-slow-control	up to 400 registers/transfer, speed depends on GbE latency
Connectivity	Max. 8 SFPs, each 2GBit/s on board. With hub-addon: max. 32 SFP
	4 AddONs on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate	about 300 KHz (depending on configuration and network size)
Max Hit Rate	50 MHz (burst of 63 hits)
TDC Channels	260 (Single edge detection)
Time Precision	<20 ps
Minimum pulse width	<500 ps

TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

WEB GUI

Threshold settings | TDC Regis

localho

Threshold Settings

Configuration	
Board	0311
DAC-Chain	1
Channel	1
Board Type	LTC242x DAC
Update Interval (ms)	500
Reference (mV)	3300
DiRich2 Flash:	Store Load
Last read	
Last set	12:46:47 PM
	OK

Coarse (0-65535)
Fine (0-255)

Shortcuts

- **c/v**: Increase/Decrease channel number
- **d/f**: Increase/Decrease chain number
- **Up/Down**: Increase/Decrease by 1
- **Shift + Up/Down**: Increase/Decrease by 16
- **PageUp/PageDown**: Increase/Decrease by 256
- **Shift + PageUp/PageDown**: Increase/Decrease by 2048
- **a/A**: Increase / Decrease board address
- **B/U/R**: Select input field
- **r**: Refresh values, read-back values from Padiwa

Threshold settings | TDC Registers | TDC Registers | TDC Registers

localhost:1234/tdc/tdc.htm

Configuration			
Board	0310		
Filter			
# of Channels	33		
Update Interval (ms)	1000	5000	
Split Table	☑	Differences	☑
Input Status	☑	Enable	☑
Hit Rate Status	☑		
	OK	RESET	

Reg	Channel	0310
	Channel group	3 2 1 0 on on on on off off off off
c000	0	31675
c001	1	0
c002	2	0
c003	3	0
c004	4	0
c005	5	0
c006	6	0
c007	7	0
c008	8	0
c009	9	0
c00a	10	0
c00b	11	0
c00c	12	0
c00d	13	0
c00e	14	0
c00f	15	☑ 31672
c010	16	☑ 31672
c011	17	0
c012	18	0
c013	19	0
c014	20	0
c015	21	0
c016	22	0
c017	23	0
c018	24	0
c019	25	0
c01a	26	0
c01b	27	0
c01c	28	0
c01d	29	0
c01e	30	0
c01f	31	☑ 31677
c020	32	☑ 31677

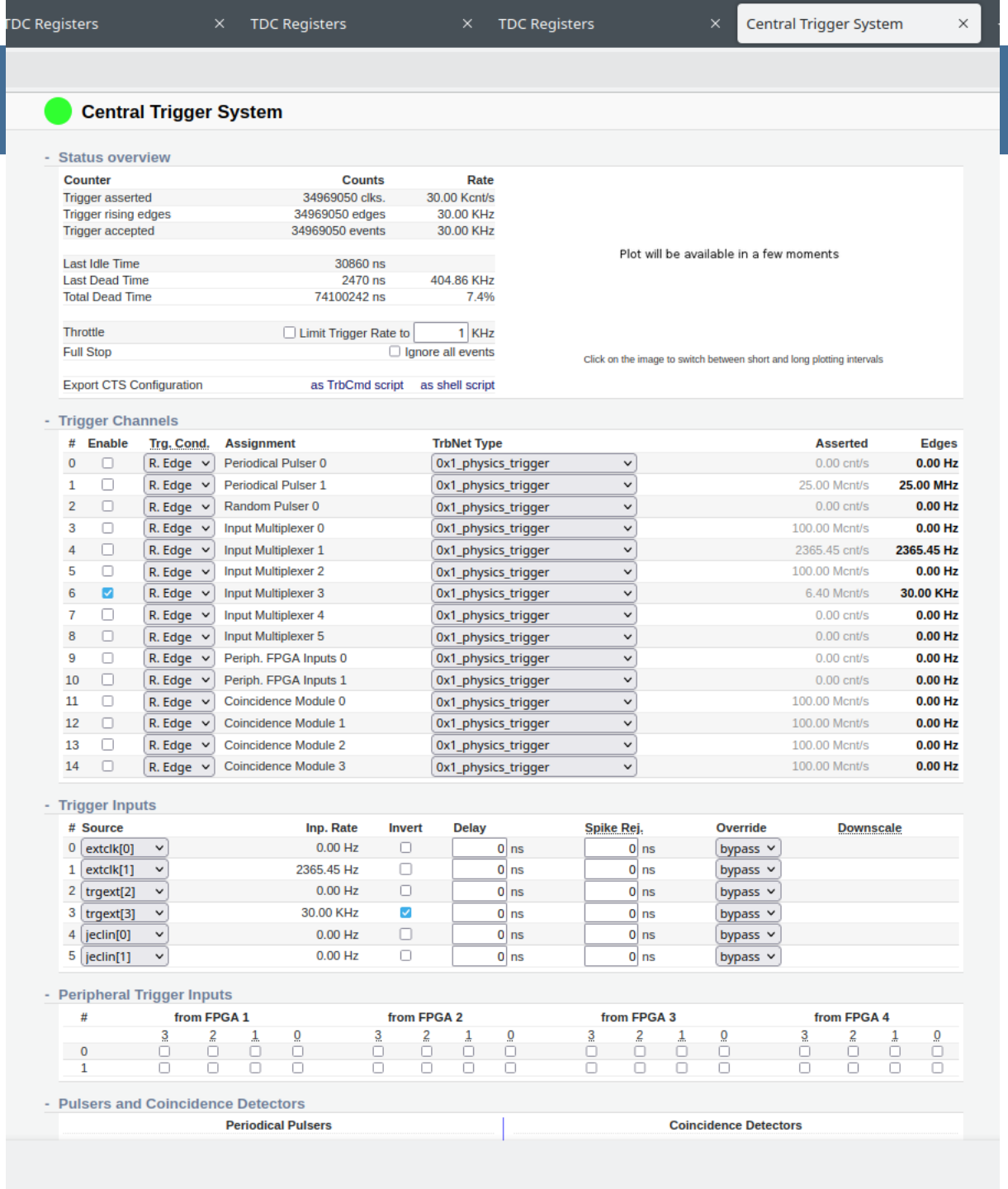
Reg	Content	0310
c100	tdc version channels ref input	2.1.5 32 polarity correct
c104	valid trg	14844561
c105	valid tmg trg	14844561
c106	valid notmg	0
c107	invalid trg	0
c108	multi trg	0
c109	spurious trg	0
c10a	wrong rdo	0
c10b	spikes	0
c10c	idle time	7274799
c10d	wait time	14227882
c10f	releases	14844561
c110	rdo time	412354
c111	timeout number	0
c112	data finished number	14844561

Reg	Content	0310
c800	Logic Anal. Debug Mode Calib. Prescaler	0 0 0
c801	window en. window bef. window aft.	Disabled on off 0 ns 0 ns
c802	act chan 1	0xc000c000
c803	act chan 2	0x0
c804	data limit	8
c805	inv chan 1	0x0
c806	inv chan 2	0x0

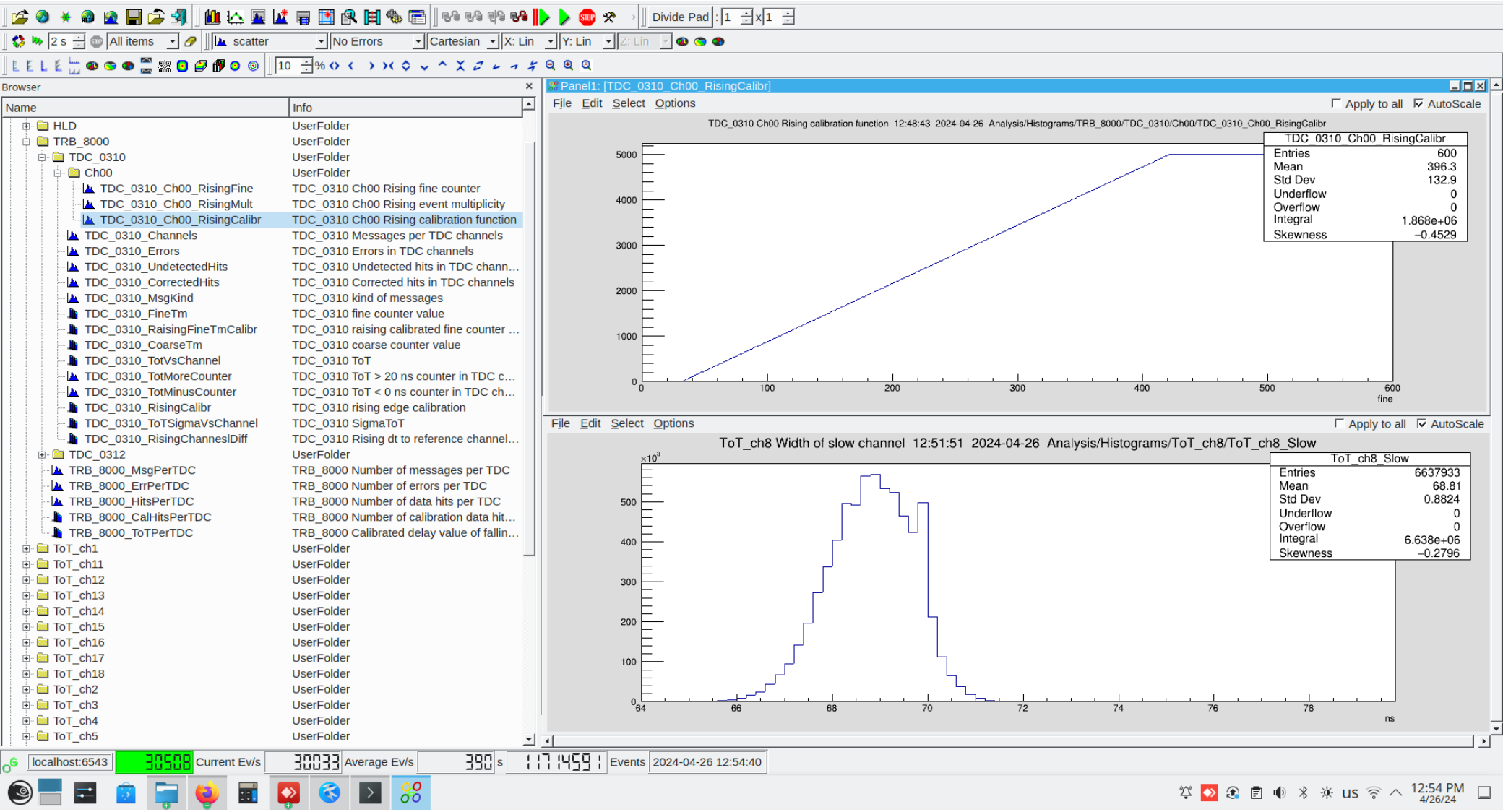
WEB CTS

ZOO on SUSE Tumbleweed:

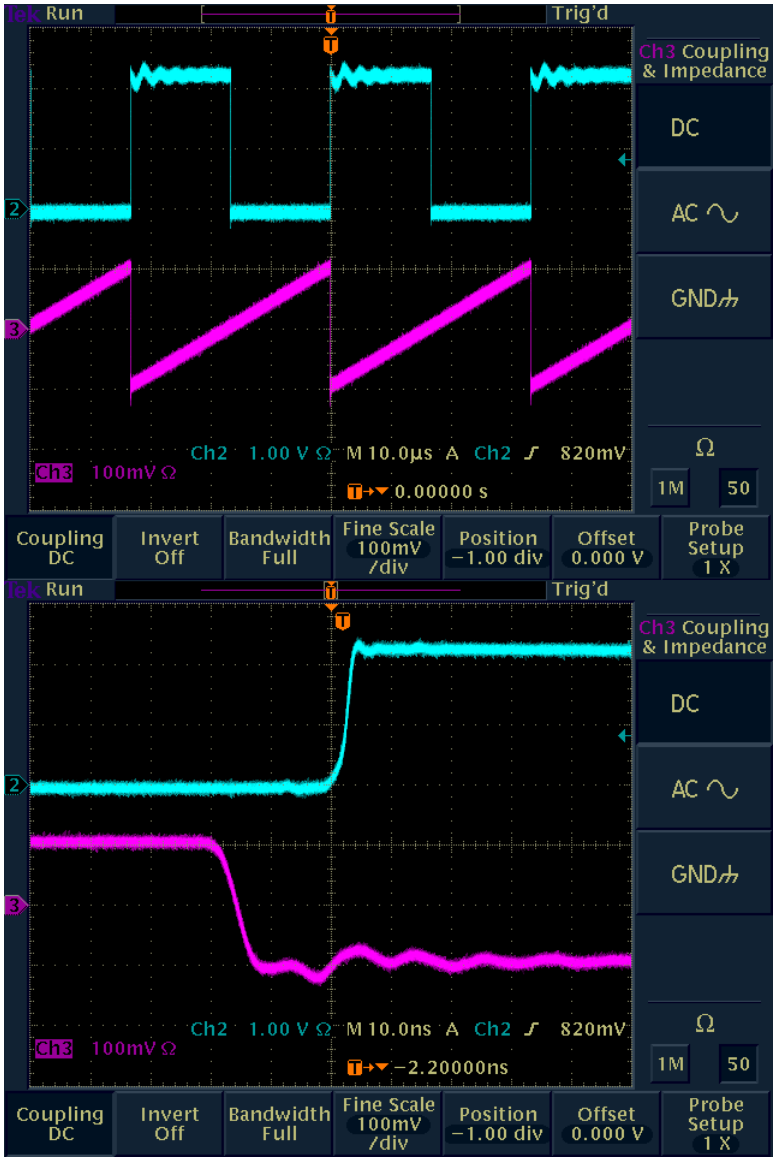
- **VHDL** is ranging from the system level down to that of logic gates, for design entry, documentation, and verification purposes.
- **Perl** Practical Extraction and Report Language.
- **XML** ExtensibleMarkupLanguage for storing, transmitting, and reconstructing arbitrary data.
- **C++** (ROOT etc.)



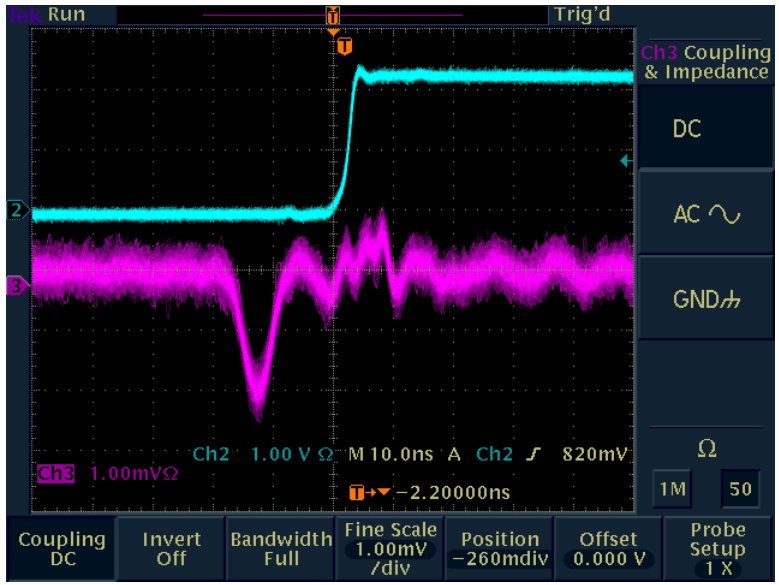
GO4 for data visualization and analysis



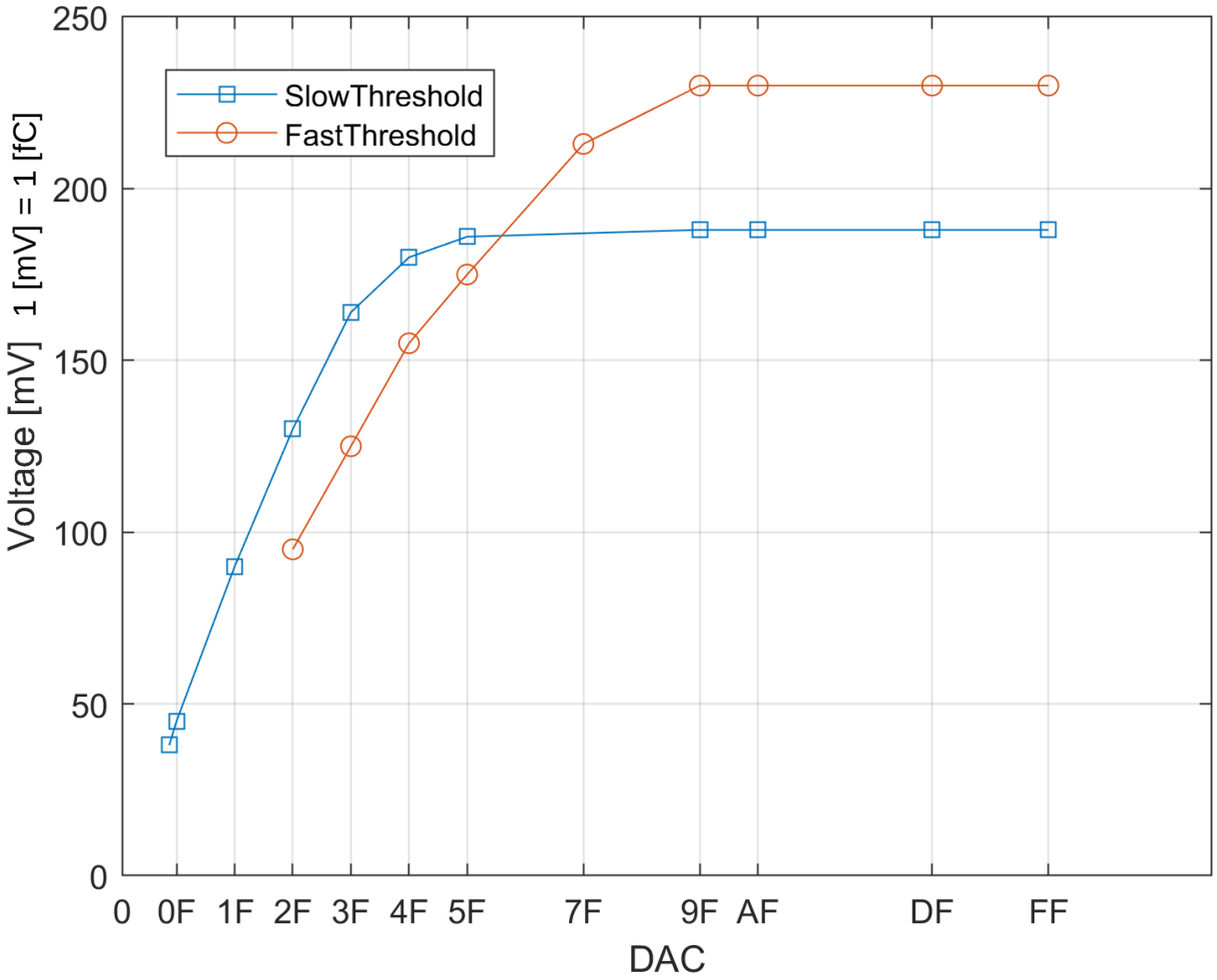
Test signal forming chains and key parameters

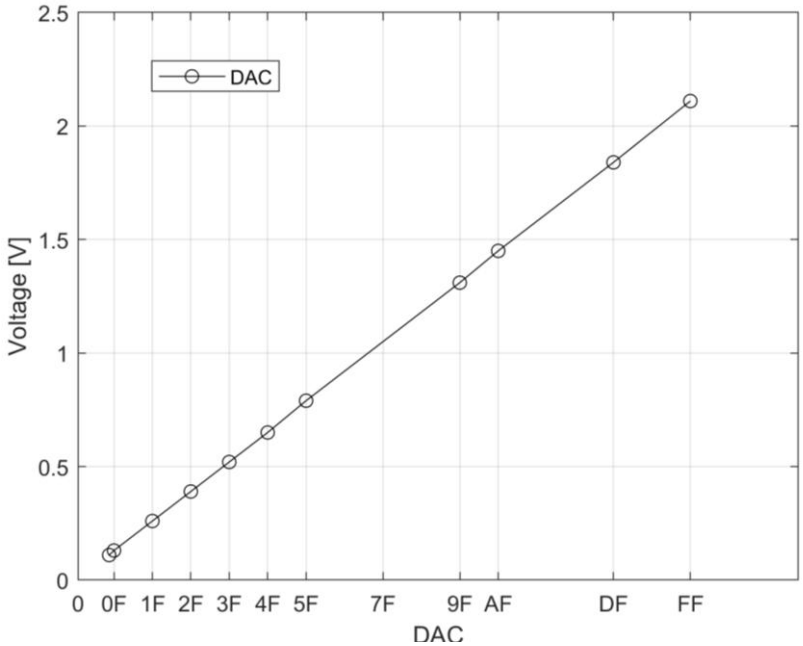


1 pF diff capacitance → 200mV = 200 fC



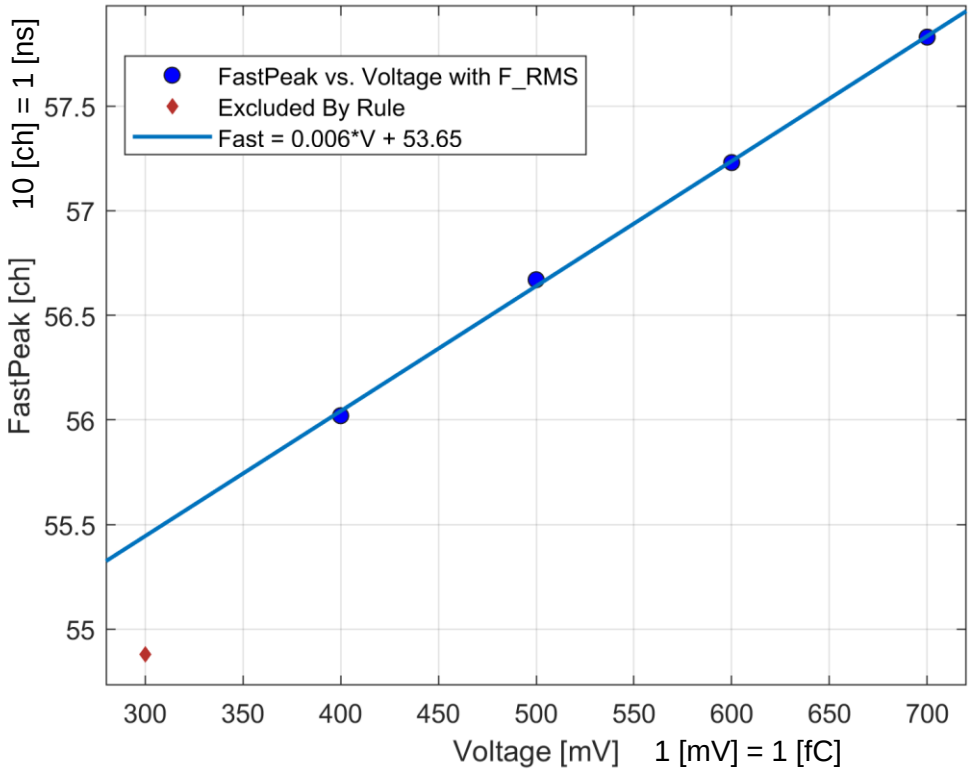
Threshold for Fast and Slow FEE output





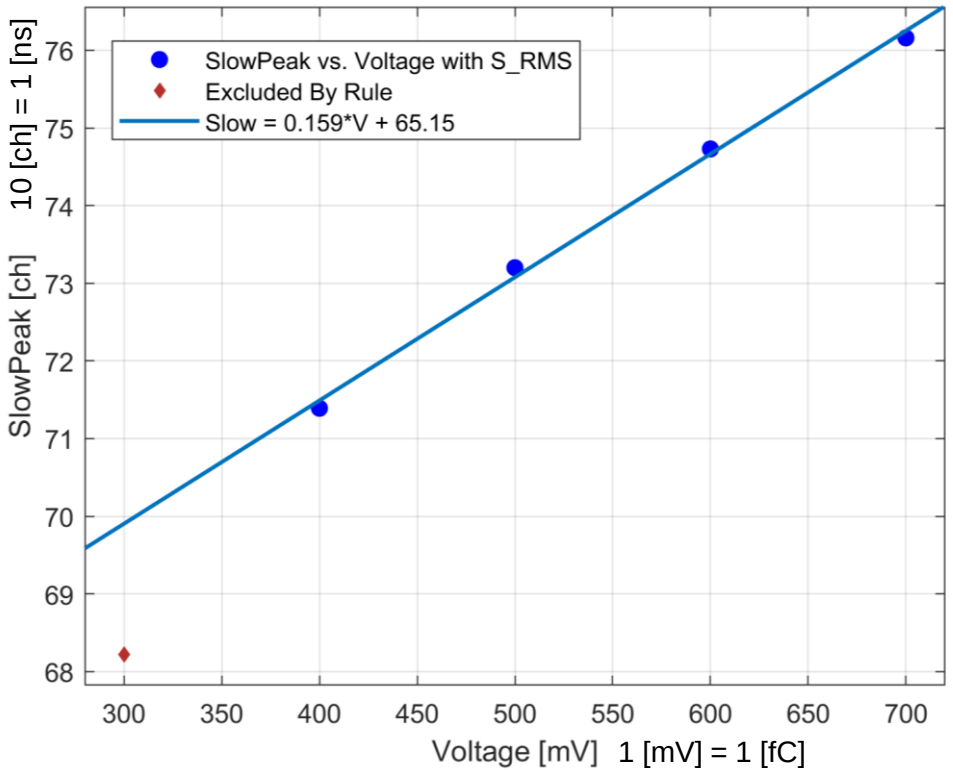
Counts on Fast and after for Slow channels becomes equal to triggers number (Threshold)

Linear response to test signal for Fast and Slow output



Fast peak width 5.5-6ns STD<100ps

Slow peak width 7-7.6ns STD<90ps



Possible FEE and Digitization

https://www.caen.it/subfamilies/fers-5200/

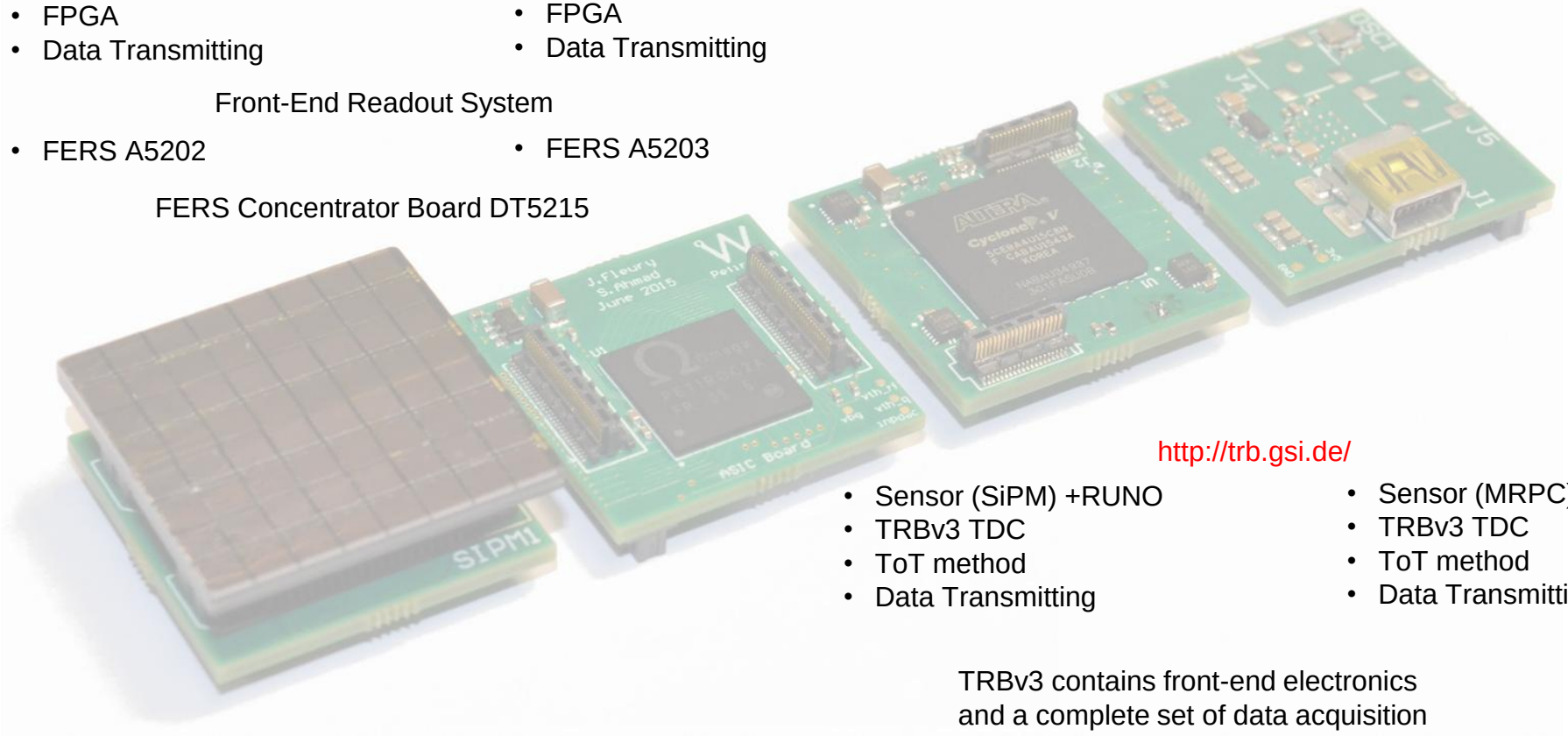
- Sensor (SiPM)
- ASIC (WEEROC family, citiroc-1A)
- FPGA
- Data Transmitting

- Sensor (MRPC) + NINO
- ASIC (picoTDC)
- FPGA
- Data Transmitting

Front-End Readout System

- FERS A5202
- FERS A5203

FERS Concentrator Board DT5215



http://trb.gsi.de/

- Sensor (SiPM) +RUNO
- TRBv3 TDC
- ToT method
- Data Transmitting

- Sensor (MRPC) + RUNO
- TRBv3 TDC
- ToT method
- Data Transmitting

TRBv3 contains front-end electronics and a complete set of data acquisition and control software.

FERS FERS+NINO vs. TRBv3 FPGA-TDC+RUNO

The only way to do great work is to love what you do. © S.J.

- **Artem Semak, Evgeni Ladygin**

- **Sergei Morozov, Evgeni Usenko**

- **Artem Ivanov**
- **Vladimir Ladygin, Aleksey Tishevsky**
- **Vadim Babkin, Mikhail Buryakov, Sviatoslav Buzin**

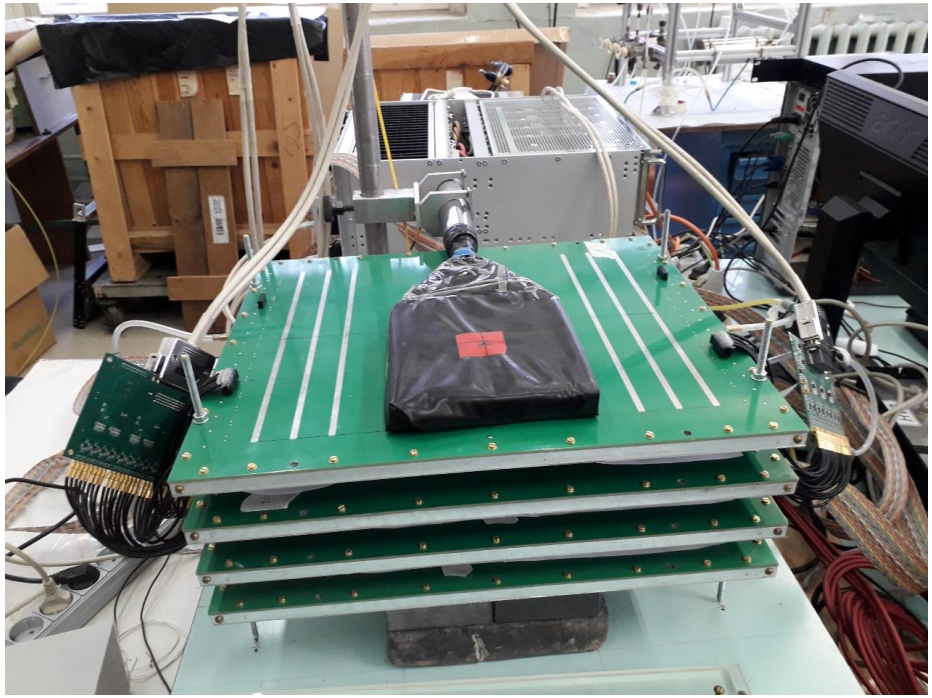
- **Yi Wang at al.**

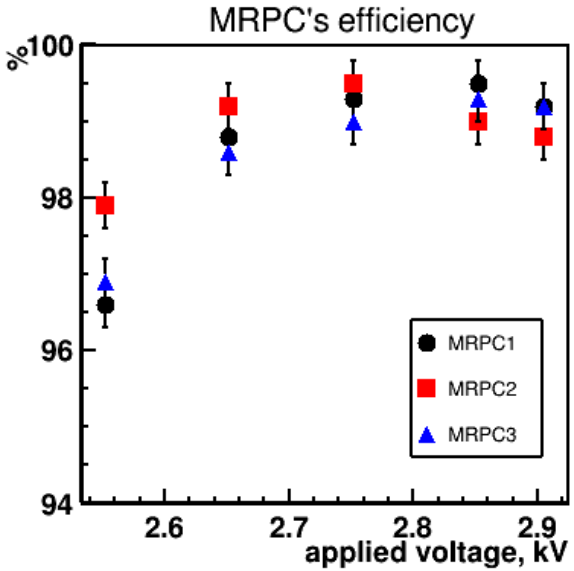
- **Michael Traxler & the TEAM**

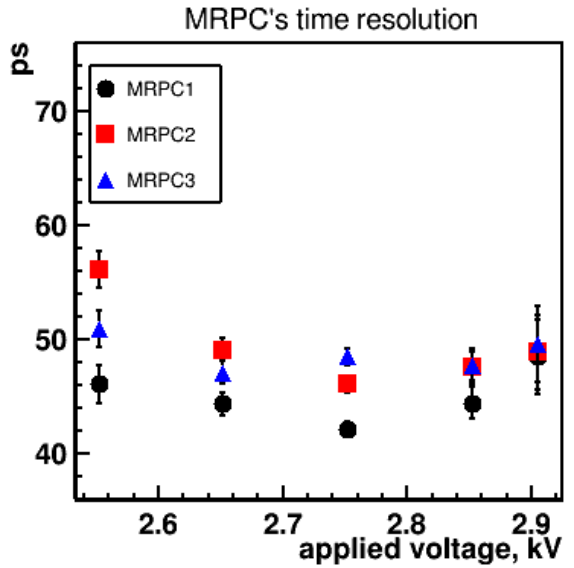
Thank you for your attention

Spare slides

Protvino MRPC prototype for SPD project at NICA

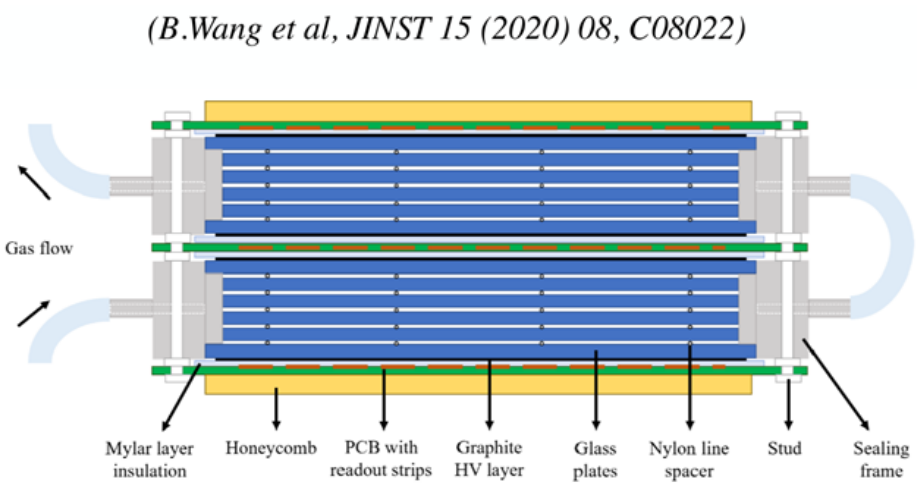


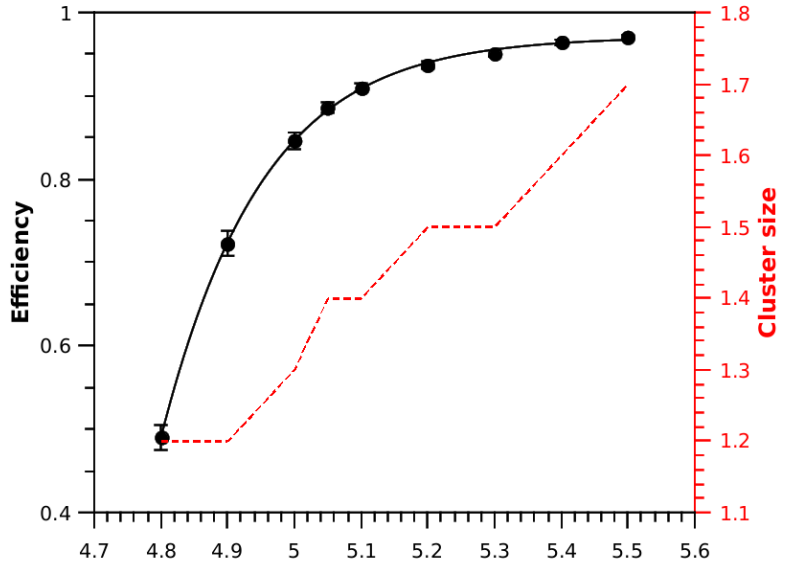




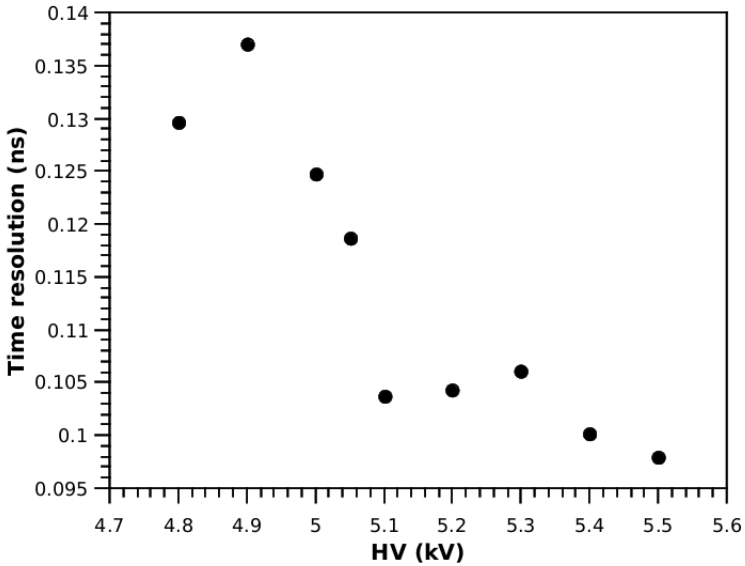
- To start MRPC and check functionality
- To obtain detection efficiency and time resolution on a new DAQ
- Preparation for using 3 MRPC as a servicing system at TEST AREA (Anton Baldin).

Sealed (MRPC) are the base option of today





- The prototype was tested in cosmic rays along with 2 MRPC2 counters in the TRBv3 test stand.
- The plateau efficiency is 97%, with a 1.6 cluster size and a 100 ps flight-time resolution.
- The systematic time resolution of the prototype is about 60 ps. if we reasonably expect the same timing precision between two MRPCs.
- The prototype has the same working point at ±5.4 kV with standard gas flow (Freon/iC_4H_{10} = 90/5/5



DiRICH

The DiRICH module is a 32-channel transformer, amplifier (factor 30), discriminator (with thresholds settings), **0ps RMS** time precision TDC (currently, can be improved) and finally readout of the data via TRBNet. So, it is an improved version of the combination of a Padiwa + a small part of the TRB3.