Status of L1 concentrator

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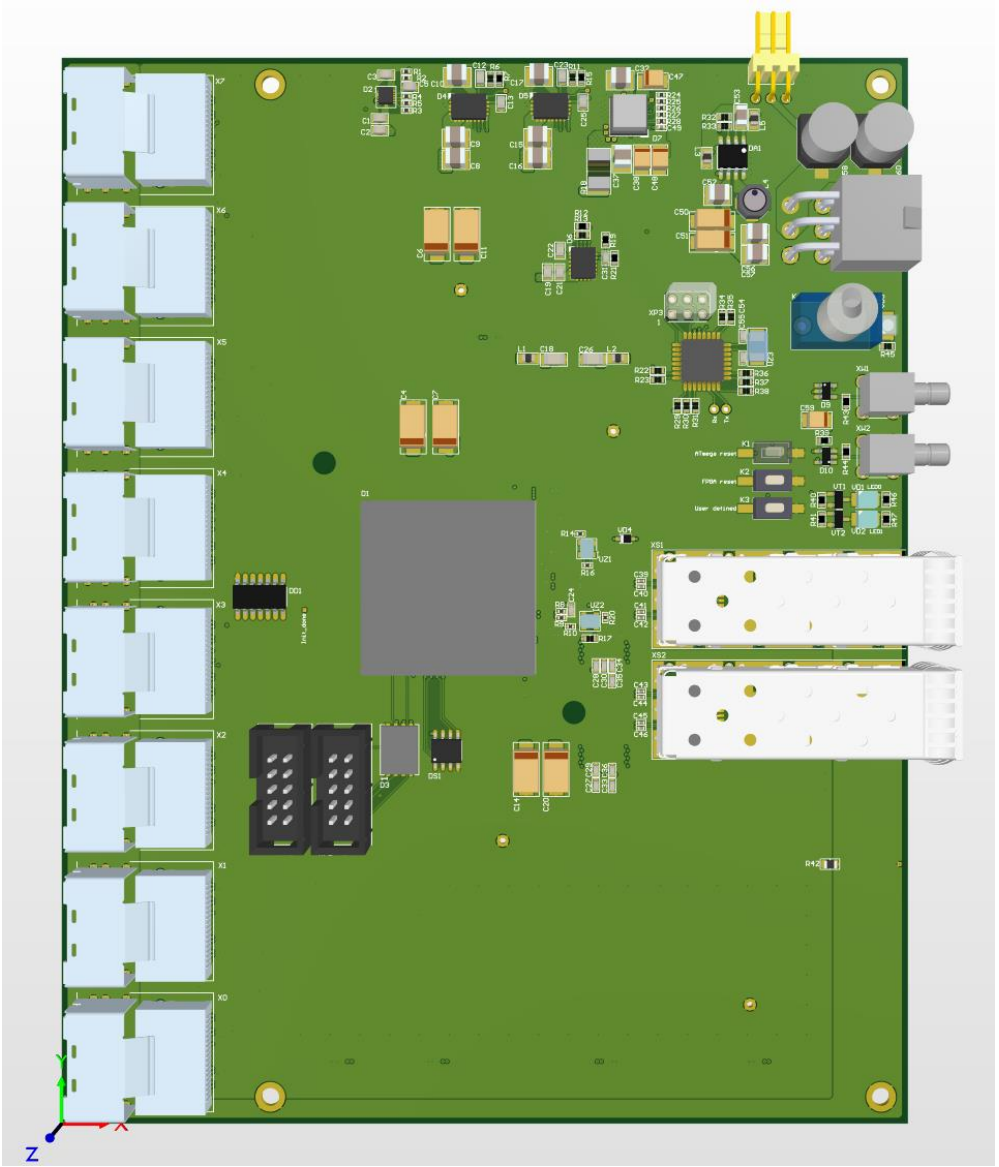
PCB of L1 concentrator (prototype)

- Cyclone 10GX (105YF780E6G)
- 8x Links for connect front-end boards (miniSAS* connectors) 8 diff pairs per connector
- SFP+ 10Gb transceiver for data transmission to L2
- SFP+ 10Gb transceiver for TSS (White Rabbit)

Concentrator tasks:

- Collecting data from the front-end boards.
- Distribution of clock from TSS.
- Distribution of commands from TSS.
- Data integrity and timestamp control.
- Reconfiguring front-end boards (firmware)?



*(*additional info on presentation slide 6*)

L1 Firmware (first iteration)

First version of modules

Ready:

✓ 10G Link (UPD packet, ARP, PING) – Without Soft-Core processor.

✓ Data collect module for custom protocol*.

✓ I2C master for slow control command. (can be change to another protocol)

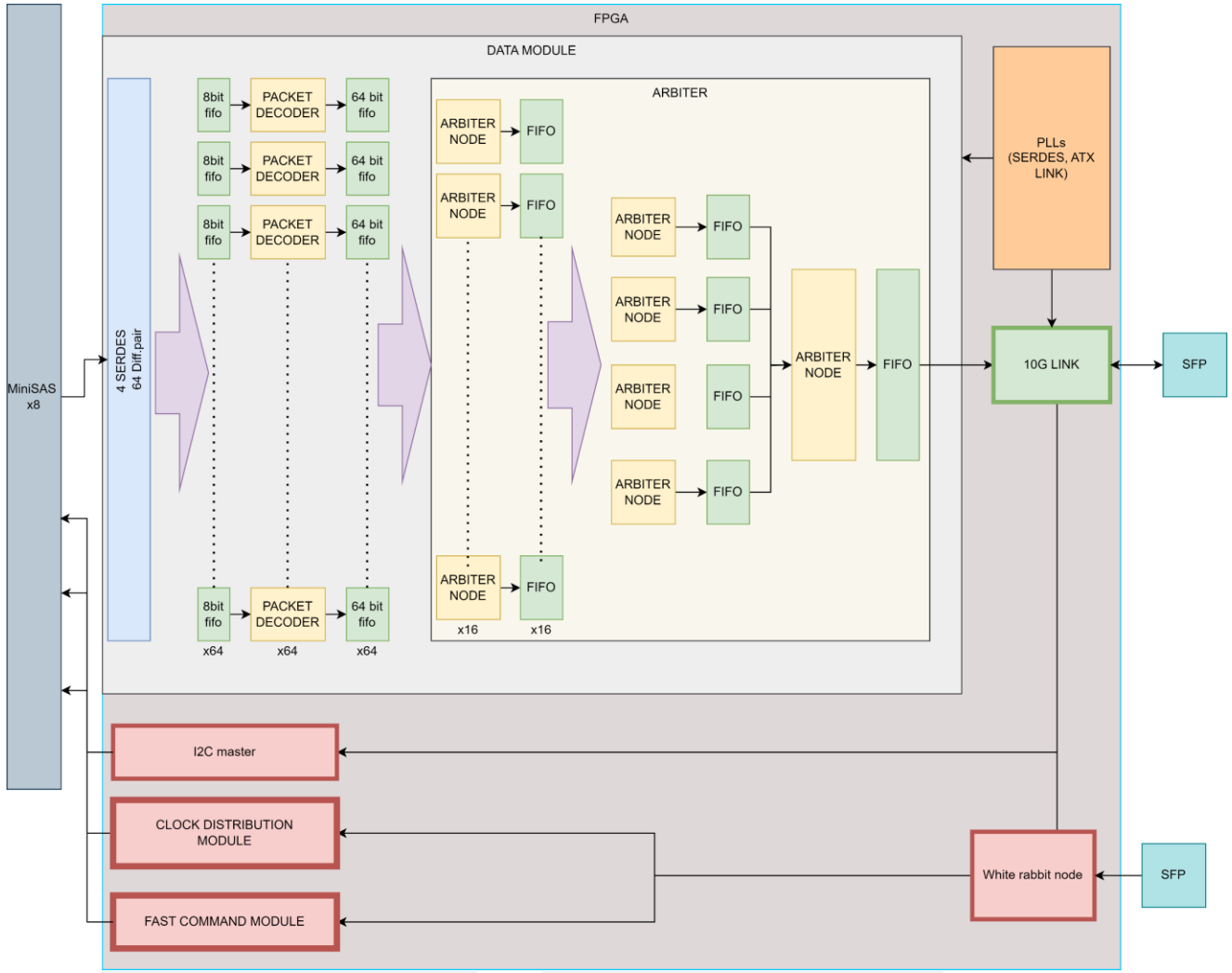
Not ready:

X TSS node (SPbPU will provide).

X Clock distribution module.

X Fast command module.

X Another optional modules.



Family	Cyclone 10 GX
Device	10CX105YF780E6G
Timing Models	Final
Power Models	Final
Device Status	Final
Logic utilization (in ALMs)	15,615 / 38,000 (41 %)
Total registers	37852
Total pins	195 / 340 (57 %)

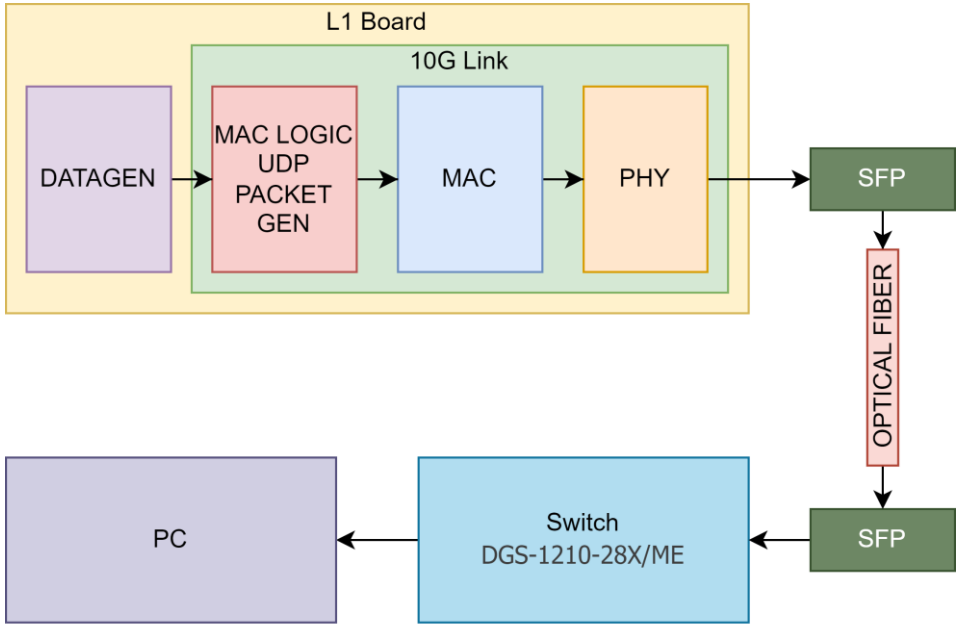
Total virtual pins	0
Total block memory bits	2,640,816 / 7,823,360 (34 %)
Total RAM Blocks	292 / 382 (76 %)
Total DSP Blocks	0 / 125 (0 %)
Total HSSI RX channels	1 / 12 (8 %)
Total HSSI TX channels	1 / 12 (8 %)
Total PLLs	8 / 30 (27 %)

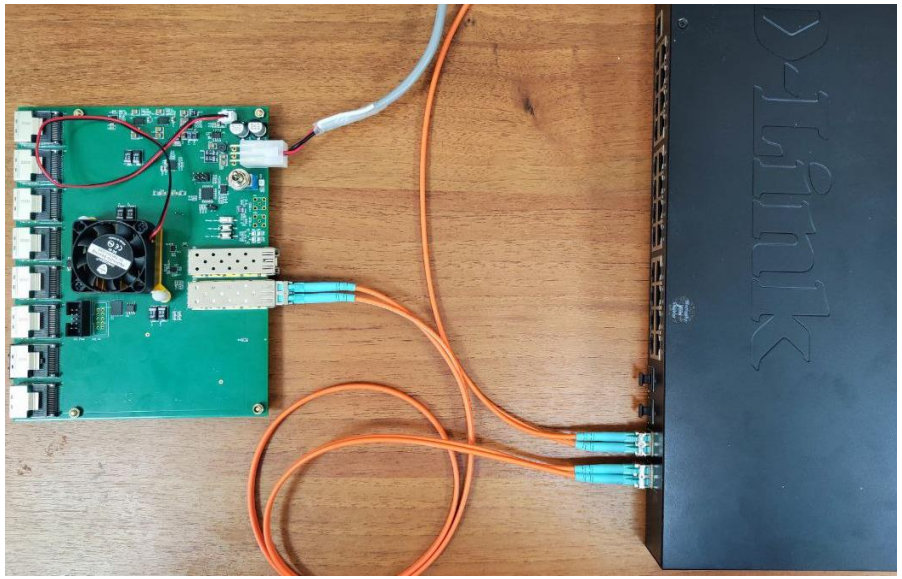
System Verilog based Firmware

*appended start and end byte into to data (*additional info on presentation slide 7*)

10G Link *Bandwidth measurement*

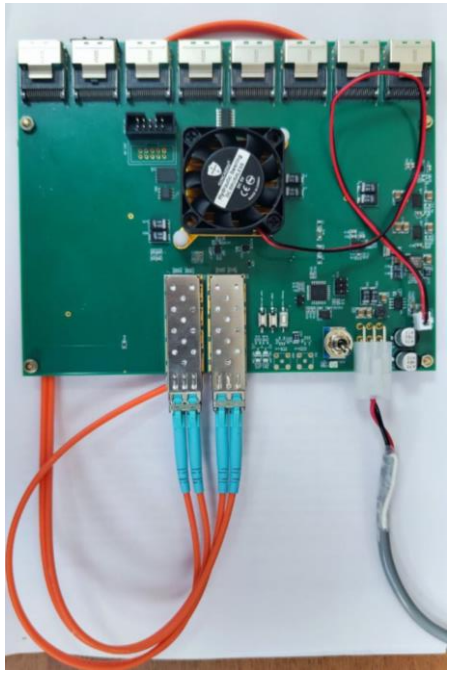
- SFP: Finisar FTLX8571D3BCV
- SWITCH: D-LINK DGS-1210-28X
- One hour test average bandwidth (speed): 9.928551 Gbit/sec
  - UPD packet
  - Fixed packet size: 1518 bytes
- Average bandwidth (speed) for payload : 9.876227 Gbit/sec

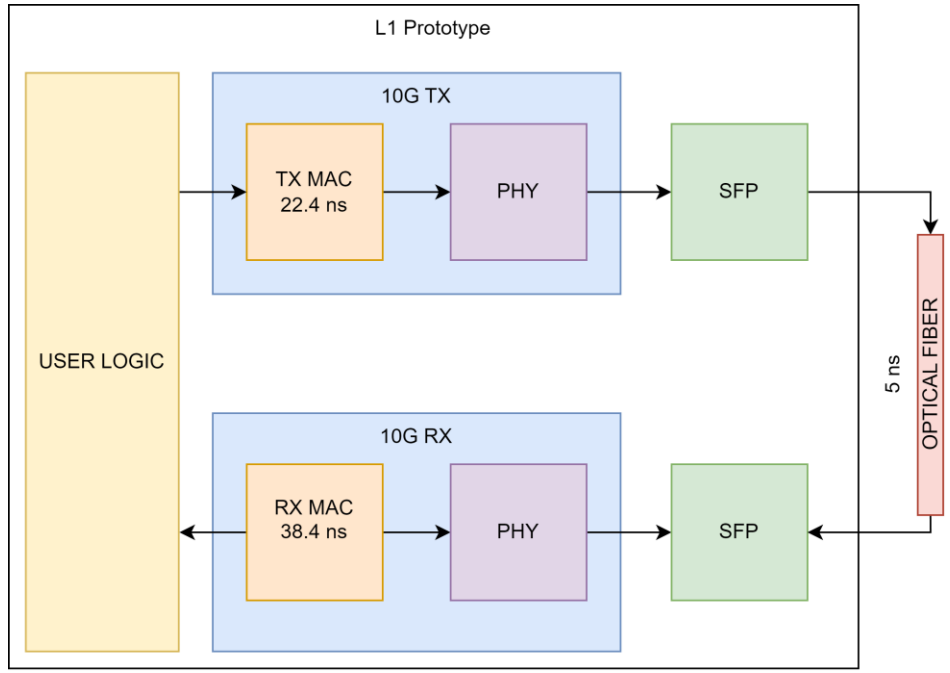




10G Link *Latency measurement*

- Test in loopback mode
- Fiber length: 1m
- SFP: Finisar FTLX8571D3BCV (850 nm)
  - Max fiber length: 300m
  - Consumed: 1 watt

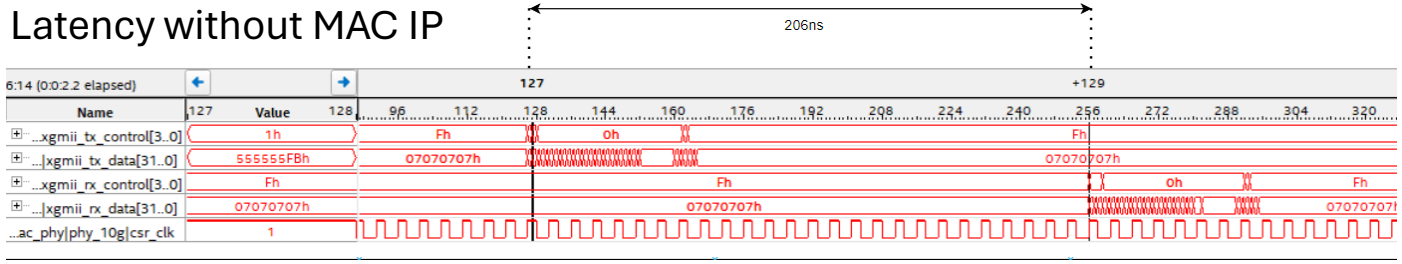




Total delay TX to RX: ≈ 266.8 ns

• Fiber:	≈ 5 ns
• TX MAC	22.4 ns
• RX MAC	38.4 ns
• PHY + SFP	≈ 2x100 ns

Latency without MAC IP



E-Link *port*

DisplayPort (TDR v1.00)

FrontEnd DisplayPort Connector		
Signal Type	Pin Name	Pin
GND	GND	2
Out	ML_Lane 0 (p)	1
Out	ML_Lane 0 (n)	3
GND	GND	5
In	ML_Lane 1 (p)	4
In	ML_Lane 1 (n)	6
GND	GND	8
In	ML_Lane 2 (p)	7
In	ML_Lane 2 (n)	9
GND	GND	19
In	Hot Plug Detect	18
IO	CONFIG1	13
In	CONFIG2	14
GND	GND	11
In	ML_Lane 3 (p)	10
In	ML_Lane 3 (n)	12
GND	GND	16
In	AUX_CH (p)	15
In	AUX_CH (n)	17
	DP_PWR	20

Data e-link

Start of slice

Start of frame

Reset

I2C SDA SCL

Set Next Frame

Global clock

spare signal

Changed connector

+3 Diff Pair
+5 Unipolar

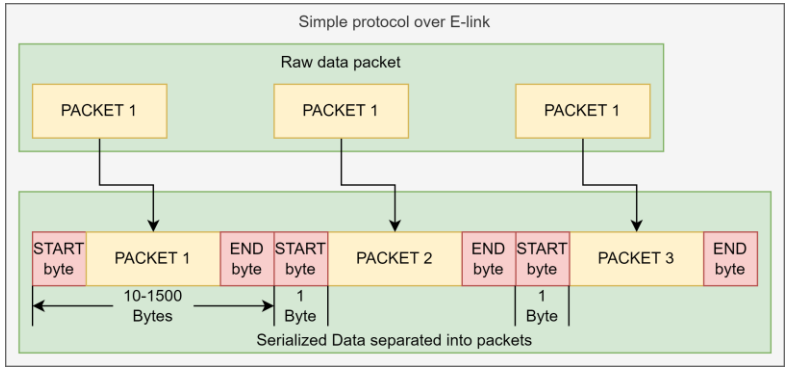
Dedicated line for:
- Start of slice
- Start of frame
- Set Next Frame
- Global clock from L1 to Front-End

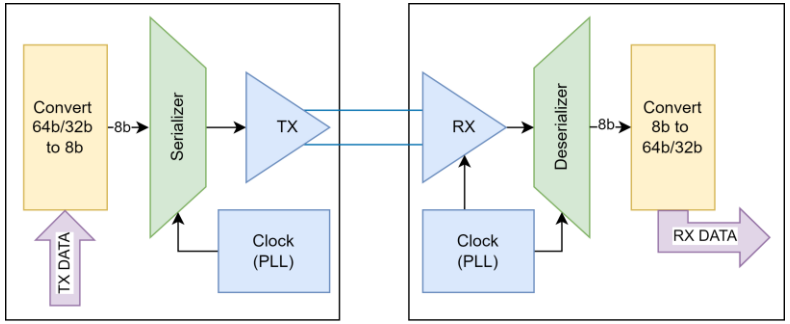
- Clock for data. From Front-End to L1
- Three data lines (Max 1250 Mbps)
- 8 Unipolar lines for slow interface and different signals

MiniSAS

Pin function	Side B Pin	Side A Pin	Pin function
GND	B1	A1	GND
Tx0+	B2	A2	Rx0+
Tx0-	B3	A3	Rx0-
GND	B4	A4	GND
Tx1+	B5	A5	Rx1+
Tx1-	B6	A6	Rx1-
GND	B7	A7	GND
Unipolar 0	B8	A8	Unipolar 7
Unipolar 1	B9	A9	Unipolar 3
Unipolar 2	B10	A10	Unipolar 4
Unipolar 6	B11	A11	Unipolar 5
GND	B12	A12	GND
Tx2+	B13	A13	Rx2+
Tx2-	B14	A14	Rx2-
GND	B15	A15	GND
Tx3+	B16	A16	Rx3+
Tx3-	B17	A17	Rx3-
GND	B18	A18	GND

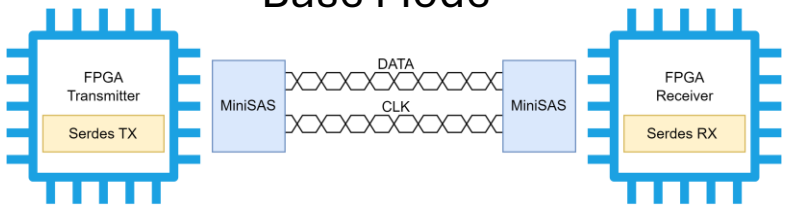
E-Link *data serialization (options)*

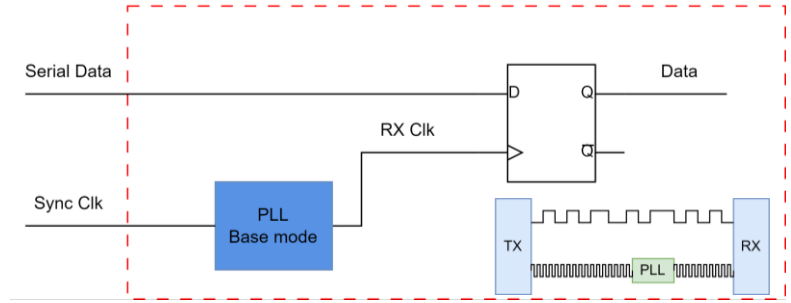




A simple transfer protocol was prepared for first test. In data append start and end bytes for data packet separation.
Data serialize and send over MiniSAS cable.

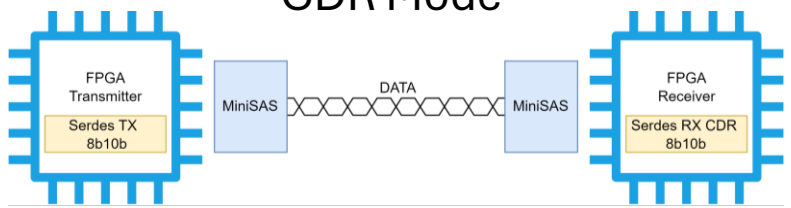
Base Mode

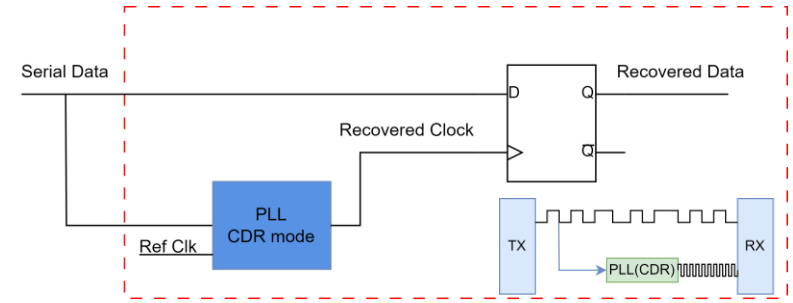




Base serial mode – using dedicated lines for data and synchronization clock for transfer. Stable for high bandwidth and long line due to dedicated clock line.

CDR Mode





CDR (clock data recovery) mode – using one line for transfer. Clock is recovered from data*. Phase of recovered clock is synchronizing with reference clock.
Increased jitter requirement for the source.

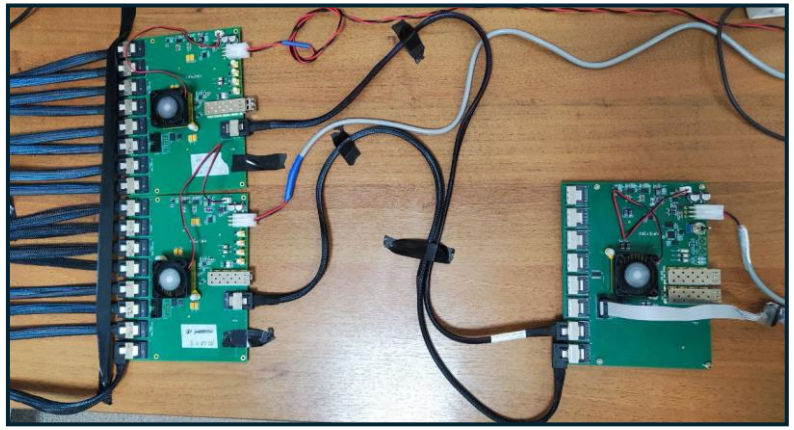
*The Front-end should implement serialize procedure with 8b/10b encoding.

E-Link *test*

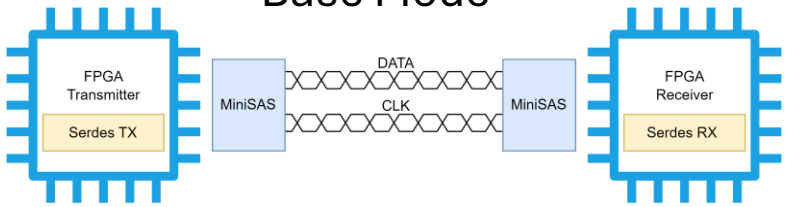
Setup

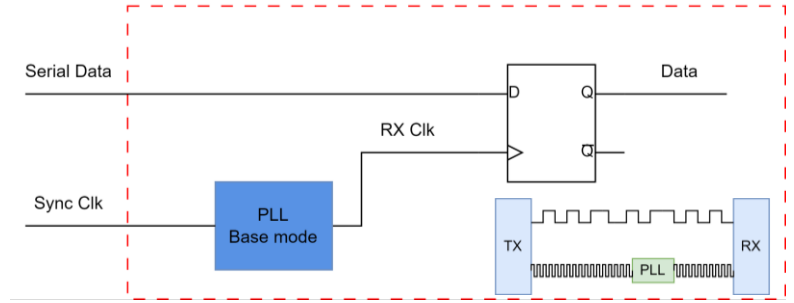
1. Two data generator boards
2. L1 concentrator prototype
3. Two MiniSAS cable (1m)
4. 24 hour test for each modes

Monitoring via JTAG



Base Mode

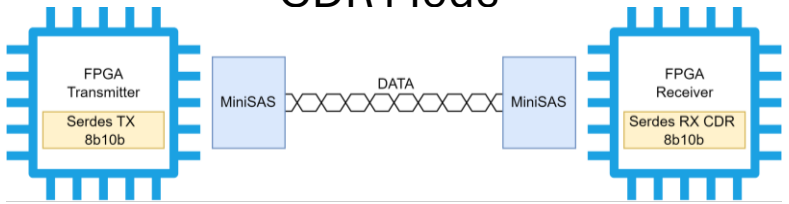


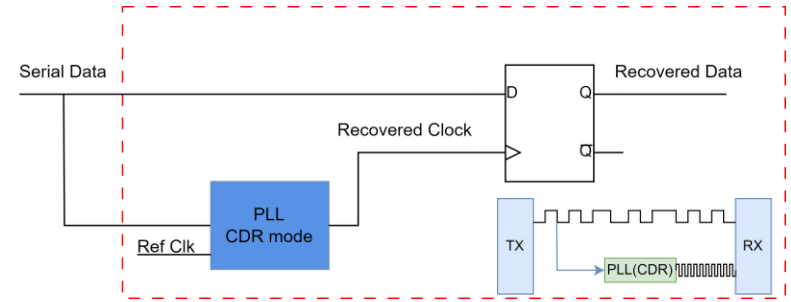


Link bandwidth per line:

150 Mbps – OK
500 Mbps – OK
750 Mbps – OK
1000 Mbps – OK
1250 Mbps – OK

CDR Mode





Link bandwidth per line*:

150 Mbps – OK
500 Mbps – OK
600 Mbps – OK
750 Mbps – ERRORS
1000 Mbps – ERRORS

*may reach 1200 Mbps after modifications

Thanks for your attention

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