National Research Tomsk State University

L2 concentrator firmware

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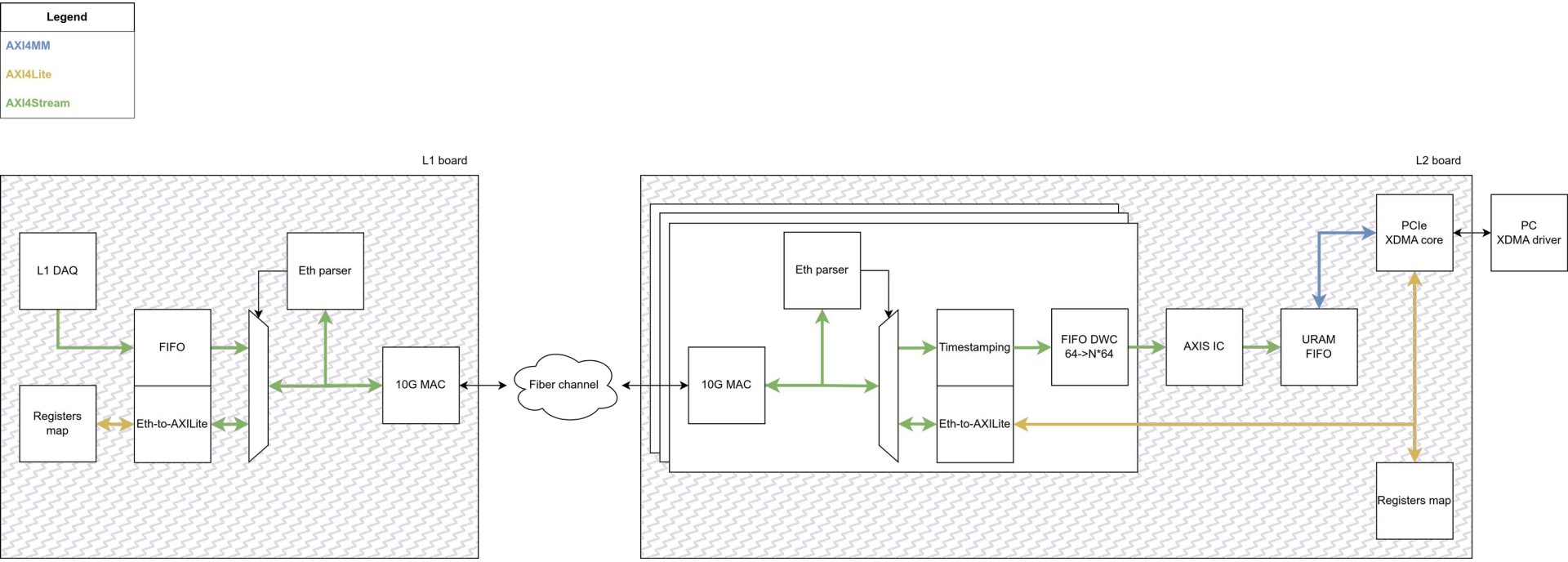
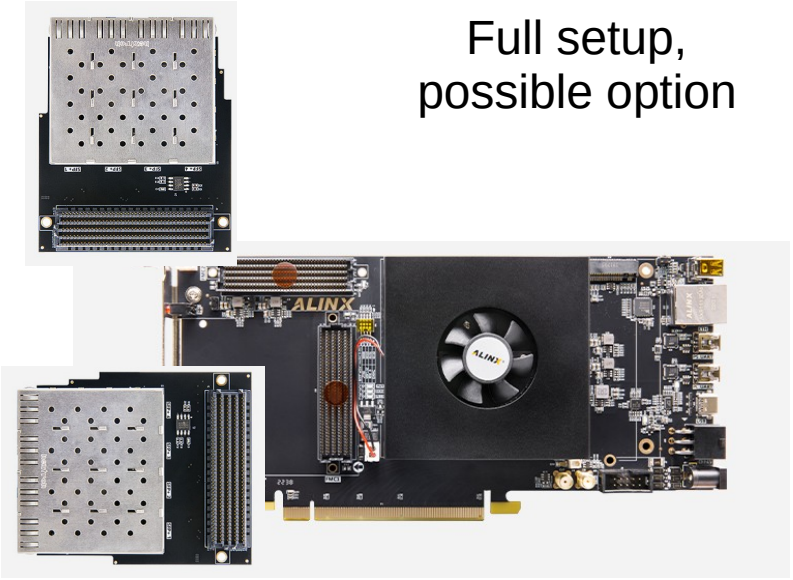
L2 FPGA architecture



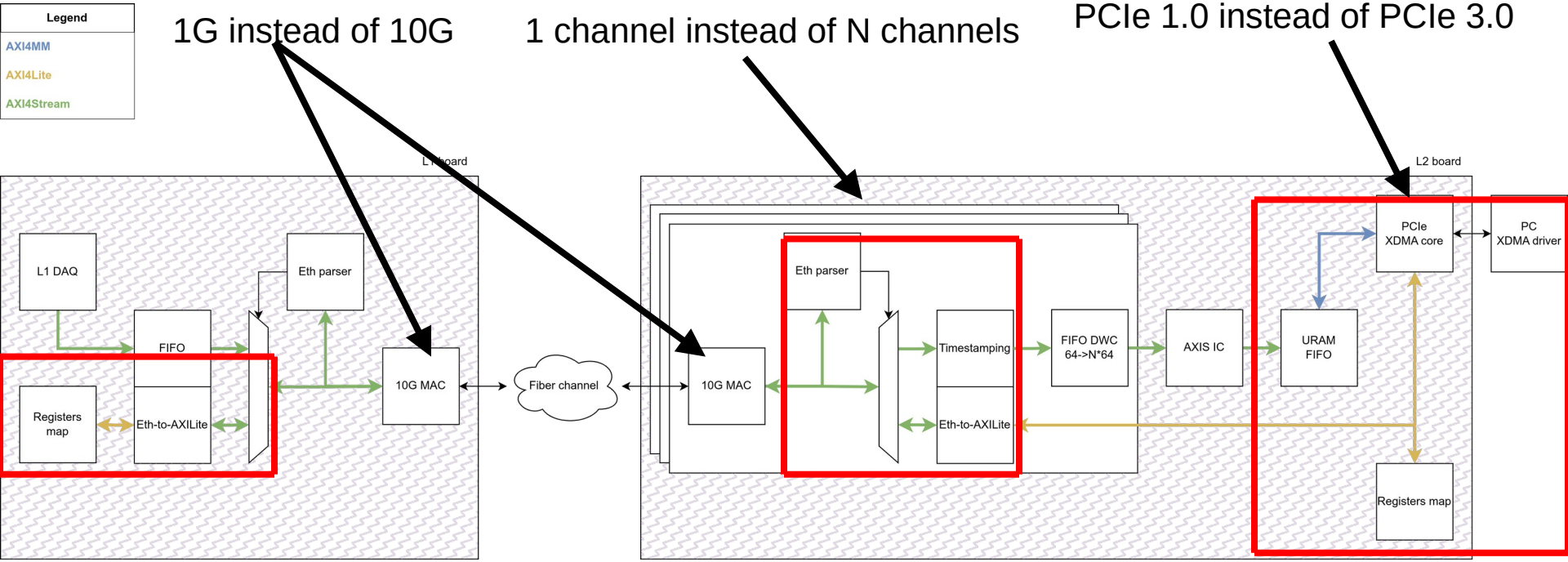
Platform

Limited setup,
Xilinx’s analog

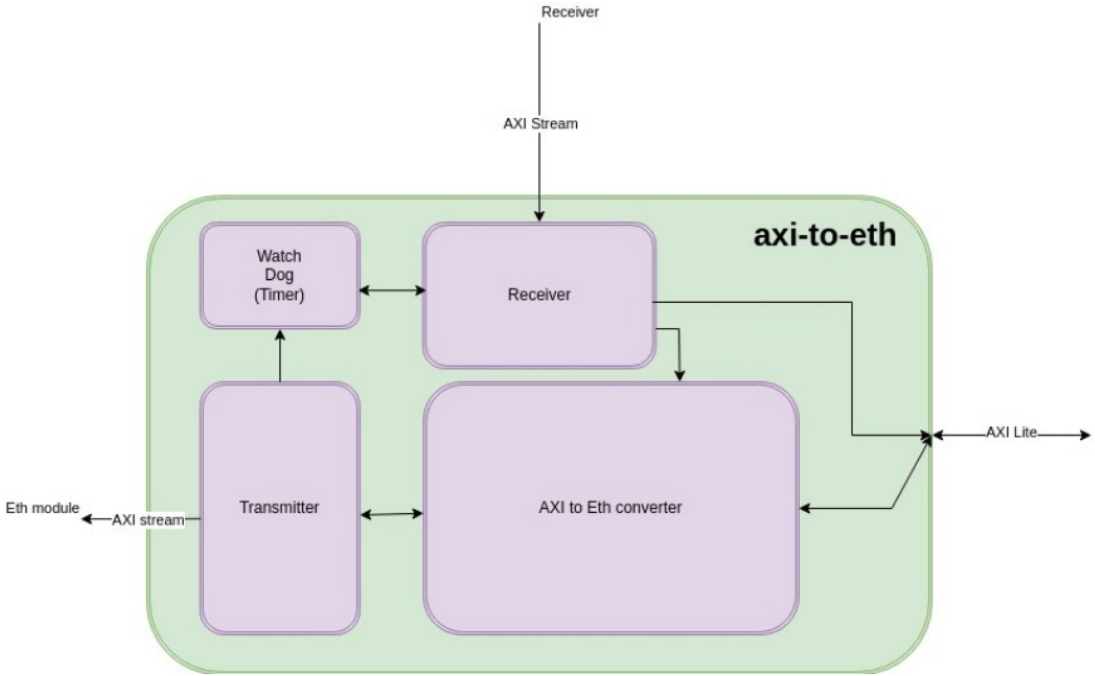
Full setup,
possible option



L2 FPGA progress. Limited setup



AXI-Ethernet transport

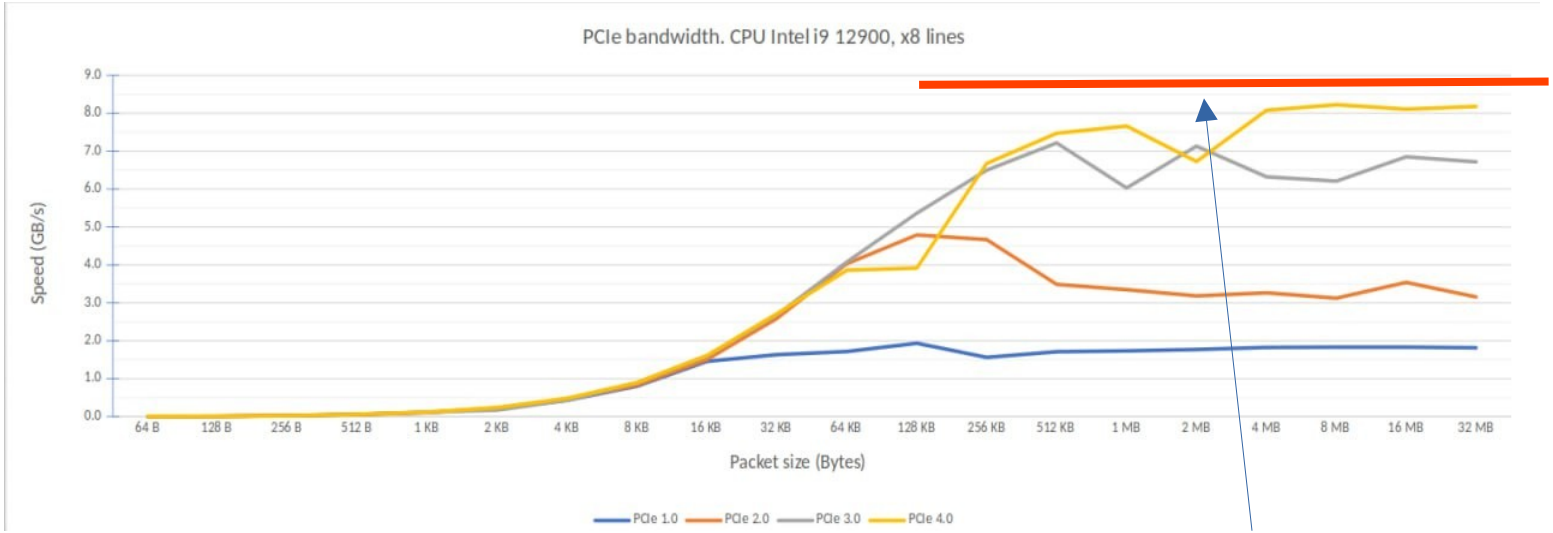


Receiving logic: prepared ethernet frame gets converted to AXI Lite

Sending logic: AXI Lite command is converted to the Ethernet frame and then gets sent by the Ethernet interface

PCI C2H bandwidth

Preliminarily result with various PCIe configuration



Kind of “bottleneck” because of CPU (100% load at this point). Might be investigated and optimized in case of needs