Передовые инженерные школы

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Peter the Great St.Petersburg Polytechnic University

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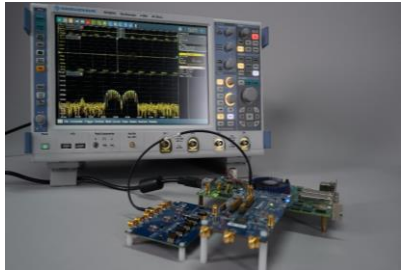
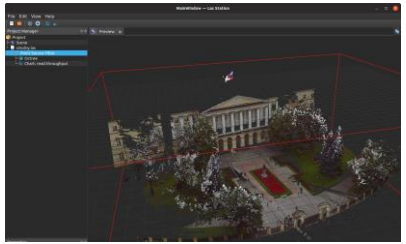
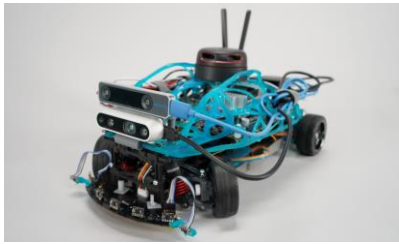
WCRC
ADVANCED DIGITAL TECHNOLOGIES

POLYTECH
Advanced Manufacturing Technologies Center
National Technology Initiative

POLYTECH
Laboratory
Industrial Systems for Streaming Data Processing



SPD-meeting

20 may 2024

Current status of TSS development. TSS control protocol

Industrial Systems for Streaming Data Processing Laboratory,
“Digital Engineering” Advanced Engineering School, SPbPU

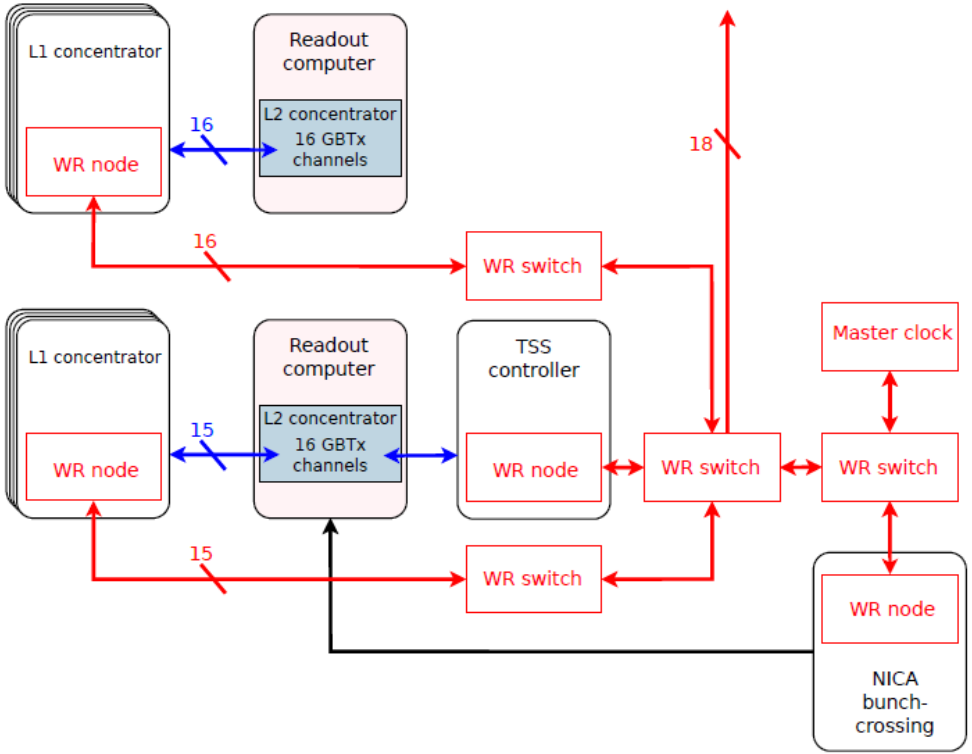
Presentation brief

- TSS subsystem – refresher
- White Rabbit technology – refresher
- SyncTechnology WR-devices – test setup and evaluation results
- TSS-protocol – requirements
- Current development work and prospects

Time Synchronization System

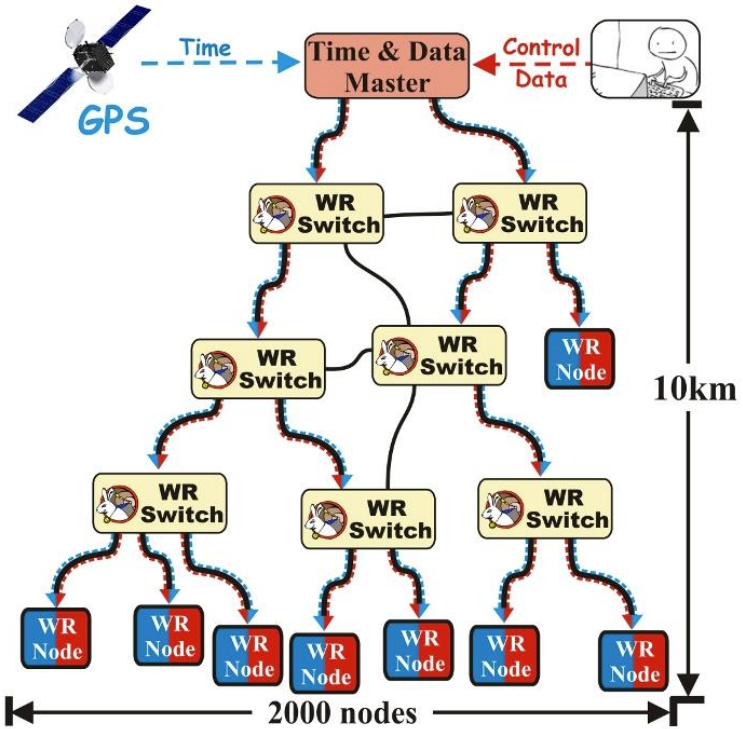
- The main purposes of the Time Synchronization System (TSS) are:
  - distribution of the global clock signal throughout the installation
  - generation and distribution of synchronous commands throughout the installation
- The central part of the TSS is the so-called TSS controller. The TSS controller generates synchronous commands, which are then distributed throughout the installation.
- The TSS controller will implement the following commands:
  - Start of Sequence — upon receiving this command, the TSS controller must start the generation of a sequence of frame batches using parameter values loaded into its registers.
  - Stop of Sequence — upon receiving this command, the TSS controller must complete the generation of a sequence of frame batches.

White Rabbit-based approach



- Guaranteed accuracy is much better than 1 ns
- WR PTP – standard protocol developed and widely used by CERN
- Same interfaces for all connections
- More elegant but expensive and sophisticated solution
- TSS-node requires support WR PTP and send/receive sync commands

White Rabbit



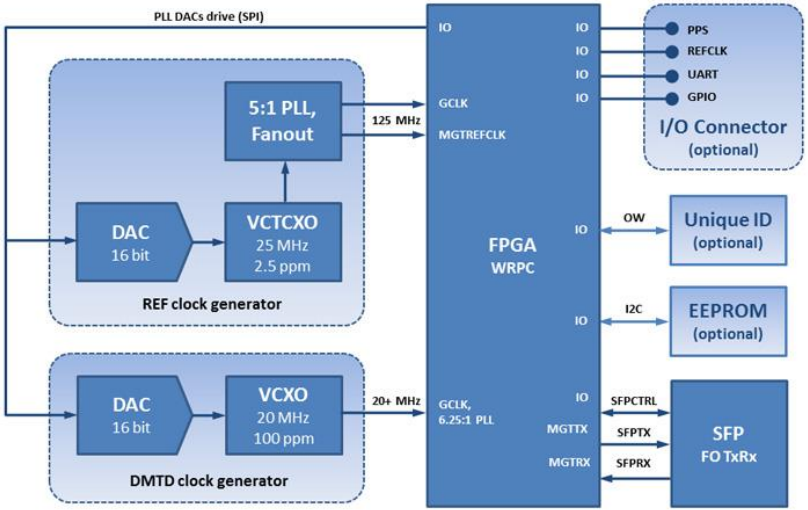
- Guaranteed accuracy better than 1 ns
- WR timing distribution is based on three elements:
  - Precision Time Protocol (PTP)
  - Synchronous Ethernet (SyncE)
  - Digital Dual Mixer Time Difference (DDMTD)

White Rabbit-node: elements of implementation

From a hardware/gateware designer point of view, integrated solution

WR-node is the last device that receives a time reference in a WR-network. FGPA-based device includes:

- SFP module for 1000BASE-X Ethernet
- tunable external oscillator VCXO
- WR PTP core (WRPC)
  - open-source soft IP-core (vhdl) and firmware
  - current release 5.0, with RISC-V (23-12-2023)
  - implements DMTD and WR PTP
  - interface for sending and receiving Ethernet frames (pipelined Wishbone)
  - Timecode interface and Tx Timestamping interface
- platform support package (PSP) (Altera/Xilinx)
- board support package (BSP)



White Rabbit Node Reference Design, ohwr.com

Sync Technology WR-devices

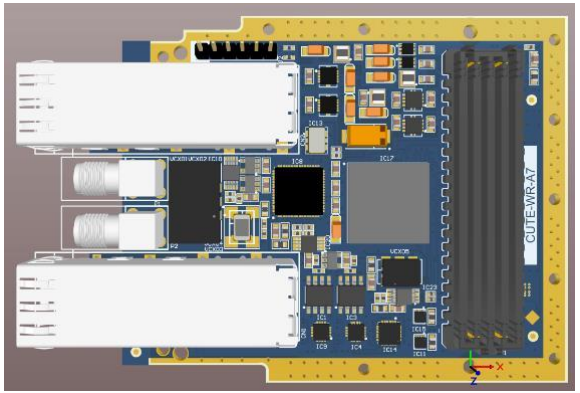
Sync (Beijing) Technology –
company from Tsinghua University, China.

White Rabbit switch **WRS-18A**

- 18-port WR switch
- Runs Linux OS
- Open-source

White Rabbit node **Cute-WR-A7**

- 2-port WR endpoint
- Mezzanine card with FMC connector
- Sync clock output
- GMII interface (not fully implemented)



Cute-WR-A7 board

Cute-WR-A7 front panel

White Rabbit switch WRS-18A

White Rabbit network topologies testing

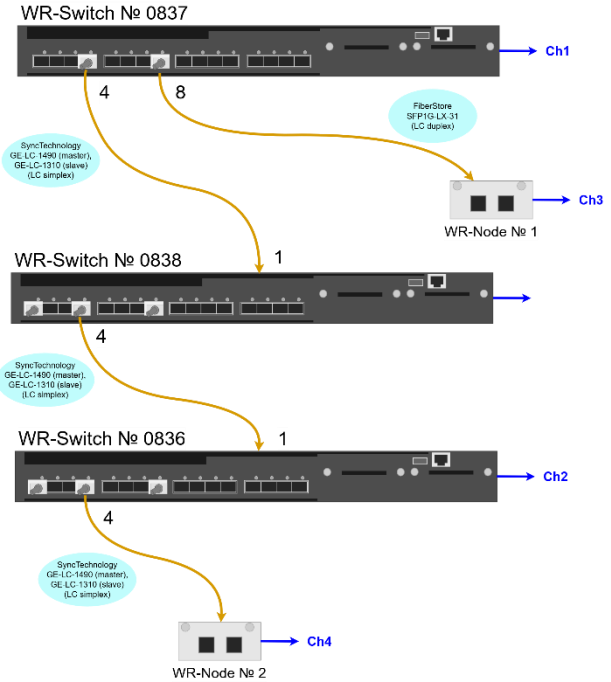
Available equipment:
- 3 WR switches
- 2 WR nodes

Reference clock: 10 MHz clock from WR switch internal oscillator
Tested topologies partially represent SPD network structure in NICA

Tested network topologies:

1. Connection between WR switch and L1-concentrators
2. Connection between grandmaster WR switch, TSS controller and L1-concentrators
3. Connecting all L1-concentrators together
4. Connection between grandmaster WR switch, NICA bunch crossing and L1-concentrators

Topology 4



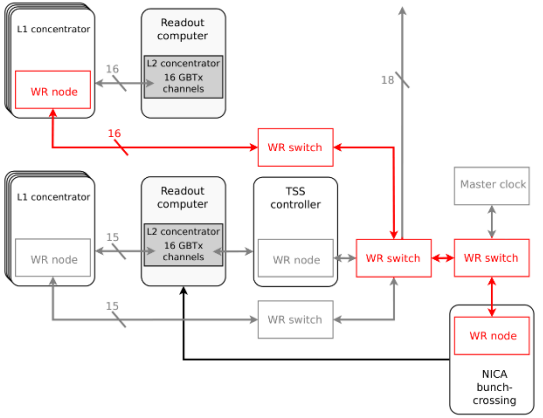
Ch1-Ch4:
PPS signal outputs for accuracy and jitter measurement.

Synchronization accuracy evaluation

- Calibration procedure is done for “Sync (Beijing) Technology” WR-Switches and WR-Nodes.
- Accuracy requirement (from TDR): < 1ns
- Precision requirement (from TDR): < 50 ps

- Measurements were taken with R&S RTO2044 oscilloscope at a room temperature with 20 Gsamples/s and ***estimated delta-time accuracy*** of *21 ps (peak)*
- The result of calibration is decreased time difference between two synchronized clocks.

- ***Jitter*** is calculated as RMS of time difference between successively acquired waveforms of a repetitive signal for a given reference level instant (50 %)***.***



TSS-protocol: functional requirements

Functions and features for a DAQ system

Principles of triggerless DAQ:

- event rate 3×10^6 1/s
- data exceeding the thresholds are annotated with timestamps
- timestamps are grouped into frames of slices
- slice length is 10÷100 μs
- frame length is 0.1÷10 s
- up to 200 end nodes (L1 “concentrator” hubs)

TSS-protocol - a user-level protocol based on a stack of standard network protocols.

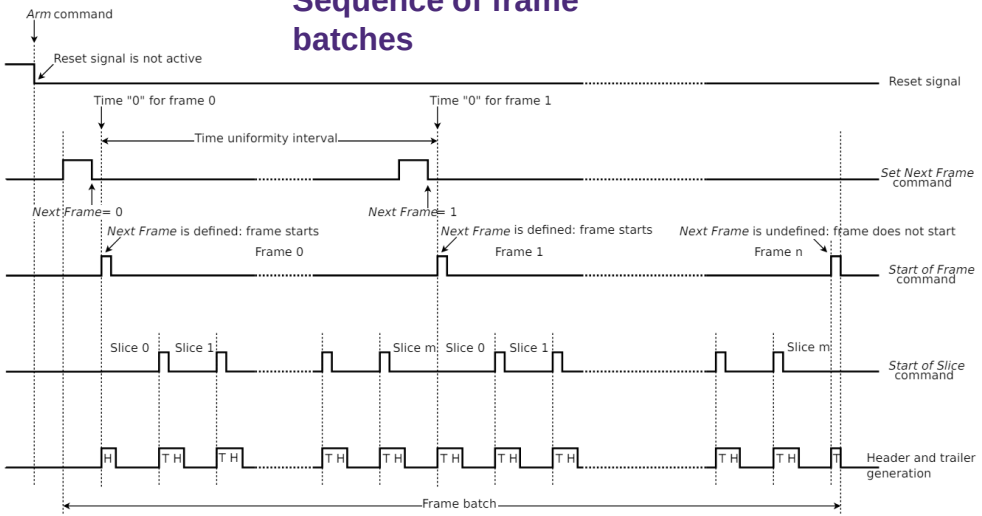
Main protocol function:

- provide a schedule when to begin and end frames and slices.

Service protocol functions:

- Network latency calculation
- TSS network discovery and diagnostic

Sequence of frame batches



Main protocol payload - Atomic broadcast “synchronous” commands:

- SNF – Set Next Frame
- SOF – Start of Frame
- SOS – Start of Slice

Examples of protocols over WR

Distributed timestamping, and event exchanging mechanisms

White Rabbit Trigger Distribution (WRTD, 2019):

- Nodes are sending and receiving Events
- Event has ID, Timestamp and sequence counter
- Timestamps are expressed using a 48-bit counter for seconds, a 32-bit counter for nanoseconds and a 16-bit counter for fractional nanoseconds
- Events are distributed as UPD messages
- Nodes can have rules for input and output Events, can add fixed delay to Timestamps

Early Timing System Prototype (2013)

- makes use of the Etherbone (Ethernet to Wishbone communication)
- data master sends «bus transactions» to control data slave
- data master does not have to be White Rabbit enabled

TiCkS: A White-Rabbit Based Time-Stamping Board (2017)

- ns-precision time-stamping
- UDP stack

General approach:

- Deterministic Controller (master) and distributed controlled devices (slaves)
- UDP packets over 1000BASE-X in WR network
- Slaves are programmed to execute certain actions
- Negligible risk of packet loss in a dedicated network

Common concern:

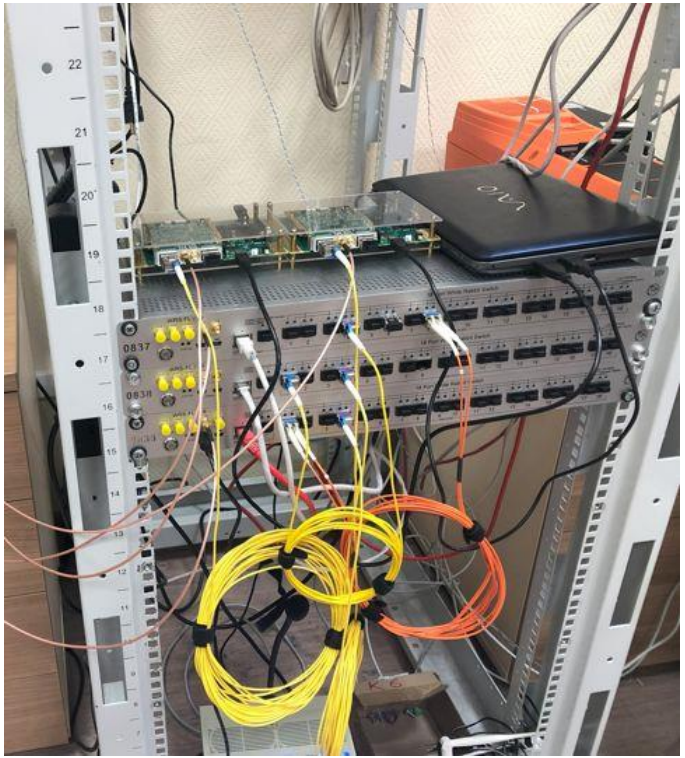
- Upper-bound latency of the network

Data transfer through WR-network

White Rabbit network can be used like a regular gigabit Ethernet

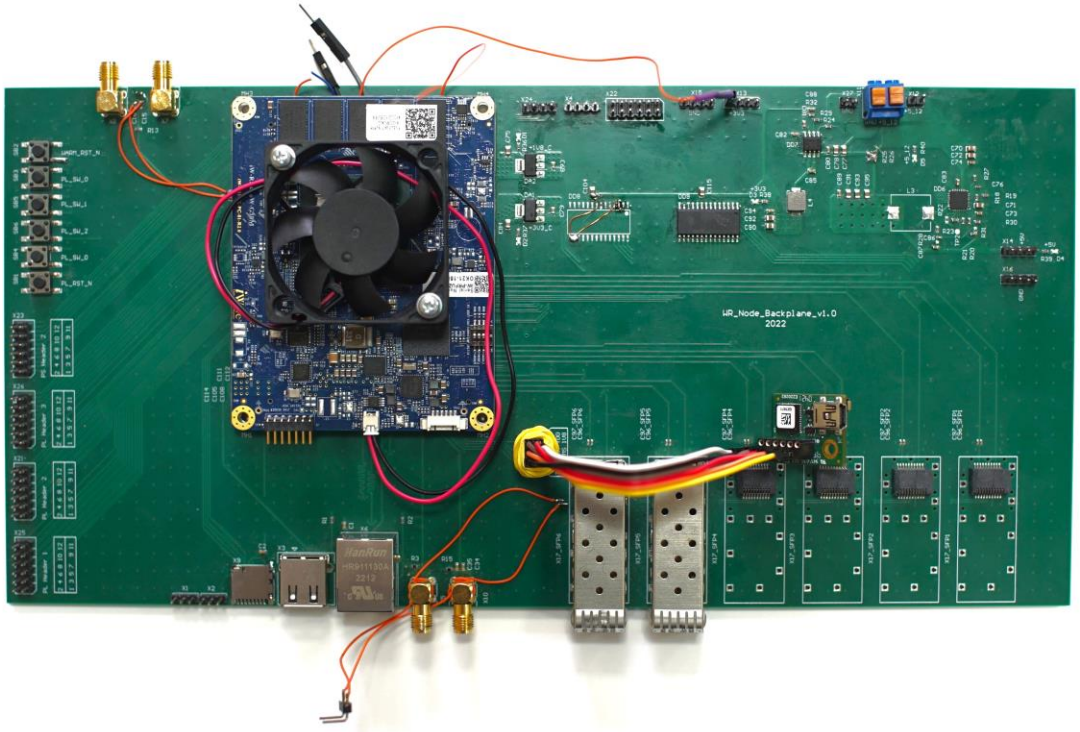
Research objectives:

- Build TSS network prototype
- Create FPGA-based TSS-controller IP
  TSS controller sends triggers to all other devices in WR network
- Create FPGA-based TSS-node IP
  TSS node receives, filters and processes incoming triggers

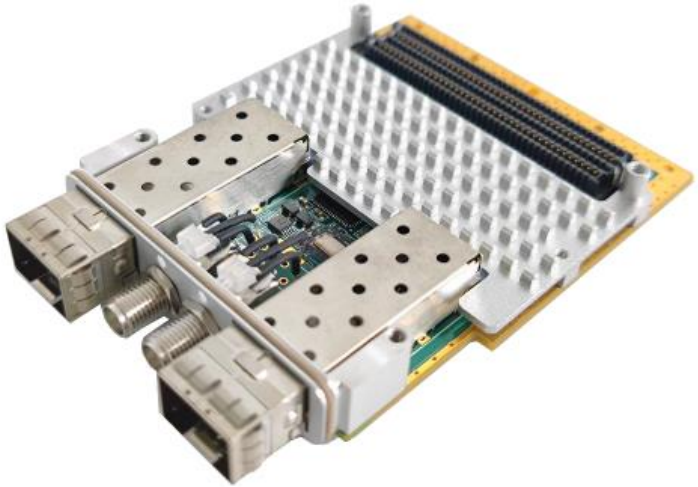


White-Rabbit evaluation board

- Custom board based on CERN White Rabbit reference design
- Multi-port baseboard with WR switch functionality – could be a multipurpose device

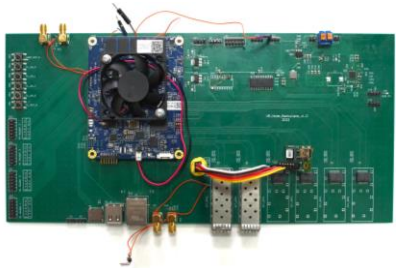


CUTE-WR-A7



- Sub-ns Accuracy and pico-second precision
- 20Km distance (up to 160Km by special SFP module)
- Dual WR port, supporting Cascade topology
- 10/125 MHz, PPS, UTC/TAI output
- SNMP, Remote update via UDP
- GMII like interface for data transmission
- Embedded ethernet protocol process engine written in HDL, 900Mbps for UDP, 255Mbps for TCP

Hardware platforms to test protocol



Self-developed platform

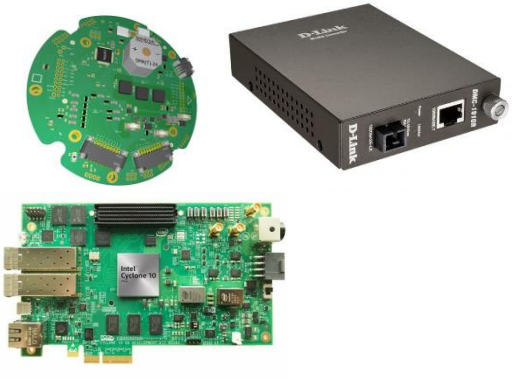
- Zynq UltraScale+ FPGA
- Connection via SFP
- Can act as WR-node

DK-DEV-10CX220-A

- Cyclone10 GX FPGA
- Connection through SFP with Triple-Speed Ethernet IP Core

iW-RainboW-G30D
ZCU-106 Dev Board

- Zynq UltraScale+ FPGA
- Connection via FMC RGMII
- Connection via SFP



Platforms with 1000-Base-T + D-Link Media Converter

Defectoscope:
- Gowin GW2A FPGA
- RGMII

DK-DEV-10CX220-A :
- SGMII

Increased data transfer delay

TSS development roadmap

- Development of TSS protocol specification elements
- Release of 2nd revision of WR evaluation board
- Project porting for Cyclone 10

- TSS controller prototype implementation
- Preliminary integration and testing with DAQ L1 elements

- WR network deployment and configuration for TSS network segments

- Continuous support and refinement of TSS