MPD DAQ & Trigger status

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Joint Institute for Nuclear Research

XIII Collaboration Meeting of the MPD Experiment
at the NICA Facility

MPD DAQ Design Goals

Properties

Reliable data transfer. Pipeline operation with sync and async stages.
Extensive diagnostics in hardware and software. Monitoring, logging.
Data integrity check on all levels. CRC, sequence numbers, FEC.
Fault tolerant, Highly available. Fast self recovery after SEU events.
Distributed, scalable, extendable. Based on open and industry standards.
Flexible architecture. Partitioning for independent subsystem operation.

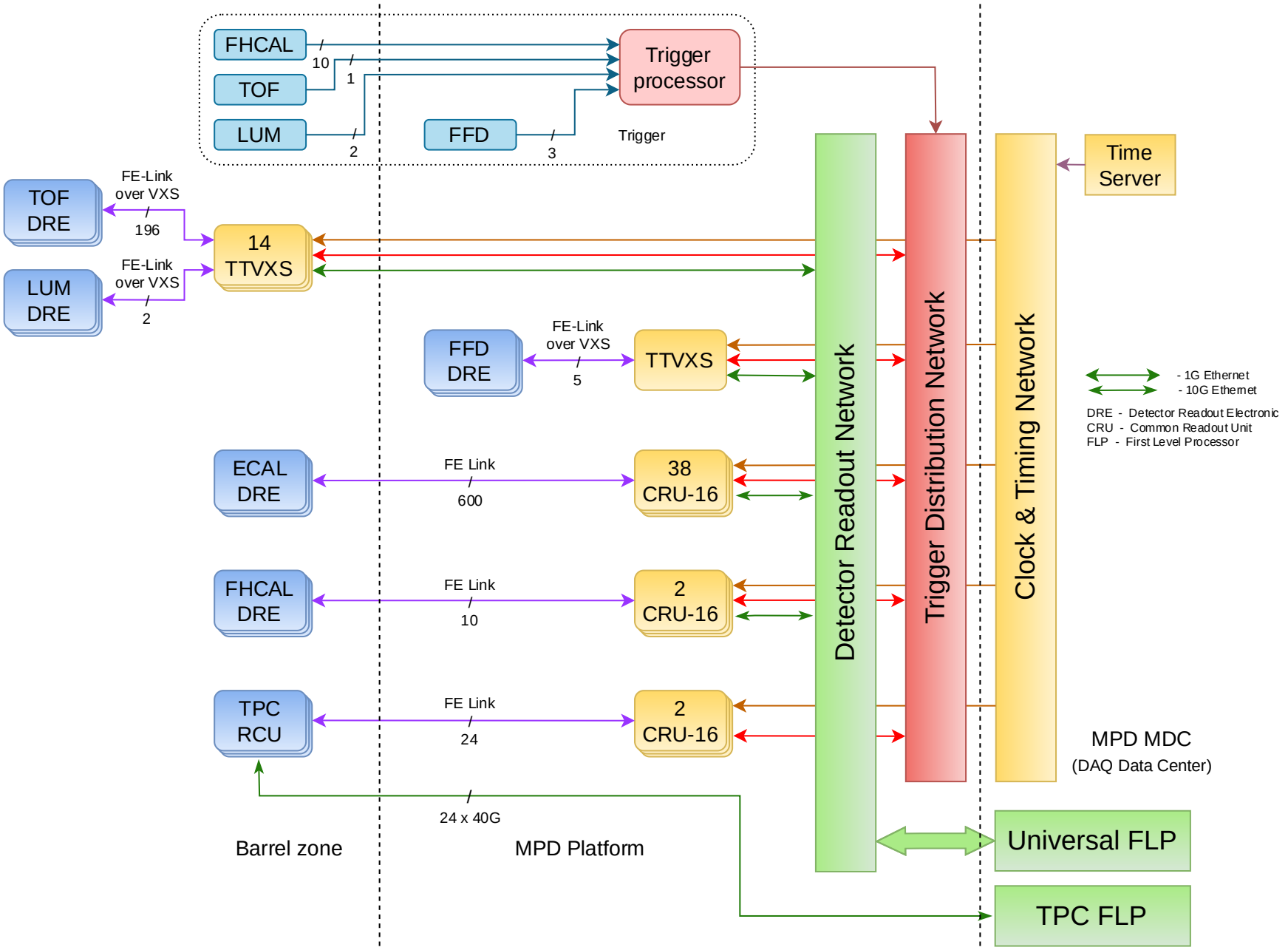
Operation Modes

Multiple hardware trigger classes
Uncompressed, full raw data during MPD commissioning
Large calibration data events at low trigger rate
High multiplicity events from central collisions at planned trigger rate

DAQ in numbers

Up to 7 kHz trigger rate, over 1 MB event size to storage device
From 5 to 30 GB/s uncompressed raw data rate from readout cards to FLP
Up to 200 PB per year of raw data

MPD DAQ Architecture

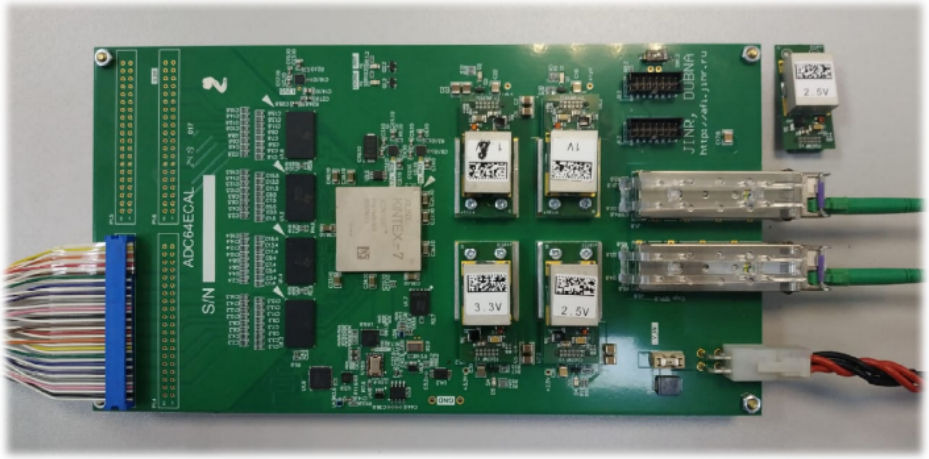


Detector Readout Electronics

TDC Boards

TDC72VHL

ADC Boards



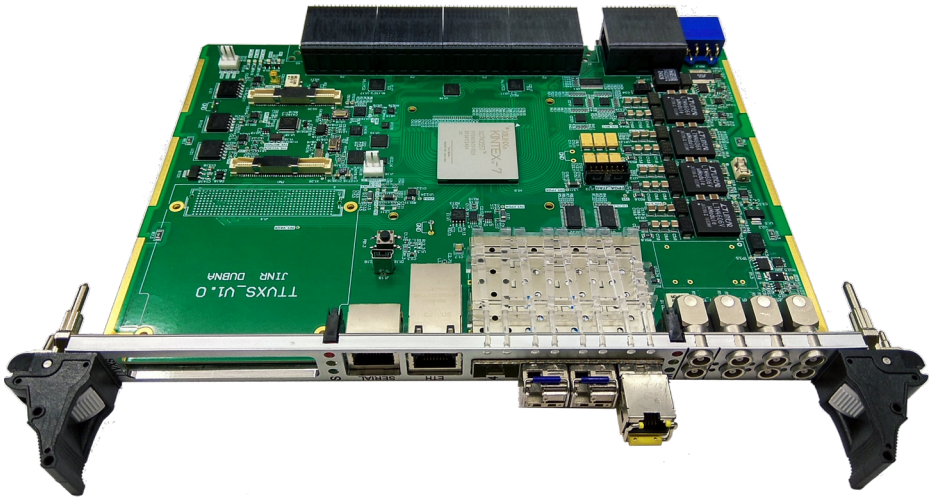
ADC64ECAL

	TDC72VHL	*TDC64VLE*
Number of Channels	72	64
Input Signal	LVDS	
Input Impedance	100 Ohm	
Input Diff. Voltage	25 mV min	
Input Connector	CXP	Molex P50
Time Resolution.	~25 ps (with INL)	100 ps
Data Transfer	1Gb/s Ethernet	
Synchronization	FE-Link over VXS	

	ADC64ECAL	*ADC64s2*-v6
Number of channels	64	64
Sample rate	62.5 MS/s	62.5 MS/s
Resolution	14 bit	14 bit
Power consumption	< 15 W	< 20 W
Magnetic field tolerance	by design	by design
Radiation hard DC/DC	no	no

Time, Trigger and Clock distribution modules

TTVXS



- Clock, timestamp and trigger distribution to VXS payload boards: backplane FE-Link interface
- 4 SFP+ sockets for Detector Readout, Trigger Distribution and Clock & Timing connections
- Reference frequency and timestamp provided by White Rabbit Network or FE-Link (with CRU-16)
- Additional clock and trigger interface by FMC (VITA-57) card slot – integration with other systems

CRU16

- FE-Link interface to DRE boards - multi-gigabit duplex serial synchronous interconnect with deterministic latency. Provides clock and trigger information for downstream boards and receives raw data stream
- SO-DIMM DDR3 memory for data buffers. Decouples realtime hardware data flow from high latency software data receivers
- 4 QSFP downlink sockets for 16 Detector Readout boards connections grouped by 4
- 1 QSFP uplink socket for 40 Gb Ethernet data transfer
- 3 SFP sockets for Trigger Distribution, Clock & Timing
- Timing synchronization by White Rabbit network

DAQ Electronic Modules Production

Product	Required boards							Manufactured and Tested Q1 2024	Progress
	ECAL	FHCAL	FFD	TOF	TPC	LUM	Trigger Distrib.		
TDC72VHL	—	—	10	196	—	—	—	219	106 %
TDC64VLE	—	—	—	—	—	2	—	2	100 %
TTVXS	—	—	1	14	—	—	4	20	100 %
ADC64-ECAL	600	—	—	—	—	—	—	630	105 %
ADC64S2 v6	—	10	—	—	—	—	—	0	0 %
CRU16	38	2	—	1	2	—	1	45	102 %

TDC72VHL, TTVXS status

- Hardware ready 100%
- Firmware with basic functions tested on TOF stand
- Software ready
- "FE-Link over VXS" firmware under testing on TOF stand

CRU-16 status

- Hardware manufactured
- All on-board components tested
- Some firmware parts ready
- FE-Link under testing on ECAL stand
- Control software under development

ADC64 family status

- Hardware manufactured
- Tested on stands and BMN
- Refactoring monolithic to modular design (firmware and software) in progress.

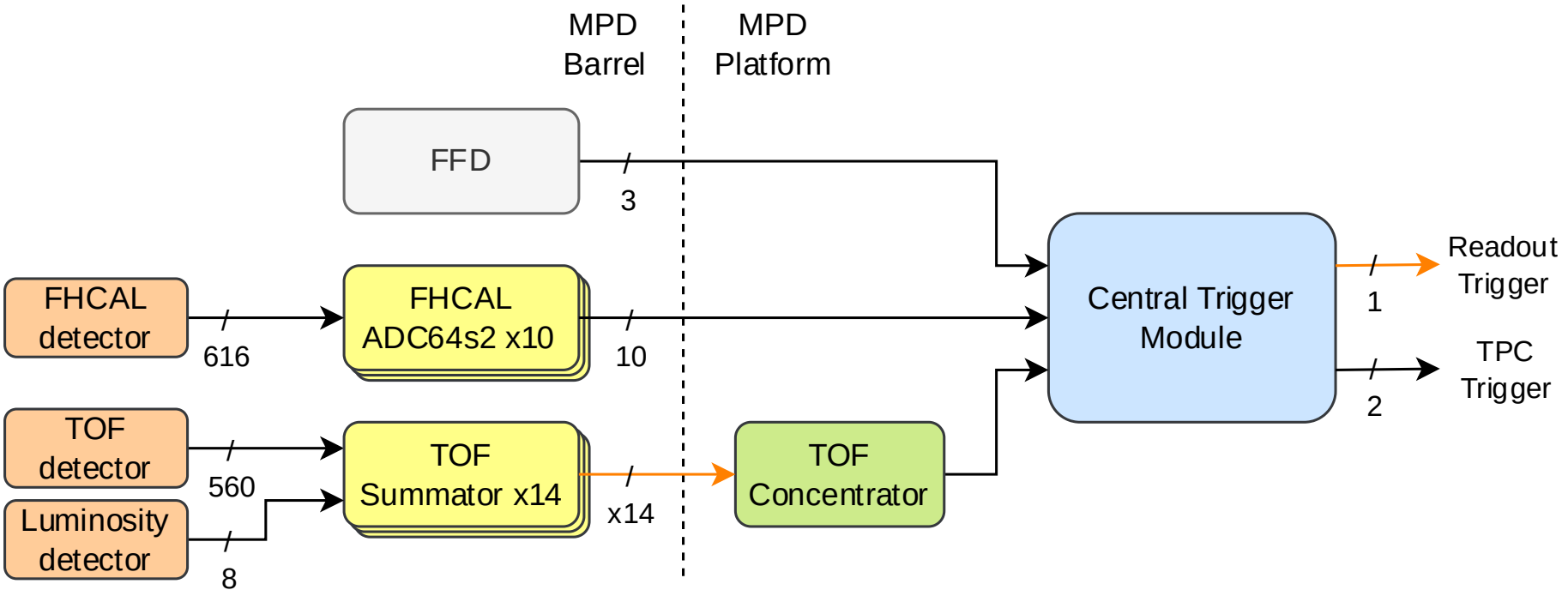
MPD DAQ Data Center

MPD Trigger

Main goal — minimize time from beam interaction event to detectors readout trigger signal.

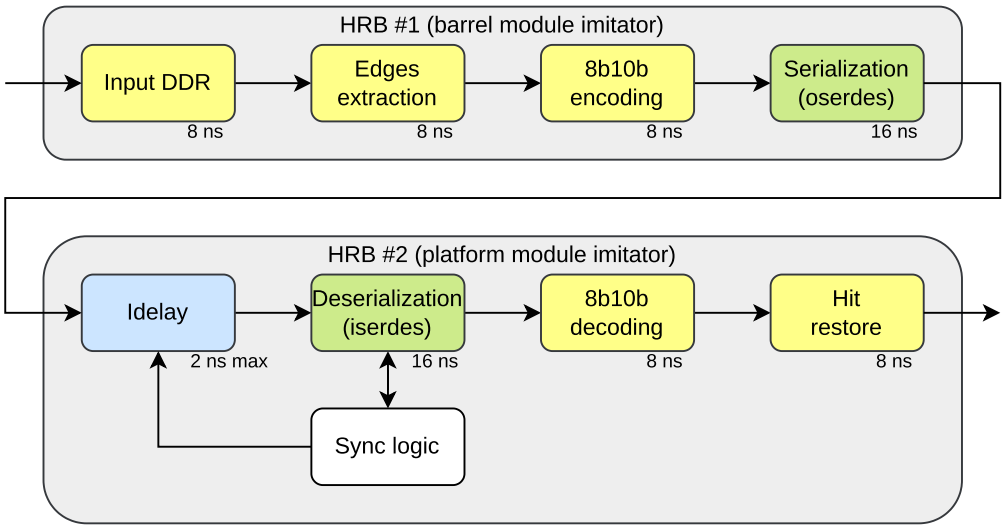
There are 4 trigger detectors in MPD — FFD, FHCAL, TOF, Luminosity:

- FFD group designed their own trigger electronics
- FHCAL — trigger processing on ADC62s2 modules: digital threshold for every channel, then some logic in central trigger module
- TOF — sum of all detector channels, new modules for trigger processing
- Luminosity — same modules as TOF, but different logic



TOF trigger

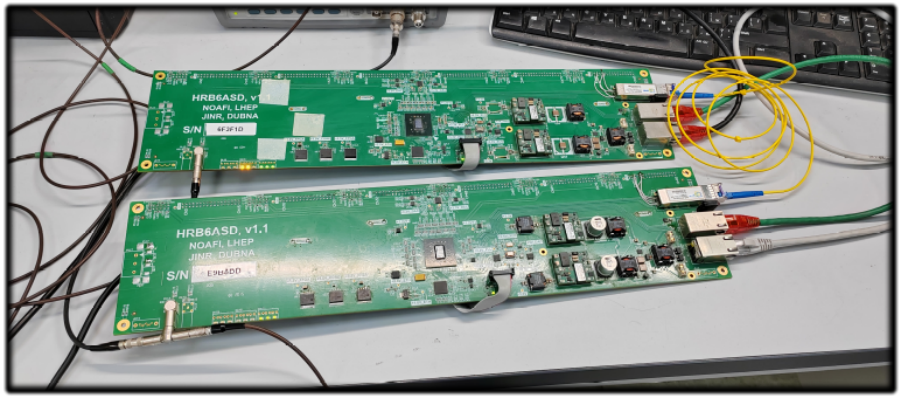
Logic diagram for test



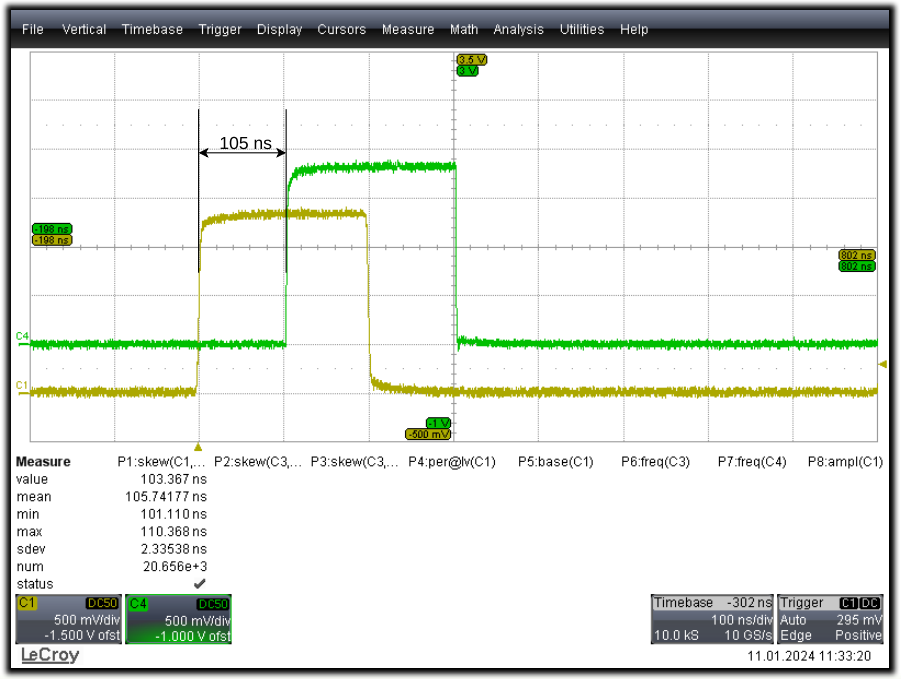
20 trigger signals are output from each TOF module

- 2 TOF modules are connected to each summator
- summators make logical "And" for pairs of input channels, then the sum is calculated.
- data from the summator to the hub is transmitted over fiber at a speed of 1 GB/s
- concentrator module on platform calculates final sum across the entire TOF detector and outputs the trigger signal for the central trigger module

Test setup

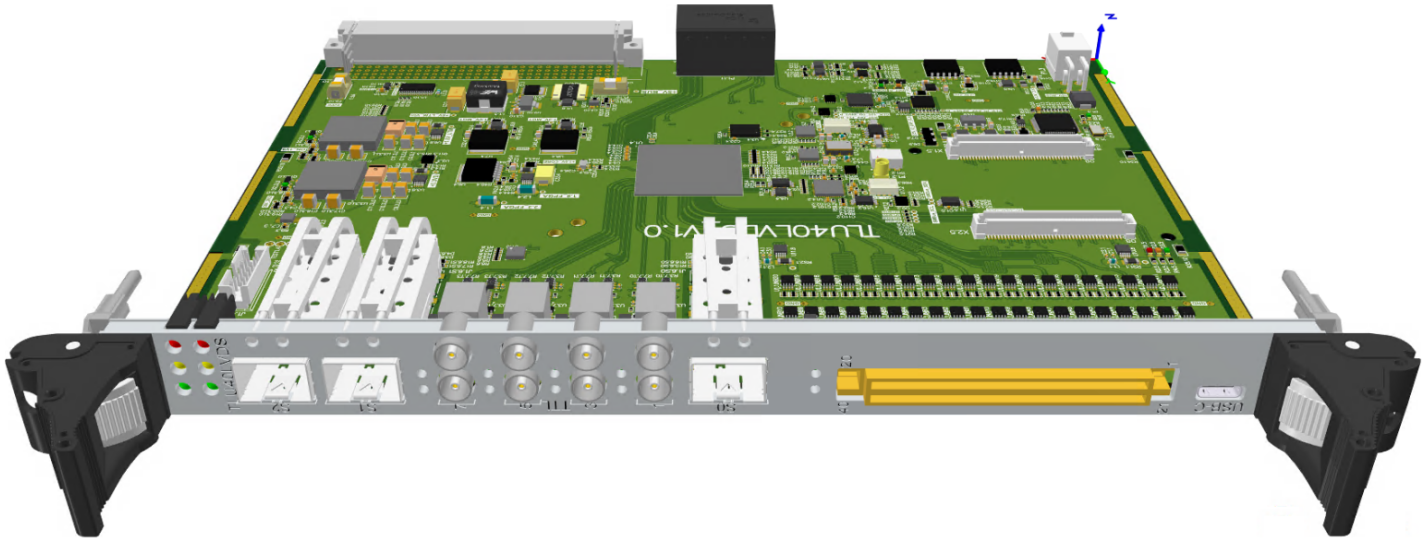


Test result — 105 ns delay from input to output



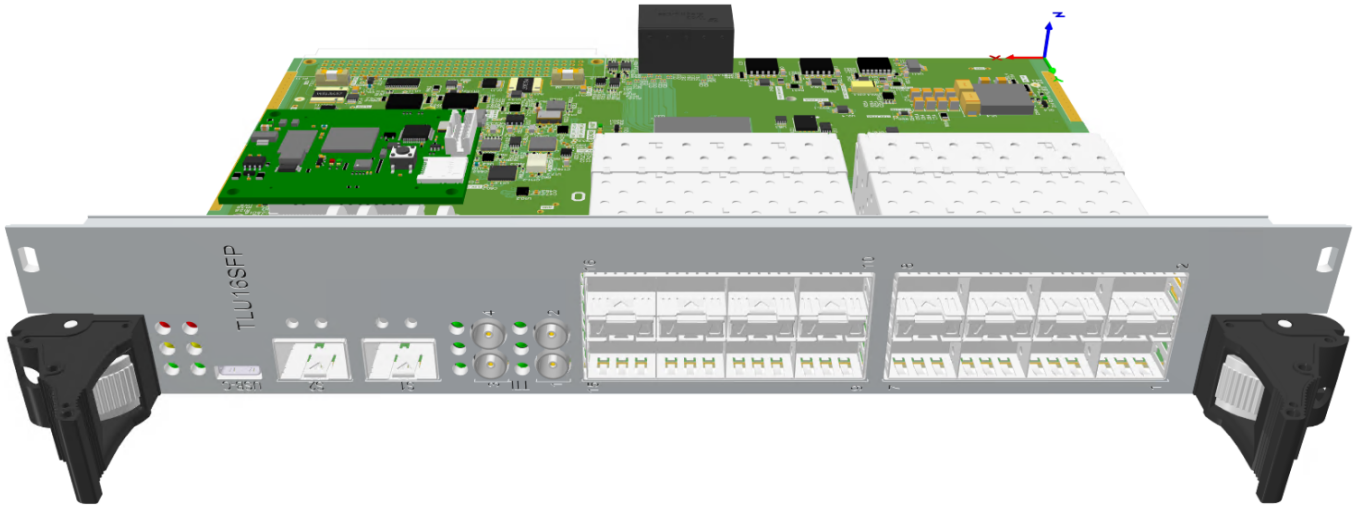
TOF trigger modules

TLU40LVDS — TOF summator



TLU40LVDS — calculate sum for two TOF detector modules and transmit it via central SFP connector.
This modules has additional 8 LEMO coaxial connectors.
Two TLU40LVDS will utilize 4 LEMO for reading trigger signals from Luminosity detector.

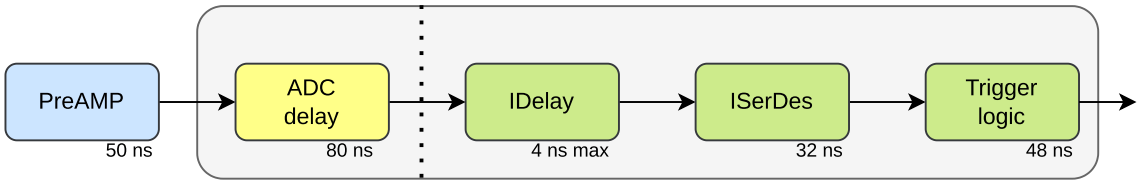
TLU16SFP — TOF concentrator



TLU16SFP — read digital sums from up to 16 TLU40LVDS modules (for MPD we need 14 TLU40LVDS). Then final sum is calculating. And after comparing with adjustable threshold transmitting complete TOF trigger signals via LEMO.

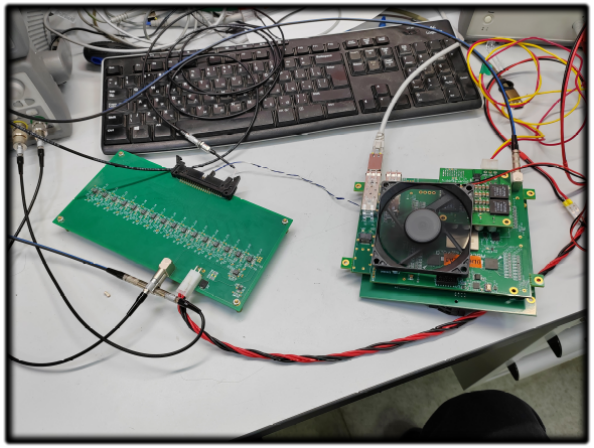
FHCAL trigger

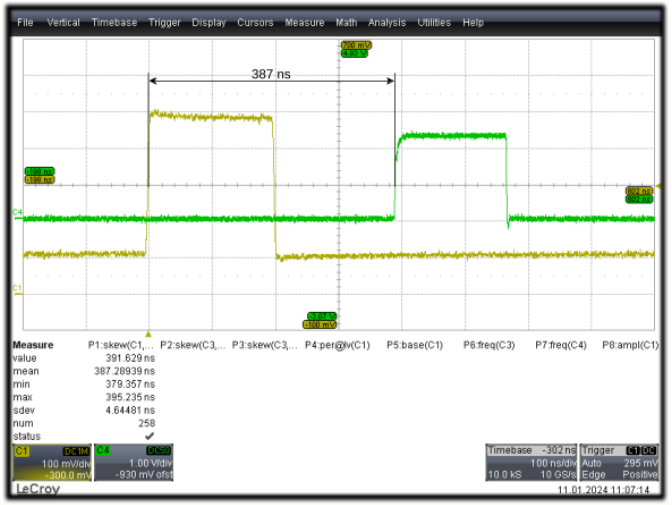
Logic diagram for test (delays are for ADC64ECAL)



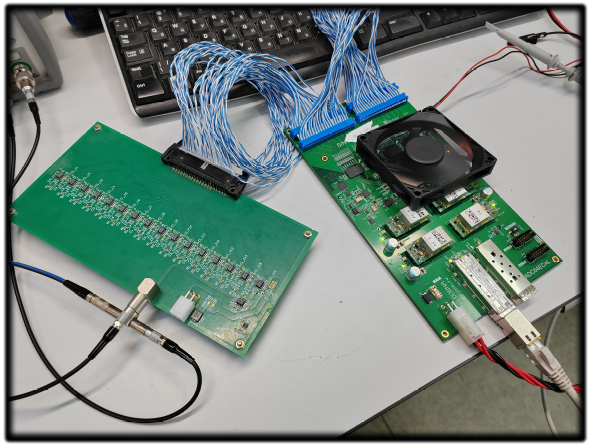
To mesure possible trigger delay for FHCAL detector two existing ADC64 module types were used: **ADC64s2 v5** and **ADC64ECAL**. Both module types used in MPD. Main difference between this boards, exept geometry, is different ADC chips.
Test shows that delay for **ADC64ECAL** module is **150 ns less** than delay for **ADC64s2**.

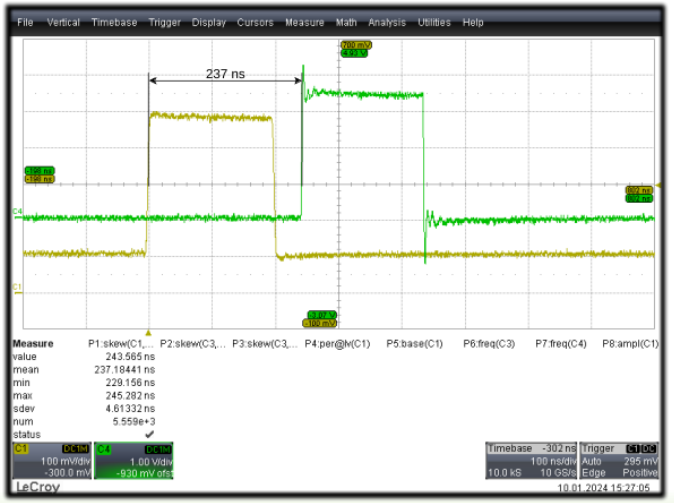
ADC64s2 v5 — 390 ns trigger delay





ADC64ECAL — 240 ns trigger delay



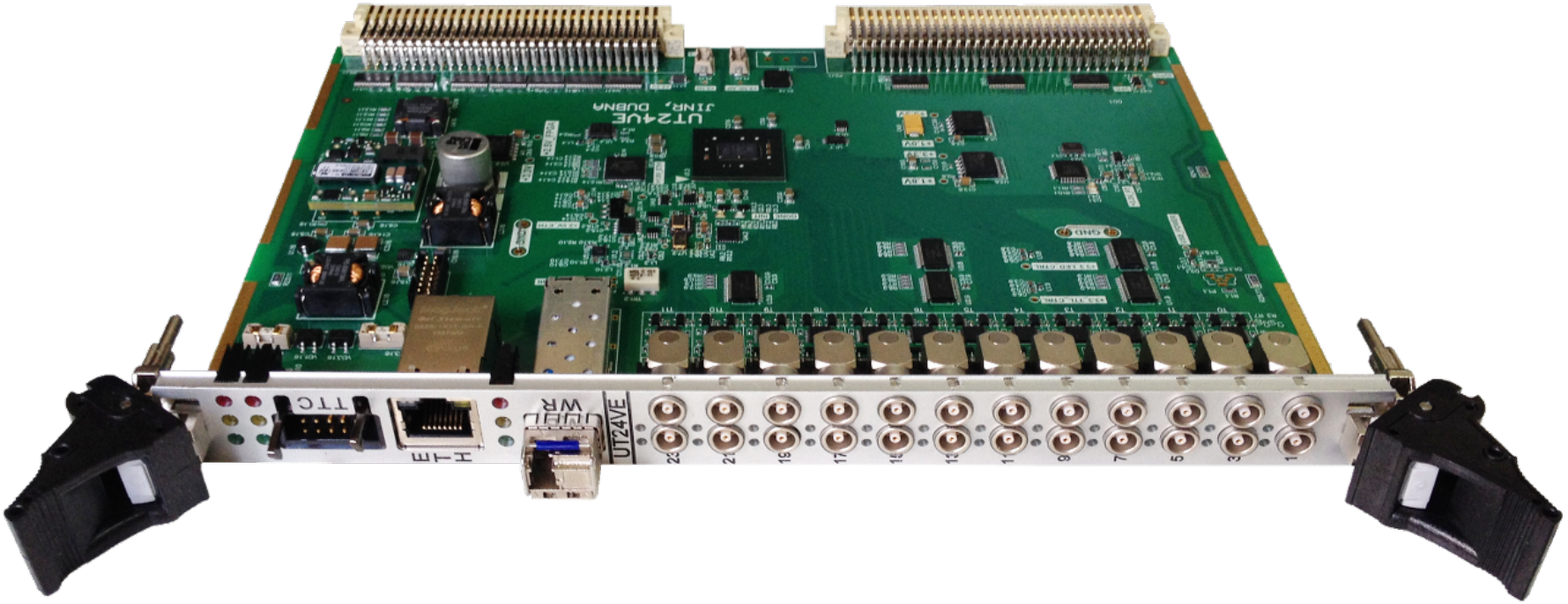


Central Trigger Module

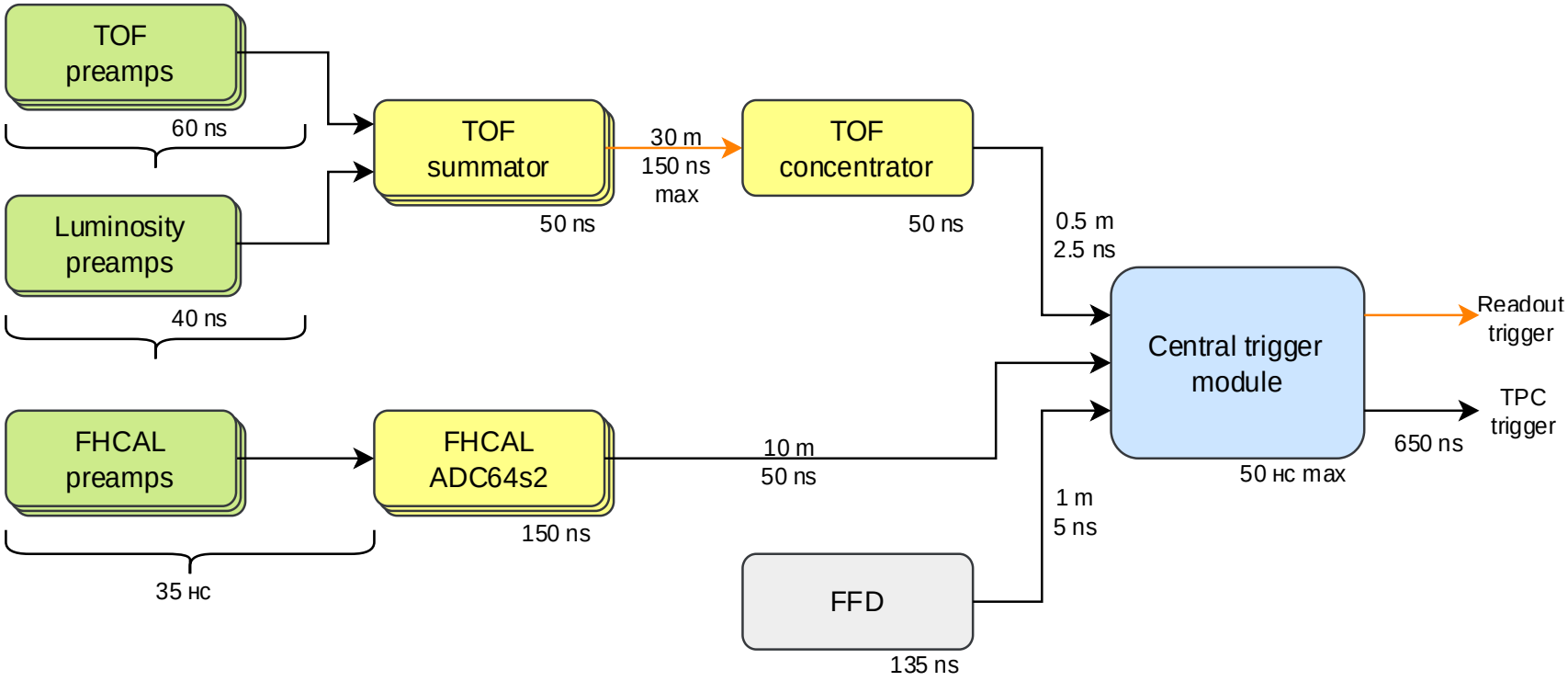
For central trigger module UT24VE module will be used. UT24VE module already designed and produced. It has 24 programmanle LEMO I/O (LVTTL). For MPD we need 18 trigger connections:

- 3 connections for FFD trigger input
- 10 connections for FHCAL trigger input
- 1 connection for TOF trigger input
- 2 connections for Luminosity trigger input
- 2 connections for TPC trigger output

Readout trigger will be transmit via FE-Link network.



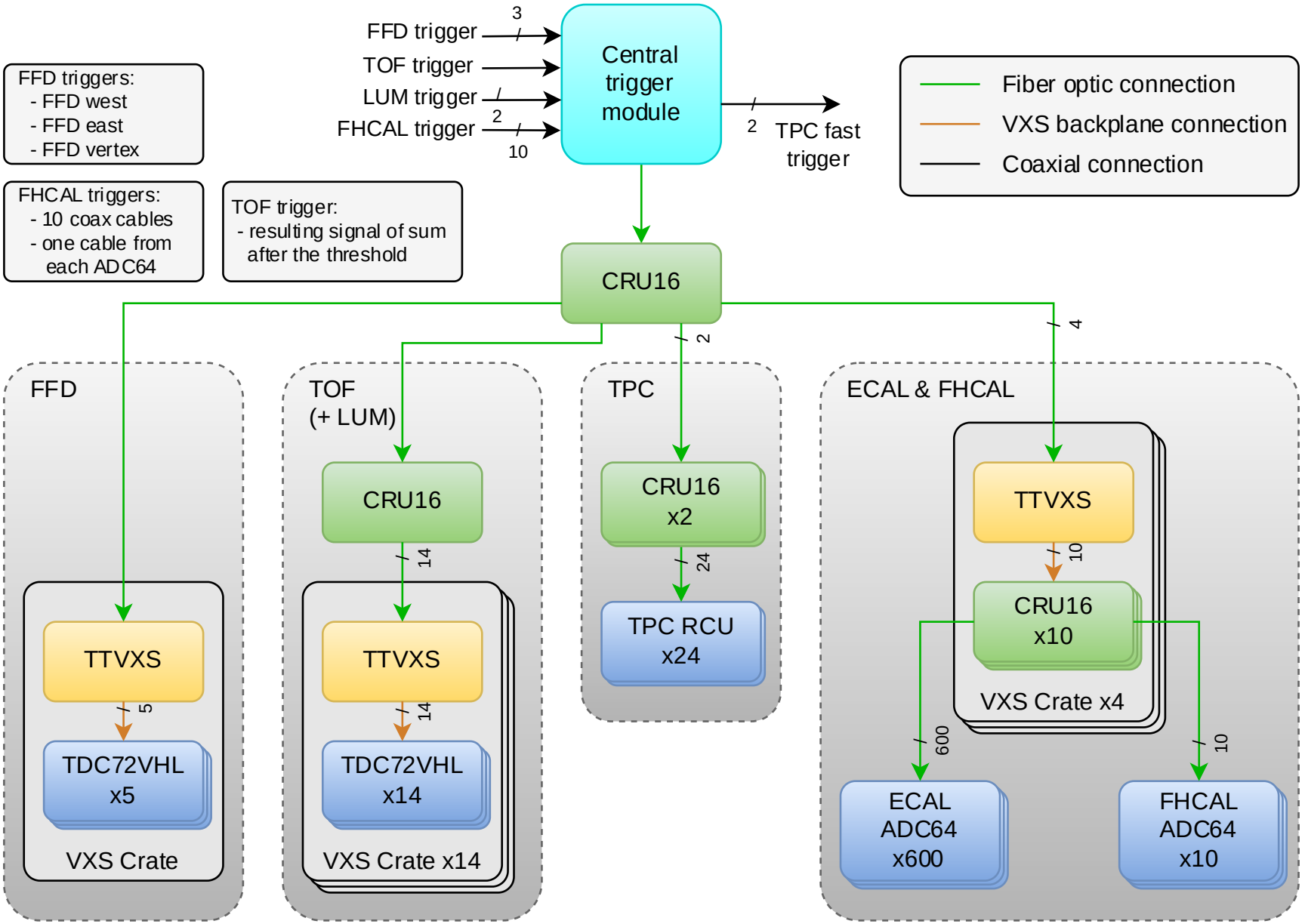
Trigger latency



Trigger subsystems		Central trigger	TPC	Full delay
TOF	300 ns	50 ns	650 ns	~1000 ns
Luminosity	300 ns			
FHCAL	250 ns			
FFD	140 ns			

Calculated full trigger delay is about 1000 ns.

Trigger distribution



Trigger Electronic Modules Production

Product	Required boards				Status Q1 2024
	FFD	TOF	LUM	FHCAL	
TLU40LVDS	—	14		—	PCB production
TLU16SFP	—	1	—	—	PCB production
ADC64s2 V6	—	—	—	10	PCB mounting
UT24VE	1				Module produced

All modules designed. UT24VE already produced.
Other — in different stages of production.

FPGA gateware — in progress.

Thank you!