Status of TPC LV, TPC GATE systems and FE cards tests

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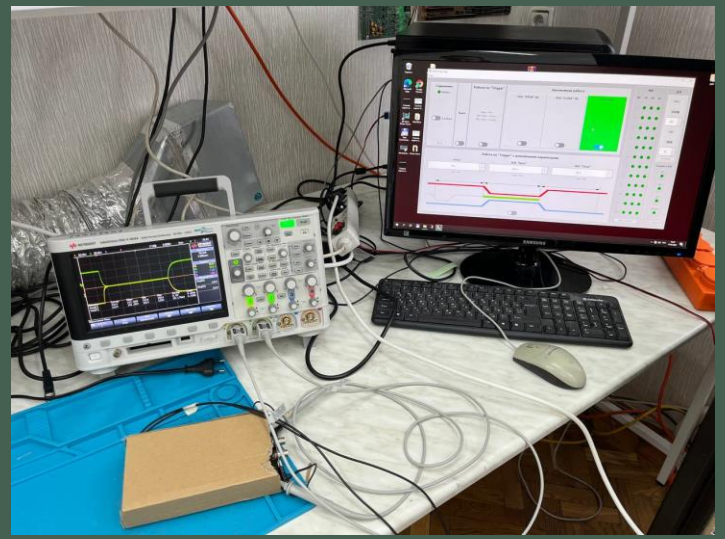
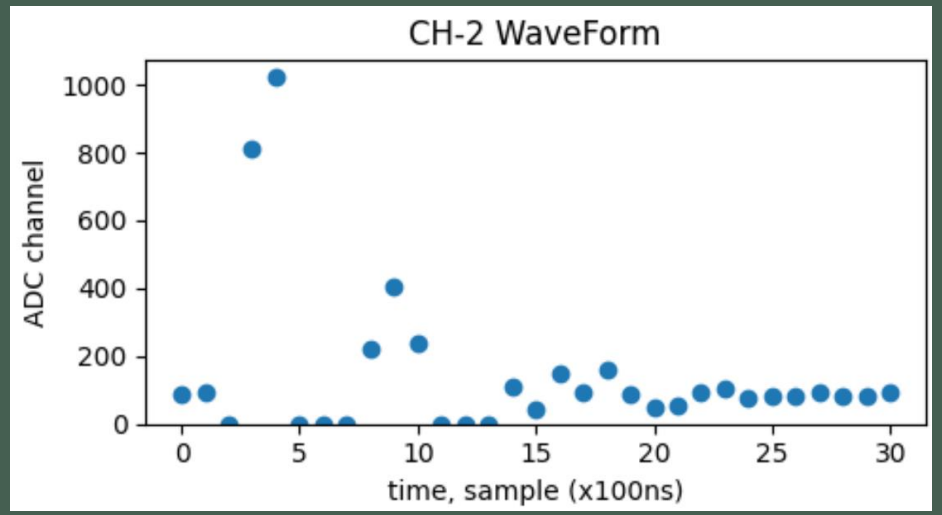
TPC GATE systems

Front and back side of Gate with connected devices for testing PSU and 12 Gate modules simultaneously

Front and back side of 1 Gate crate, in top-12 Gate modules, in bottom PSU



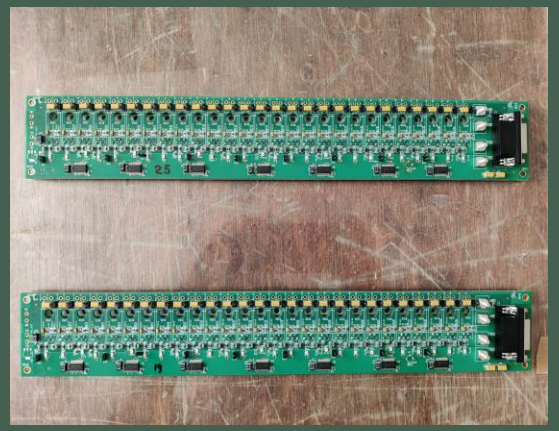
Test bench for 1 module of 1 gate crate



Example of open/close transiti on process, is about 2 us

TPC LV

Power cable for FEC



2 LVN9 with old r-angle DSUB

DSUB 26 pin with steel case

Molex Nano-Fit 12 and 16-pin

https://www.molex.com/en-us/products/part-detail/2014441112

Test bench for LVN9, RL ~ 4 FEC

New output capacitors:

- Ceramic CL31A107MPKNNWE ESR ~0.01 Ом (MIN на 5-10 MHz)
- Polimer T520C107M006AME025 ESR 0.025 Ом ESR @100 kHz/ +20 °C

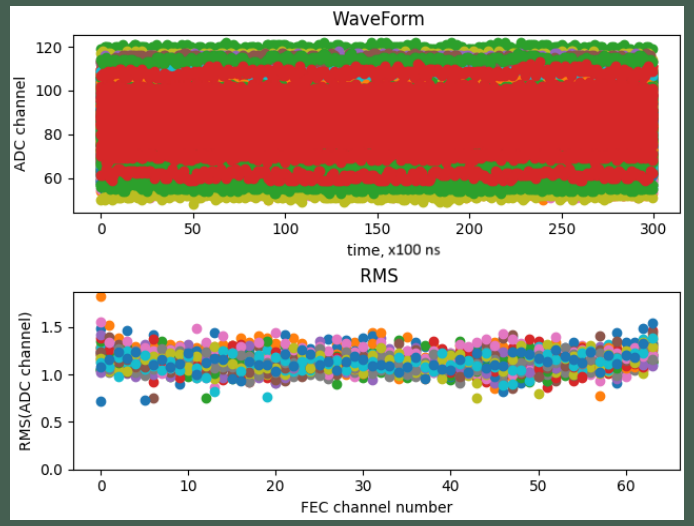
Soldered off:

- Tantalum TAJC476K020RNJ ESR 0.500 Ом ESR @ 100 kHz/ +20 °C

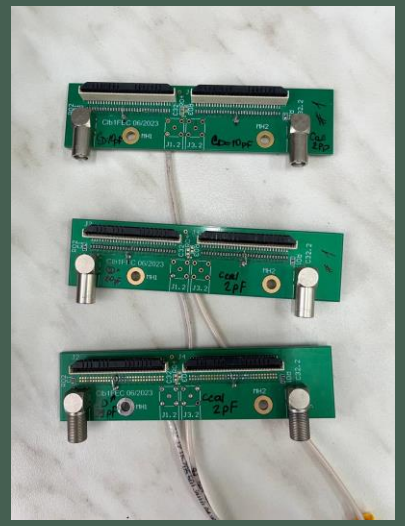
FEC testing

Test bench ROC

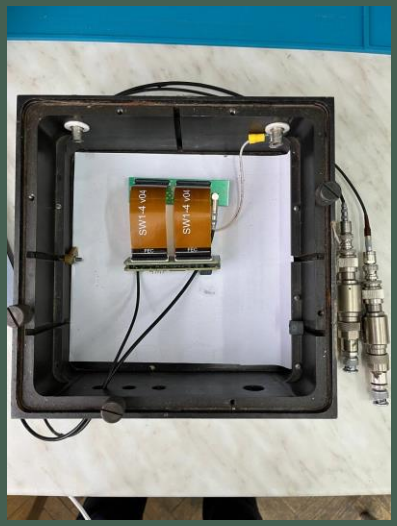
LVN9 output voltages increased to 1.8, 3.1, 3.8 V



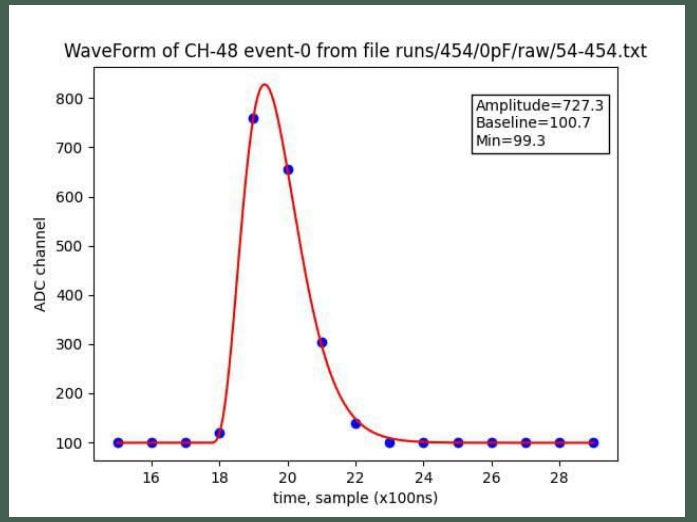
Example of 10 events data for 31 card from ROC



PCB with Ccal=2pF



Cast iron case with FEC connected by flexible PCB to PCB with Ccal



Example of SAMPA curve fitting

FEC test parameters: AFG3152C pulse 400mV at.-20dB ~ 80fC, Tran=3ns

SAMPA Based Streaming Readout Data Acquisition Prototype *y=Baseline when y<Threshold

Thank you for attention