FLNP JINR – CSNS
Workshop on the neutron scattering technology and multi-disciplinary research
International Conference Centre, Dubna

Working with the CAEN *DT5560SE* digitizer

a project for processing signals from a helium-3 filled position-sensitive detector.

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Digitizer in the data acquisition system

Digitizer – is an electronic device that continuously acquires analog pulses, passing through an analog input stage of signal conditioning, an **analog-to-digital conversion** by fast ADCs, and **storage** of the digitized samples as event data into digital memories, where they can be **read out** by a host computer through fast communication interfaces (USB, VMEbus, Optical Link, Ethernet).

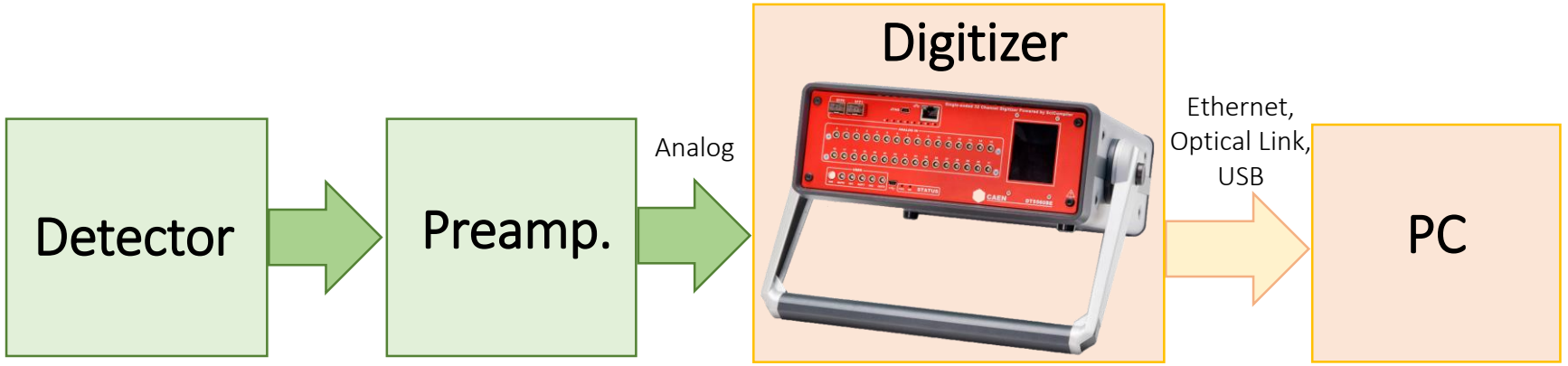


Figure 1. Structure of a digitizer-based data acquisition system

Digitizer DT5560SE:

- 32 channel, **14-bit @125 MS/s** Digitizer,
- **Programmable analog frontend**,
- Xilinx Zynq-7000 SoC with **open FPGA**,
- Supported software tool by **SCI-Compiler**,
- Board-to-board **synchronization,** etc.

Figure 2. Front panel view.

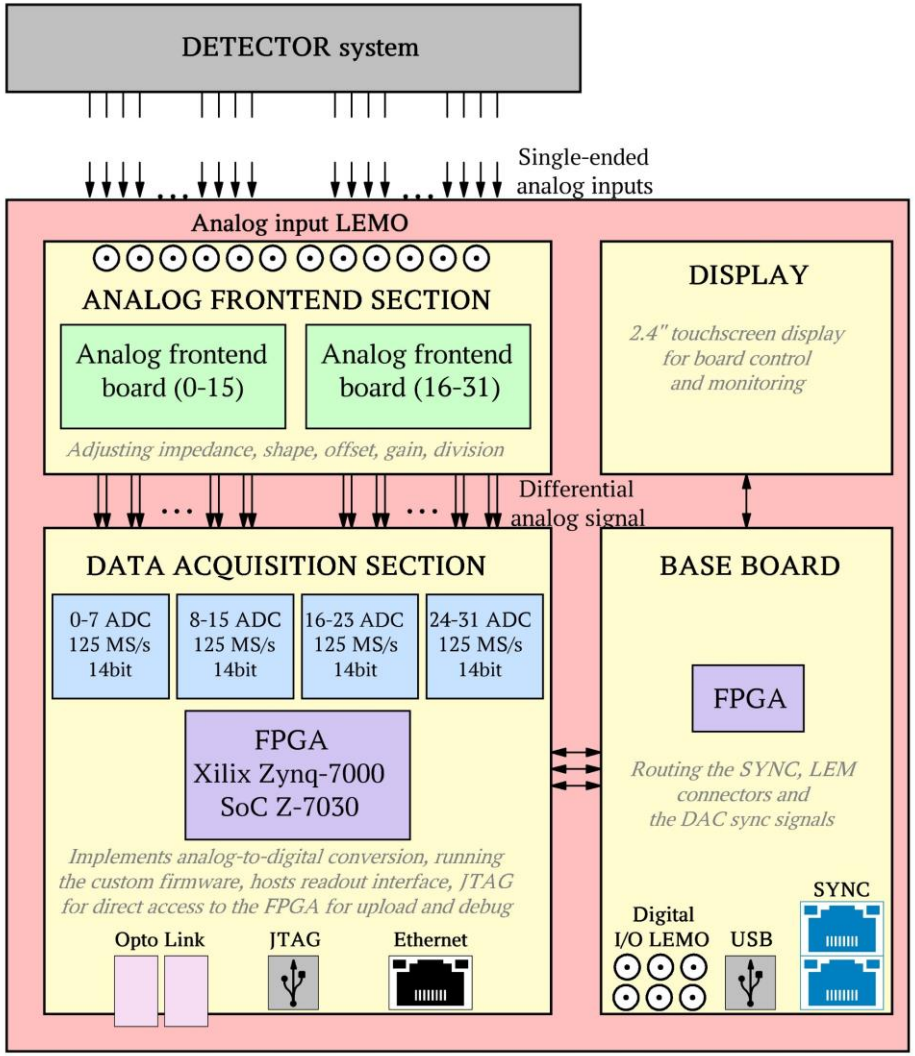


Figure 3. Block diagram of DT5560SE digitizer device

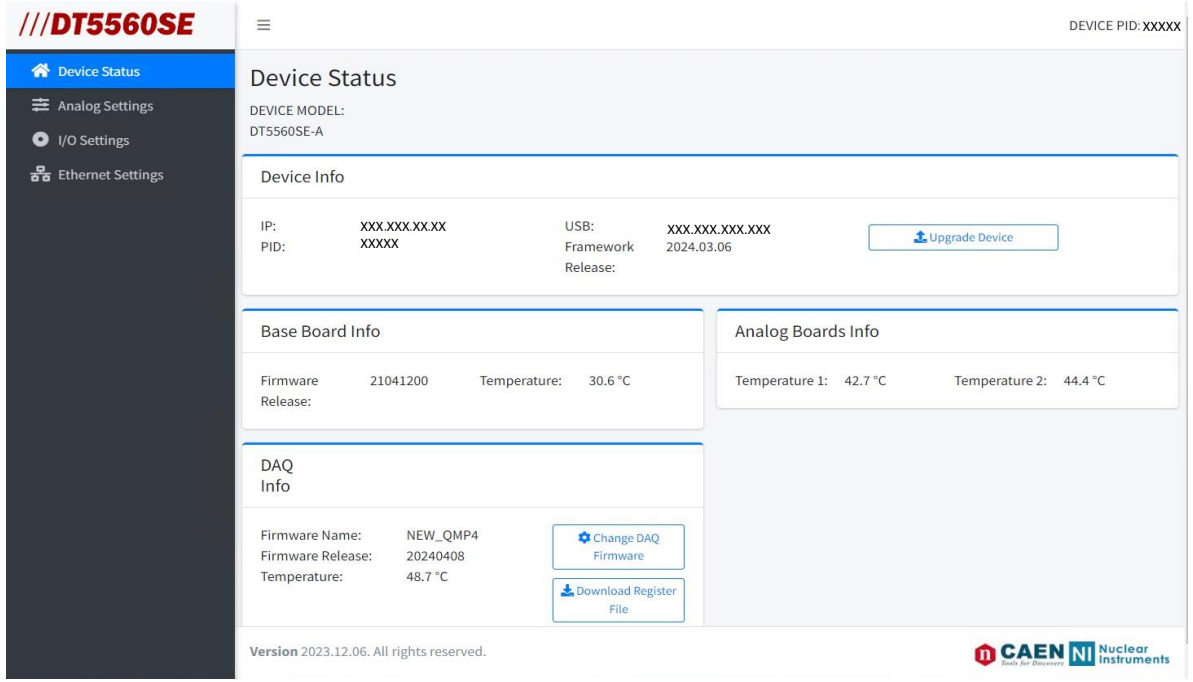


Figure 4. Embedded Web interface home page.

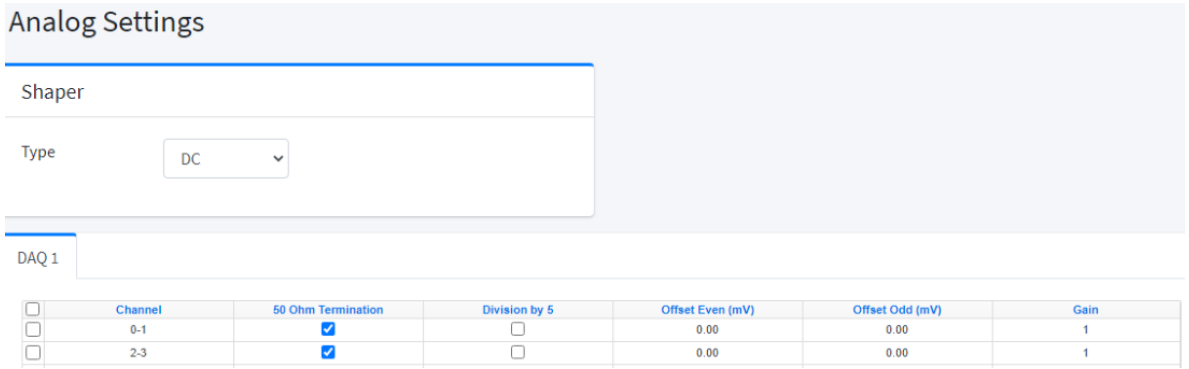


Figure 5. The Analog Settings page on Web interface.

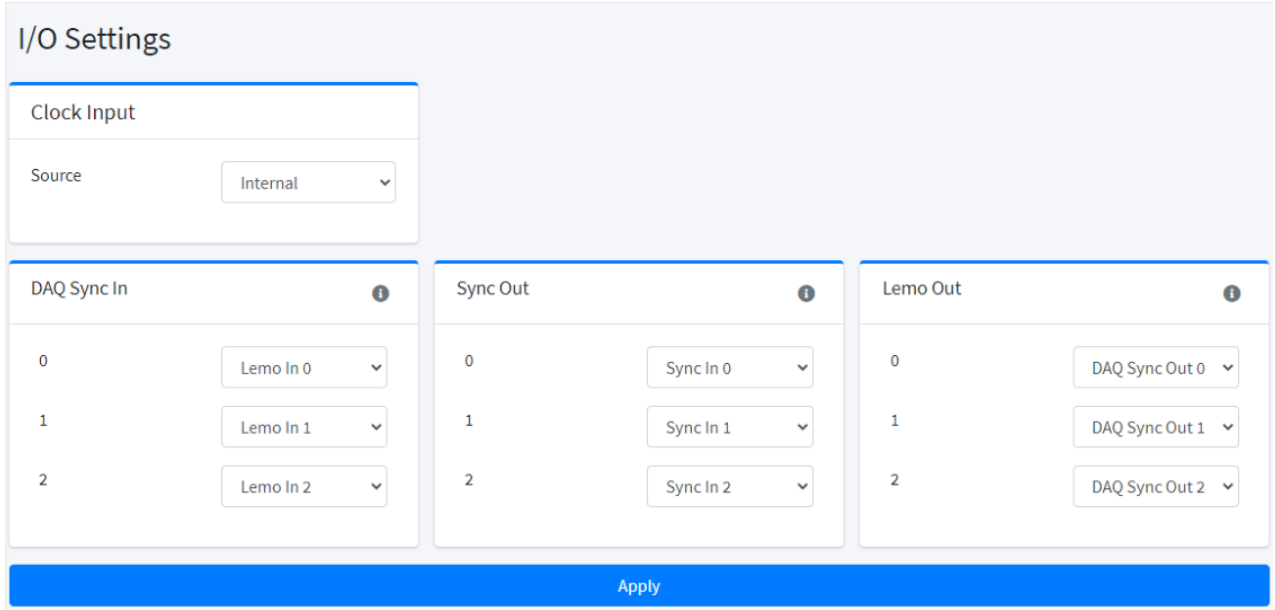


Figure 6. I/O Settings page.

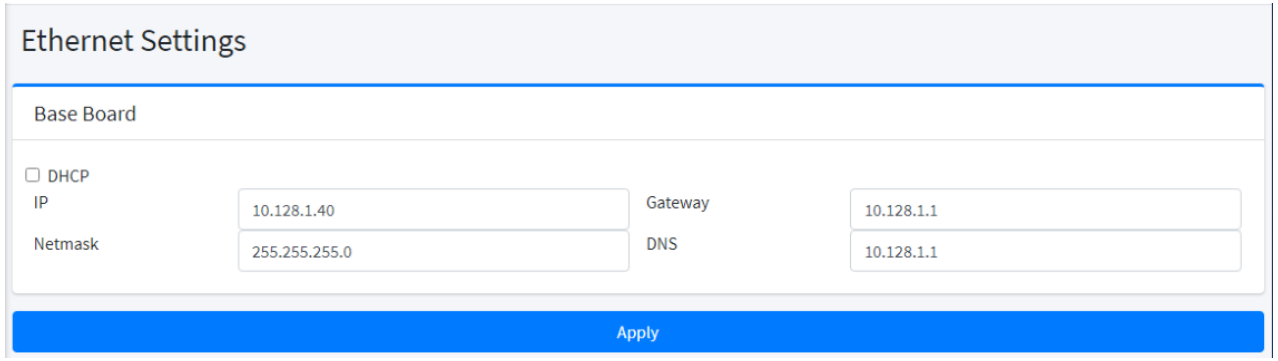


Figure 7. Ethernet Settings page.

Graphical Programming Language for CAEN Open FPGA boards

SCI-COMPILER Open FPGA

- Block Building Interface
- Automatic Firmware Code Simulation
- Debug with Resource Explorer

Sci-Compiler uses a set of high level functionalities (**IP blocks**) to mask the real firmware coding, which improves and speeds-up the R&D phase. Placing and interconnecting the available blocks on a diagram, it is able to automatically generate a **VHDL code** that implements the required function and deploy it to the **FPGA**.

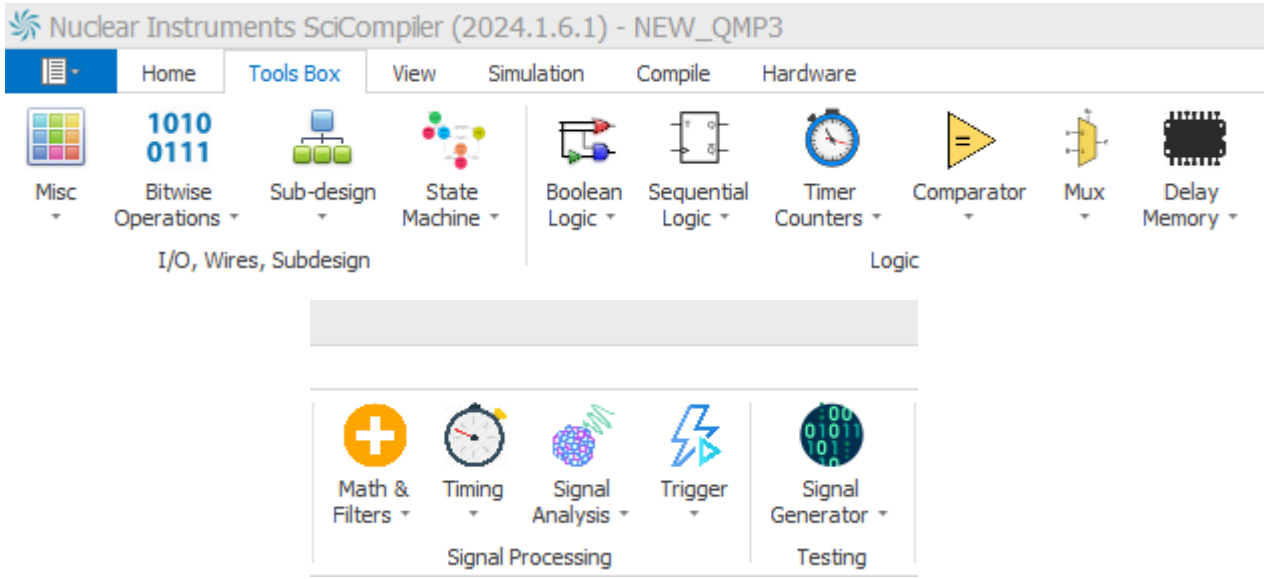
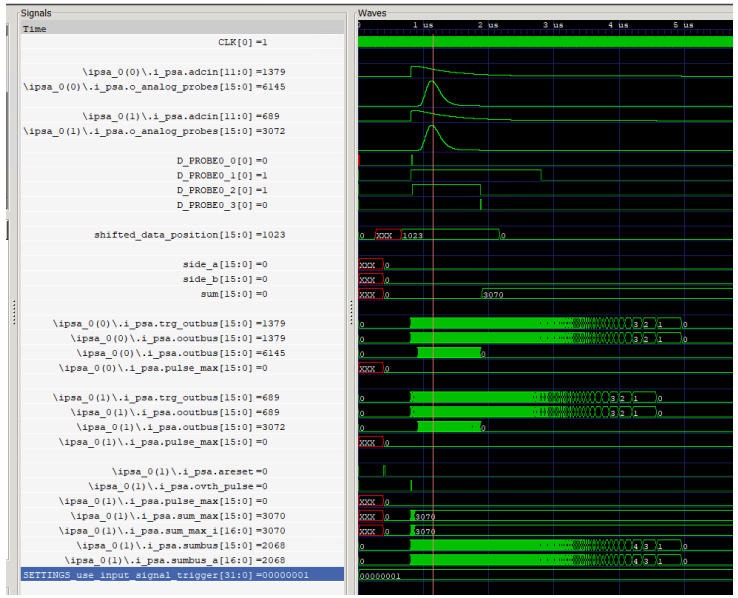


Figure 8. Tools Box with 100+ virtual blocks that works exactly as real laboratory instrumentation

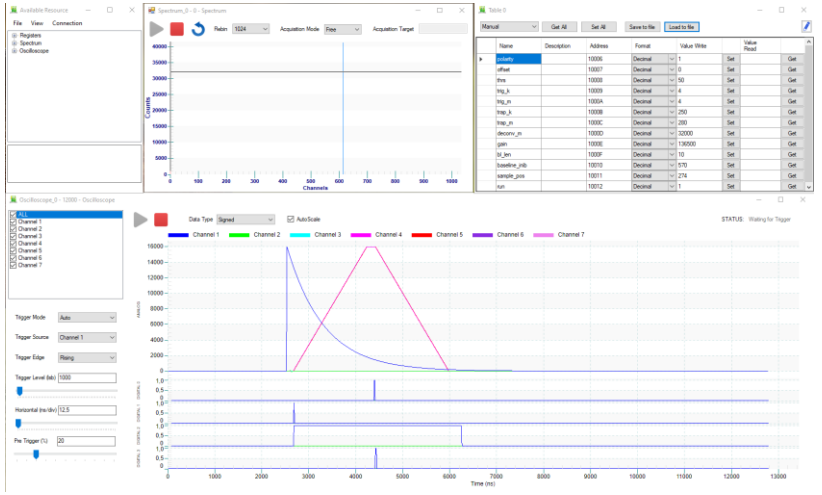
Automatic Firmware Code Simulation

Sci-Compiler allows to simulate the firmware code much faster than compilation, so the user can have a quick response on ***how the Signal Processing Algorithm implemented*** in the firmware is working. In fact, it is possible to add some input to the simulation (like an external signal) and set probing points in the block diagram. In this way it is possible to ***monitor the electrical signal*** in that point.



GTKWave is an analysis tool used to perform debugging on Verilog or VHDL simulation models.

Resource Explorer



Sci-Compiler offers a ***built-in tool***, called Resource Explorer, to connect supported boards and test the features of the FPGA firmware. This tool allows to manage all Local Bus readout blocks placed in the firmware diagram, therefore it gives the possibility ***to read and write*** the configuration registers (i.e. Signal Processing parameters) and ***shows the readout instruments*** like Spectrum, Oscilloscope, etc. in a GUI.

Measurement setup for testing digital processing system

Helium-3-filled linear position-sensitive detectors (LPSDs) are based on the position-sensitive proportional counters design and have been widely applied to neutron scattering instruments owing to the high detection efficiency, the excellent neutron/gamma discrimination, and the ability to construct the detector with large area coverage.

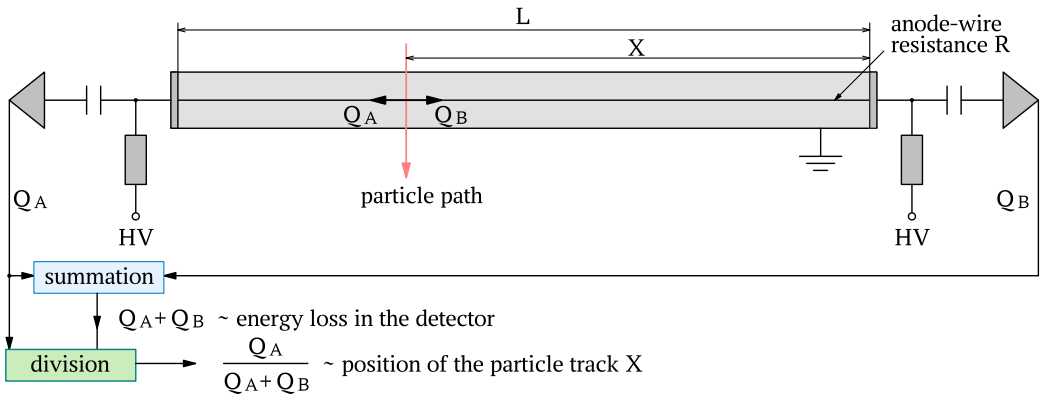


Figure 9. Schematic diagram of position determination in a Helium-3 filled position sensitive proportional counters

Научно-производственная фирма Консенсус
Scientific-Production Firm CONSENSUS

^{3}He – счетчик медленных нейтронов
^{3}He – neutron counter

Гелий–PSD–8/600–12,5/Л
Helium–PSD–8/600–12,5/L

Effective length, mm	586	Own background, count/s	0.15
^{3}He pressure, atm	10	Variation of sensitivity regarding the sample, %	5
Operating voltage for proportional mode, V	900	Position resolution, mm	4 max*
Operating voltage for PSD mode, V	1350	Anode resistance, Ohms/m	9400
Peak width at half height, %	15 max	Operation temperature range, ℃	-50÷60
Variation of the position of the peak of the mean value in a party, %	15 max	Weight, g	37

* - The position resolution essentially depends on the used measuring equipment.

This feature is taken from the Consensus website: *consensus-group.ru*

Measurement setup for testing digital processing system

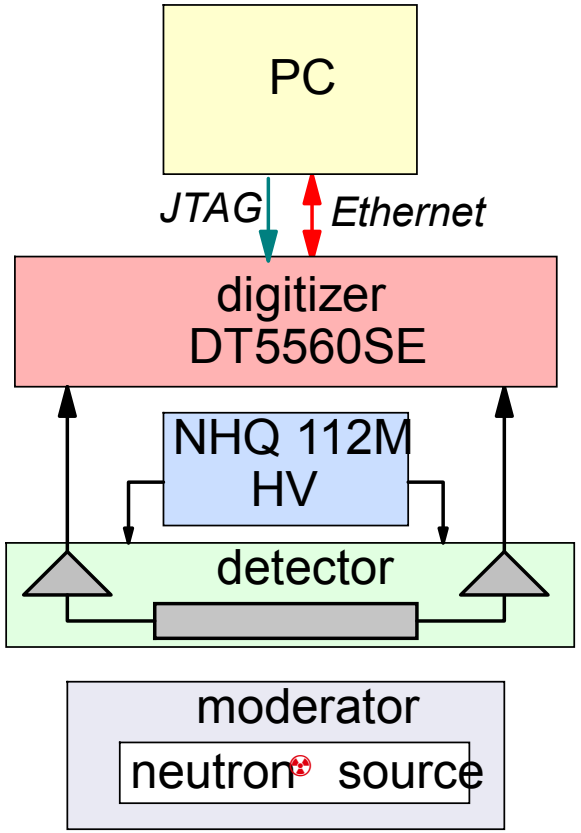


Figure 10. Block diagram connecting of installation

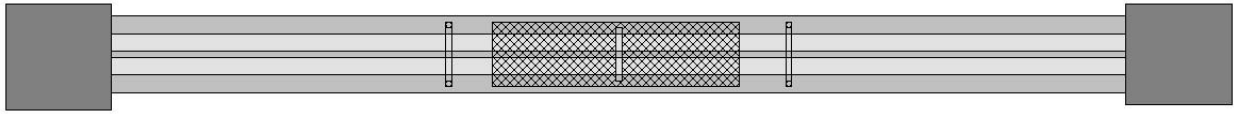
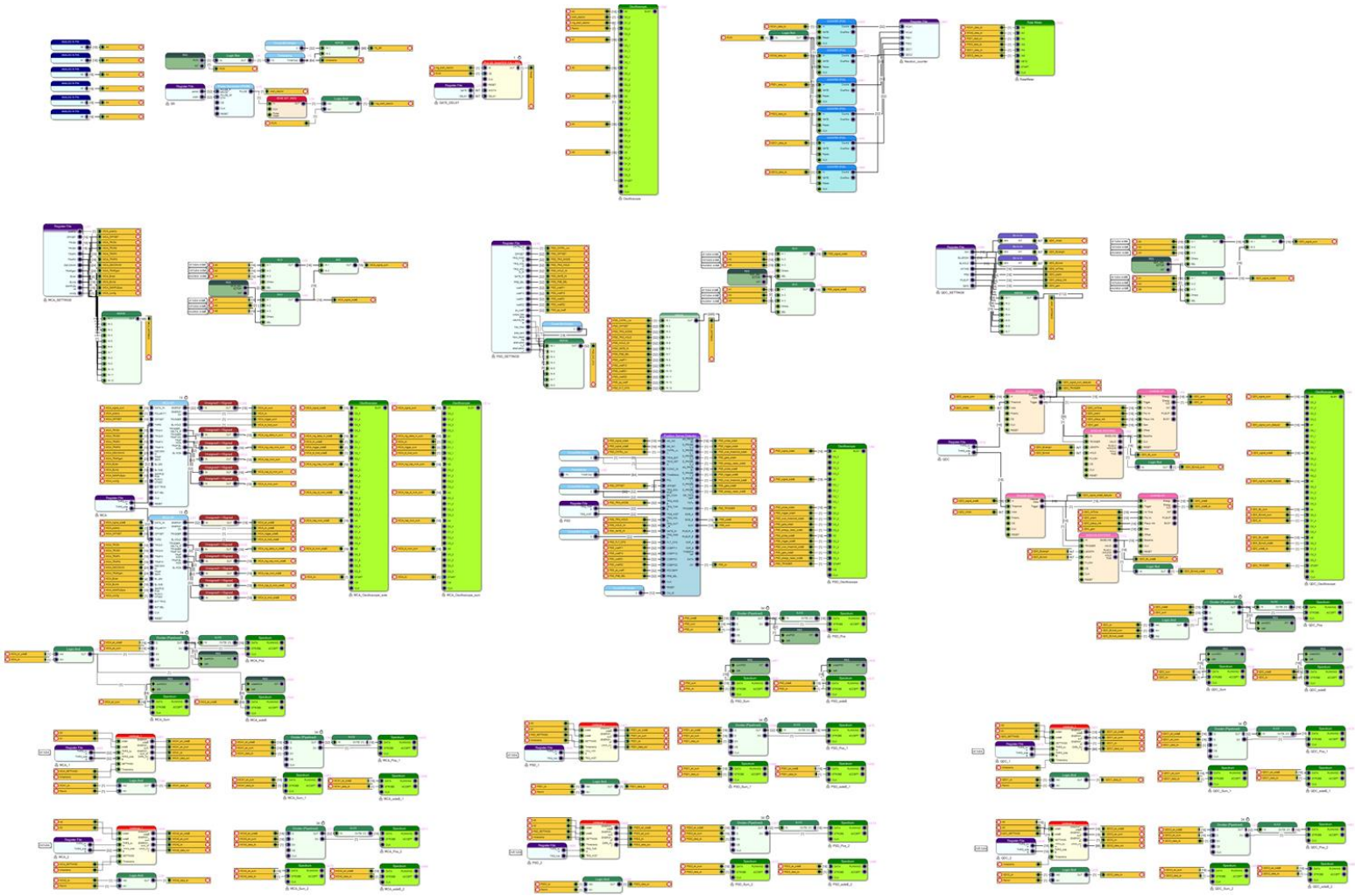


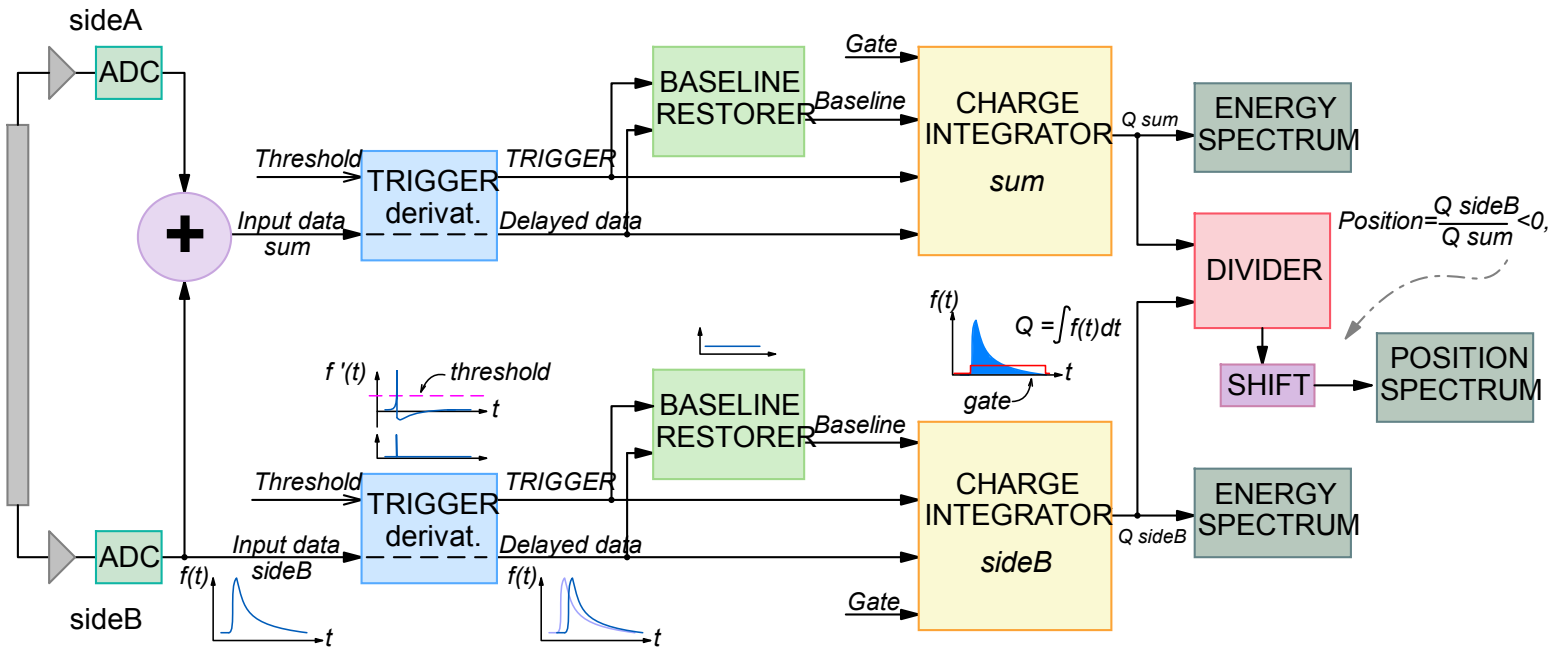
Figure 11. Schematic representation of the tubes and placement of a cadmium mask with a slide.

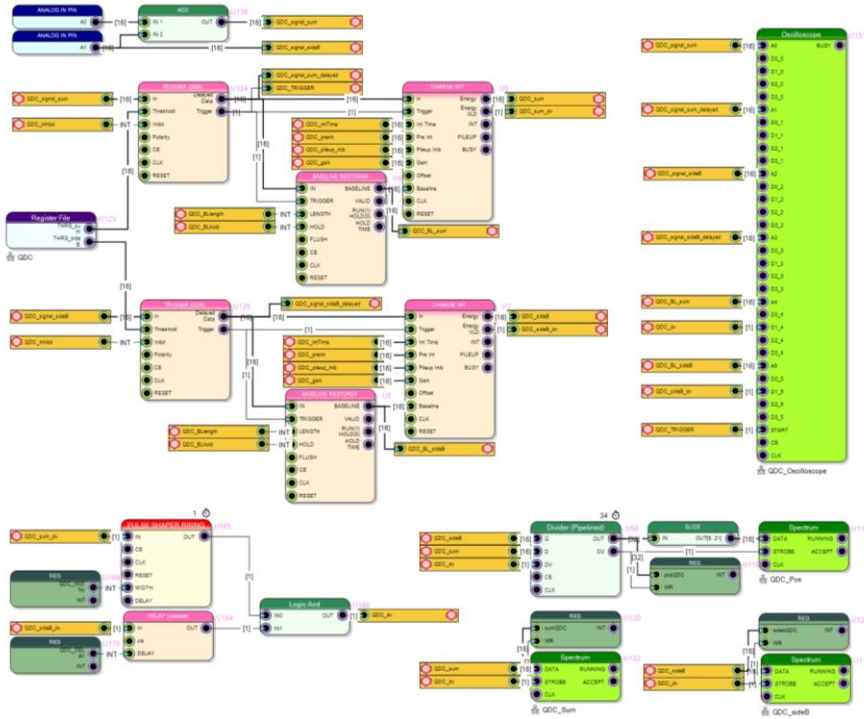
Figure 12. Part of a test setup with source, moderator and detector

Program for measurement and testing digital processing system



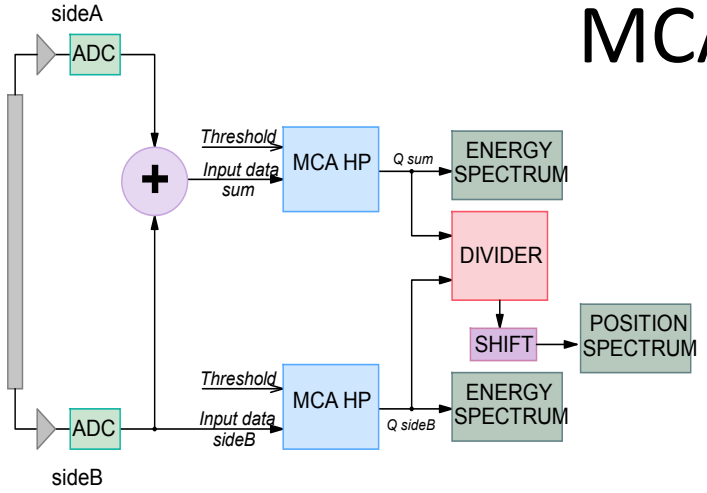
QDC («Charge-to-Digital Converter»)

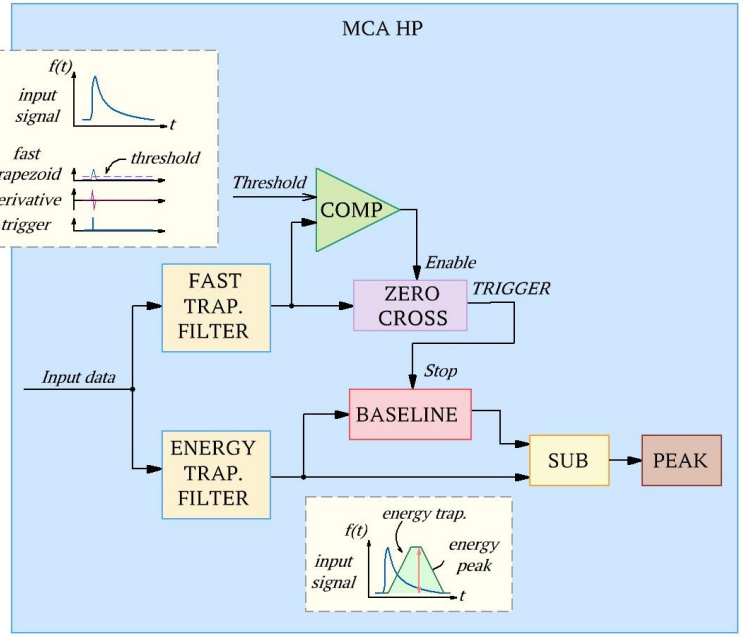


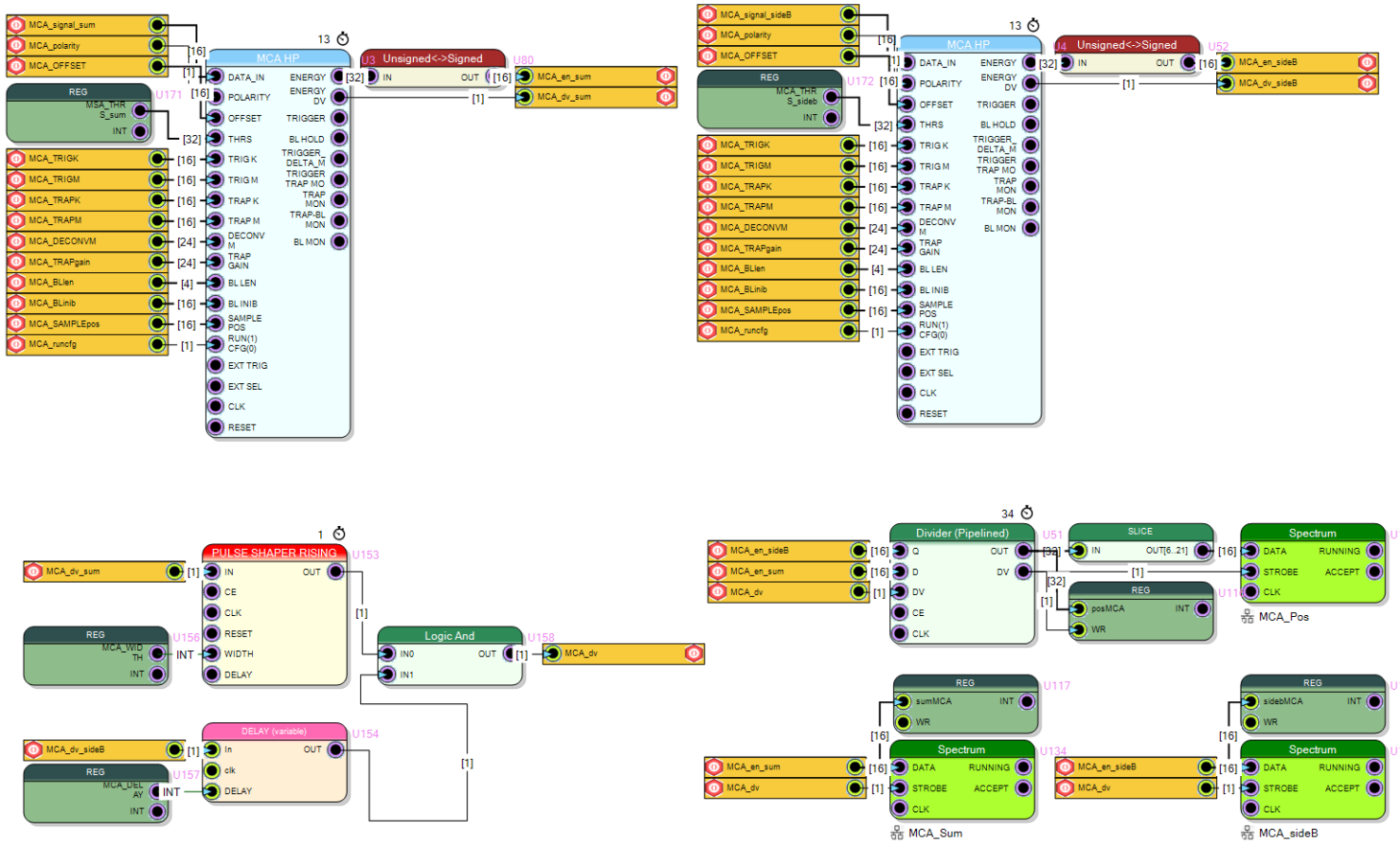


QDC methods and program workspace Sci-Compiler

MCA HP («Multi Channel Analyzer»)

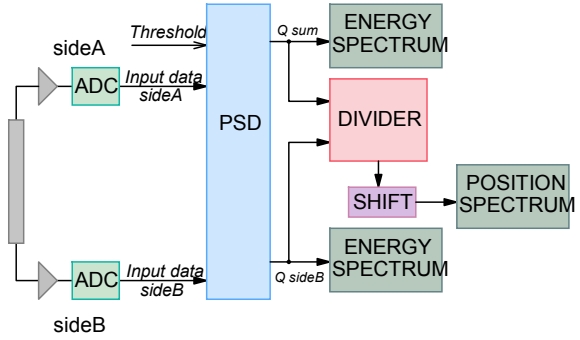


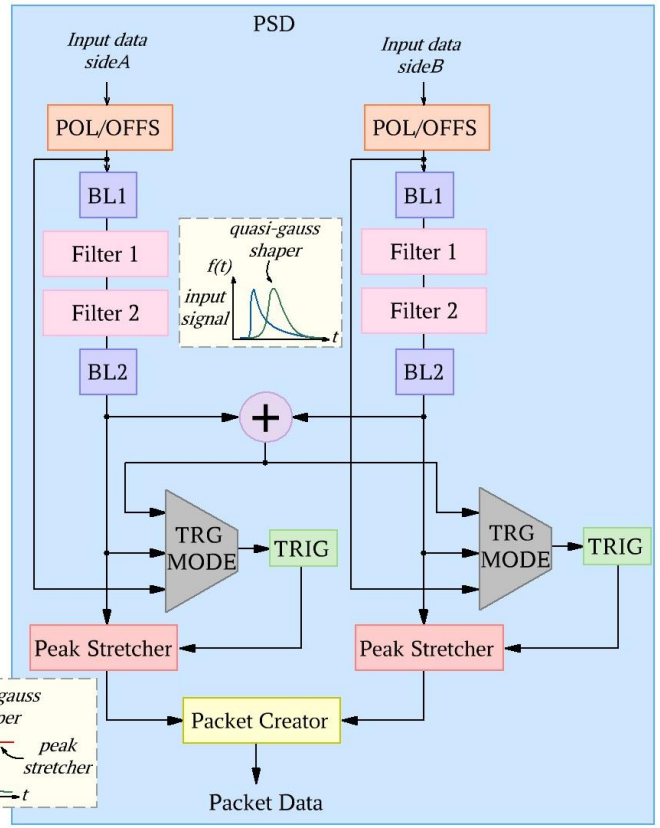


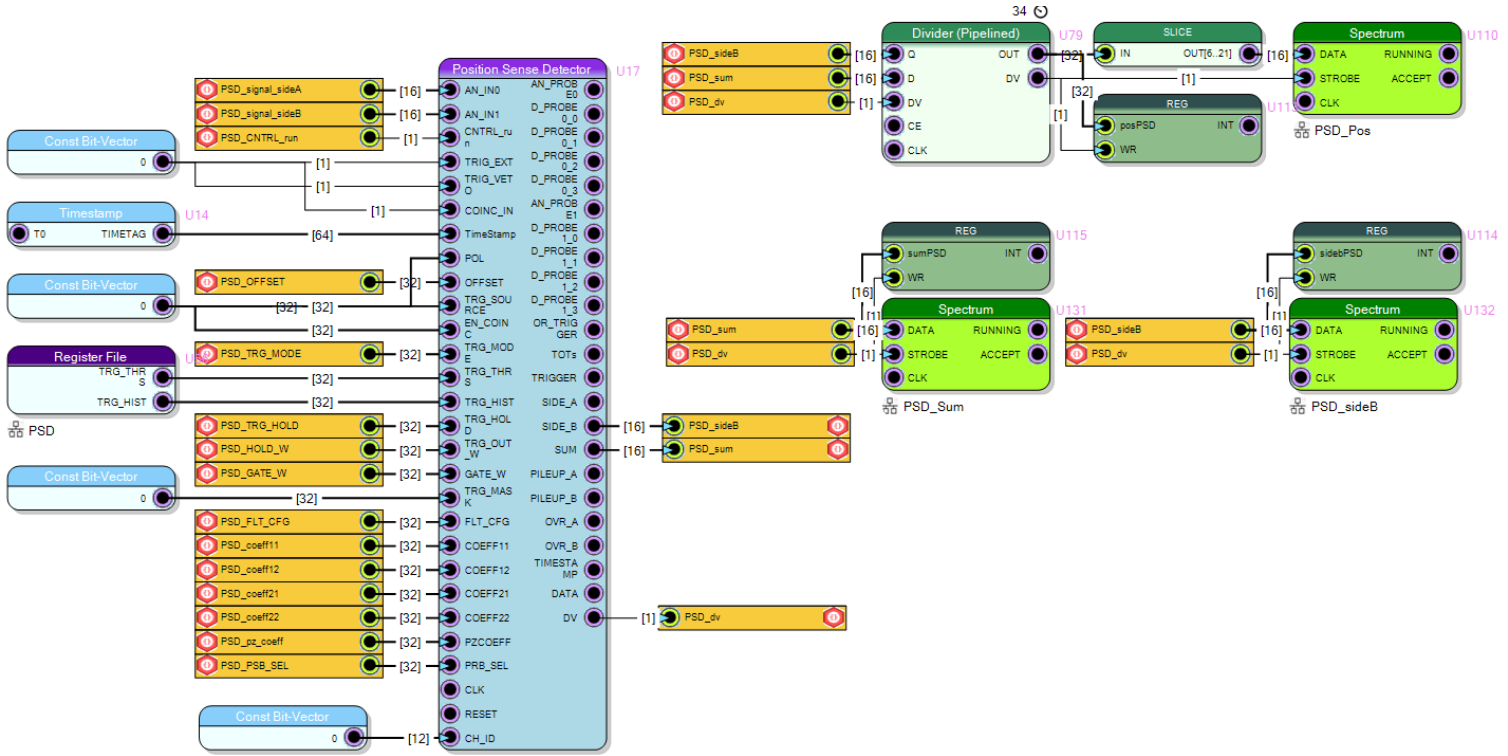


MCA HP methods and program workspace Sci-Compiler

PSD («Proportional Amplitude Position Sense»)







PSD methods and program workspace Sci-Compiler

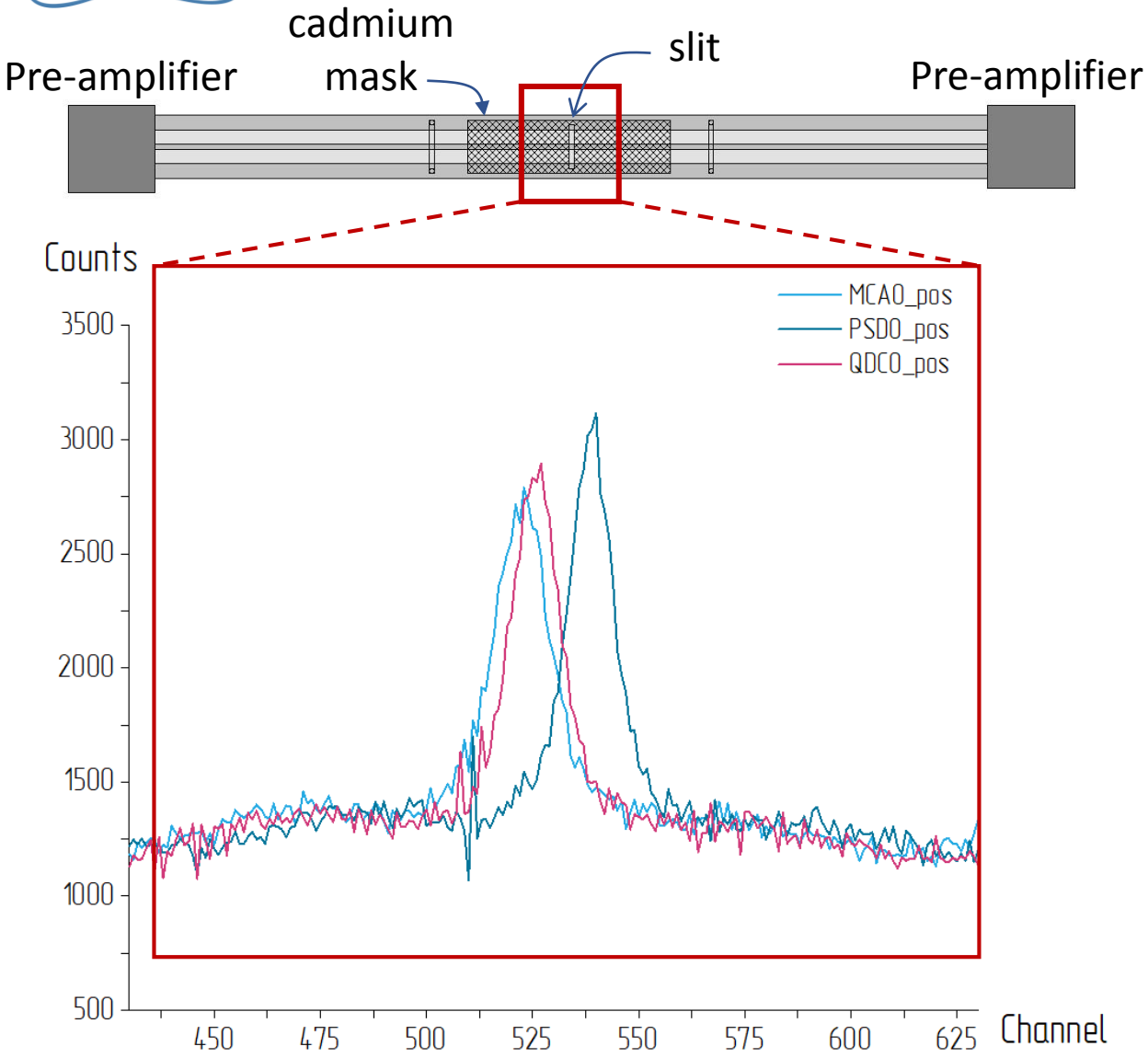


Figure 16. Slit positional resolution by three methods.

Table 1. Measurement results of the test system.

Method	Dead time methods, us	FWHM slit, channel	Position resolution, %
MCA HP	4,8	15,7	**1,8**
PSD	2	12,7	**1,45**
QDC	2	13,8	**1,56**

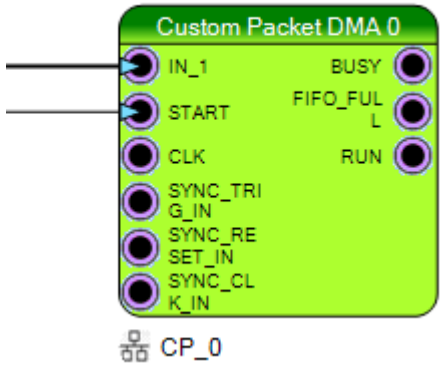
Short summary:

- Tube measurements require more extensive analysis and refinement.
- Digitizer and FPGA programming software Sci-Compiler cover almost all needs for setting up an experiment.

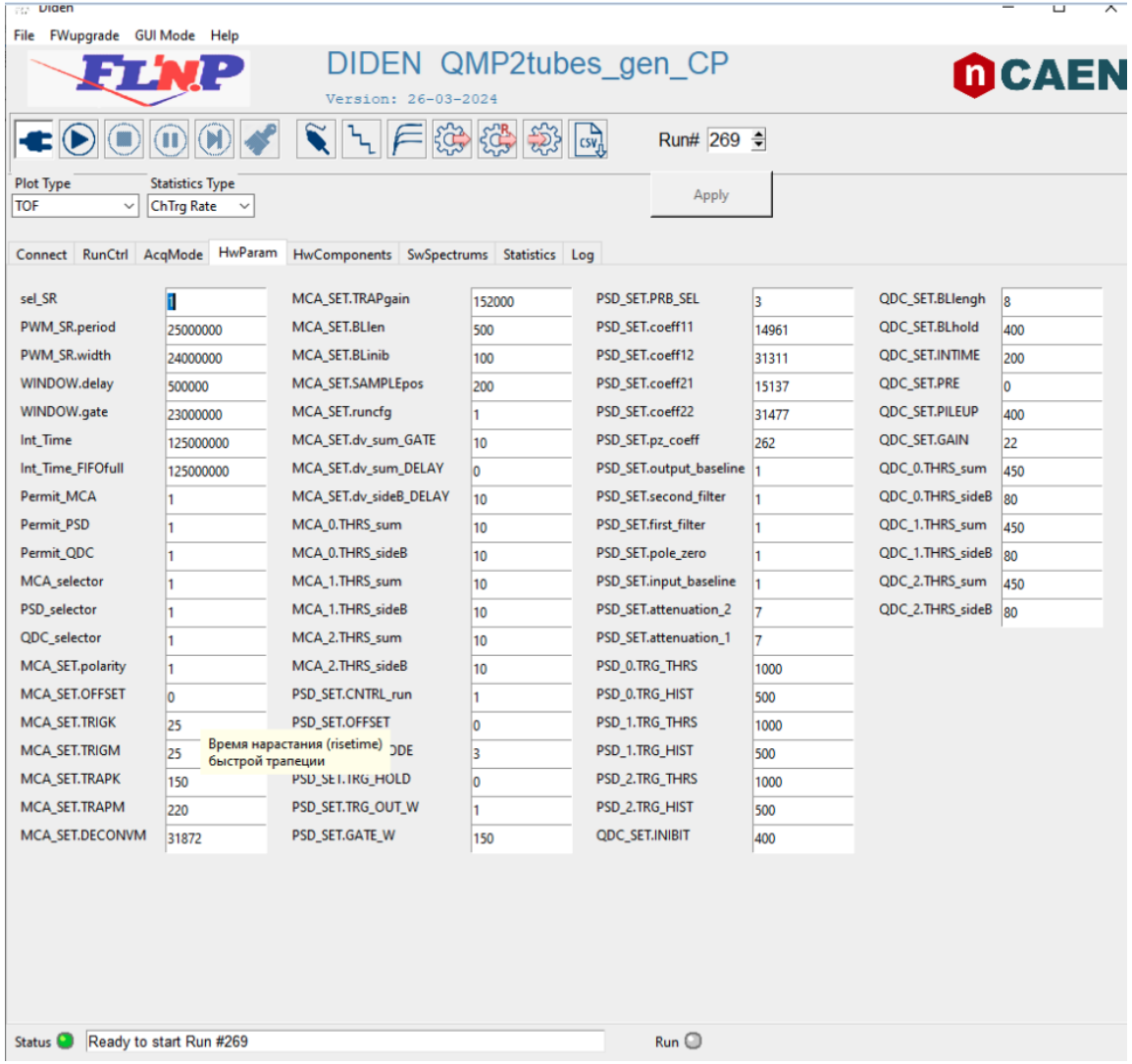
Next steps.

- Implementation of list mode data transfer between hardware memory and PC using DMA (direct memory access) technology.
- Tests and measurements using specially developed software interfaces (see next slide).
- Optimization of all set of project parameters

To speedup the data transfer in list mode, we use Custom Packet DMA SciCompiler IP.
Since all data transfer processes occur at the software level, Resource Explorer is no longer enough for us to set the parameters of this data transfer. We need our own software for this purpose.



DMA. The DMA allocate in the device 16 MWORD (word = 32 bit) FIFO in the DDR3 of the device; this allows to sustain a much higher event rate in respect of the standard custom packet. The DMA buffer is allocated in the device and the data are transferred to the PC using ZMQ socket.



DIDEN - software tool for DAQ and configuring all project parameters, including data transfer parameters between hardware memory and PC.

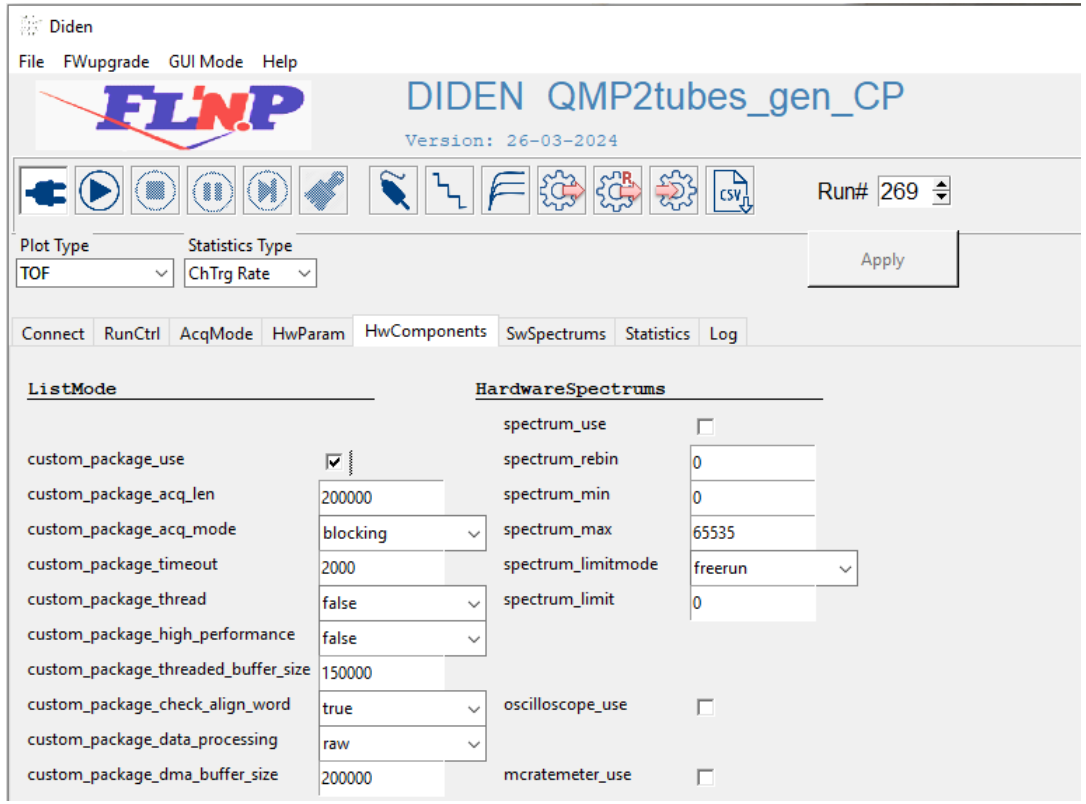


Figure 17. DIDEN – FLNP software for OpenFPGA-based projects (DAQ and flexible configuration).

Conclusion:

In my statement, I showed the main stages of the project development for signal processing of a helium-3-filled position-sensitive detector.

The methods of signal processing from such detectors are considered, the known feature of which is high and unstable rise time of signals, so for each series of detectors it is necessary to select the optimal method of signal processing from this detector.

Thank you for your patience!

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