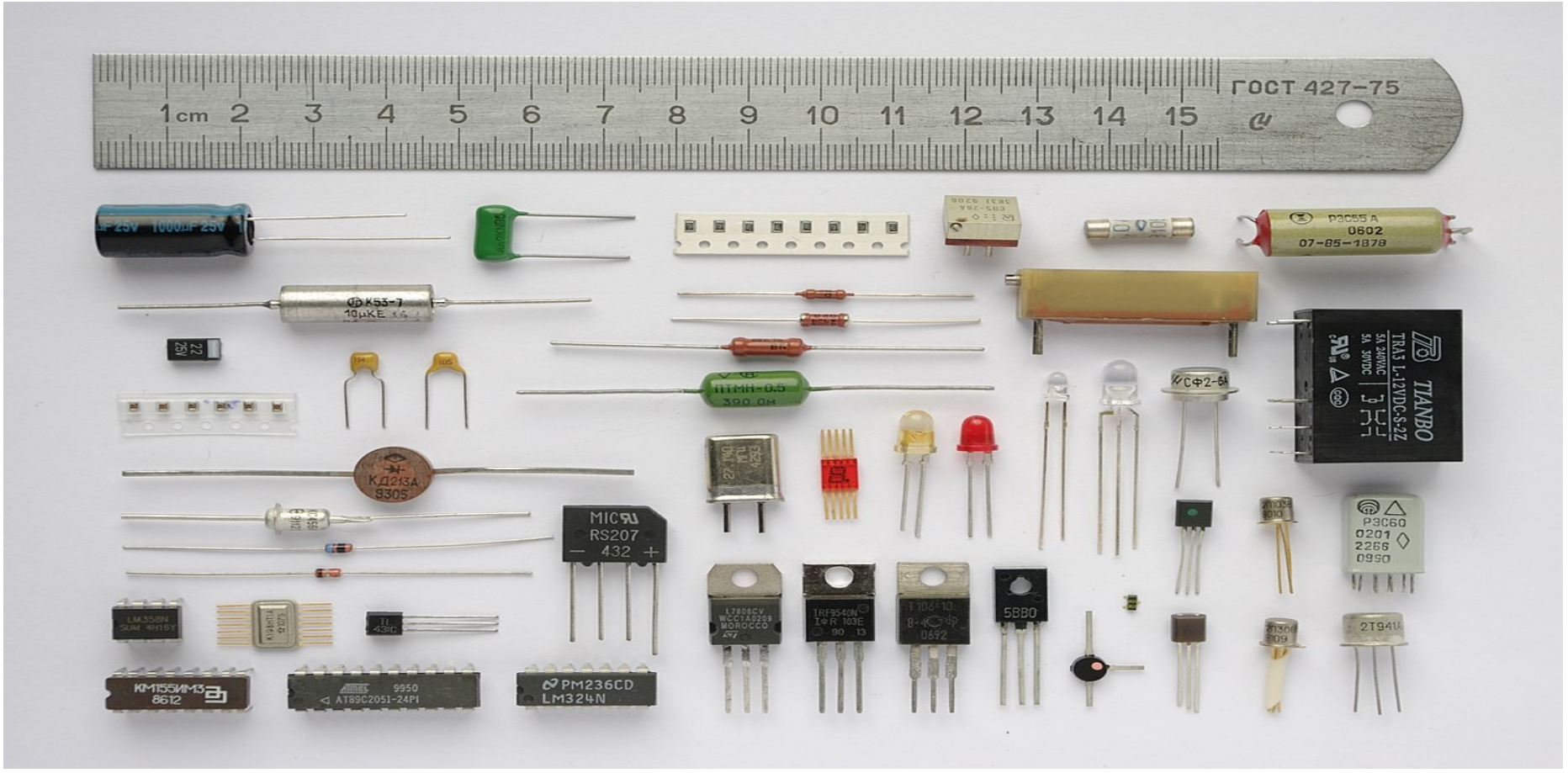
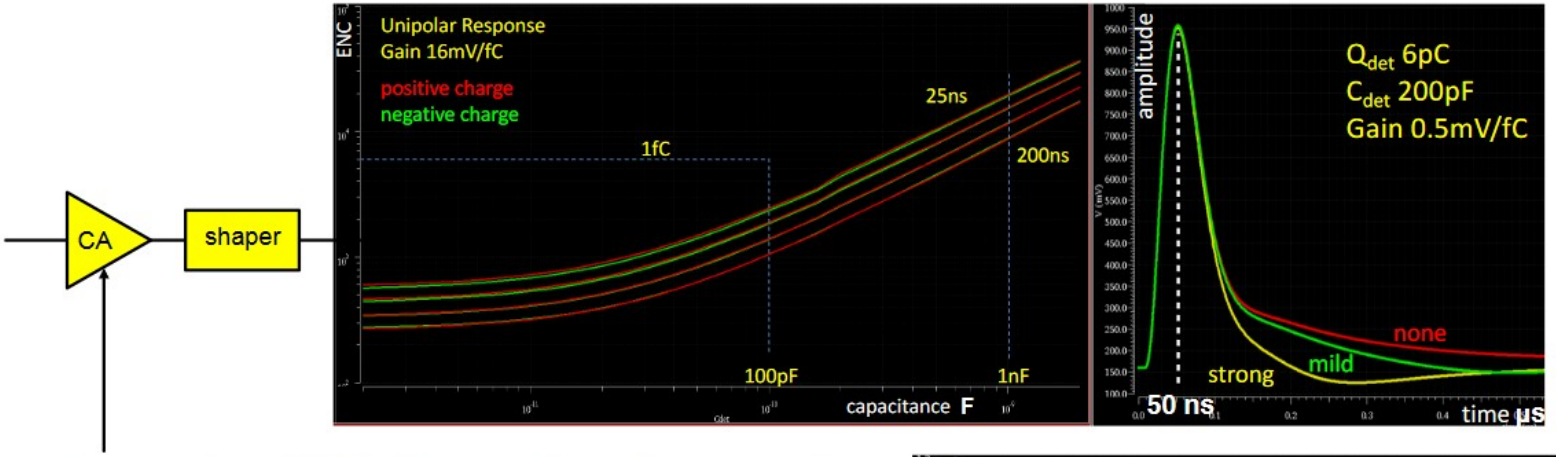
STT FE Electronics **Update**



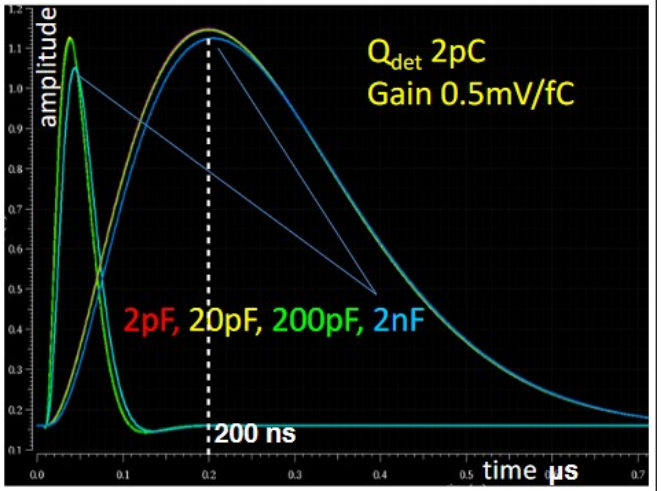
V. Bautin for Straw Tracker Team

06 JUN 2024

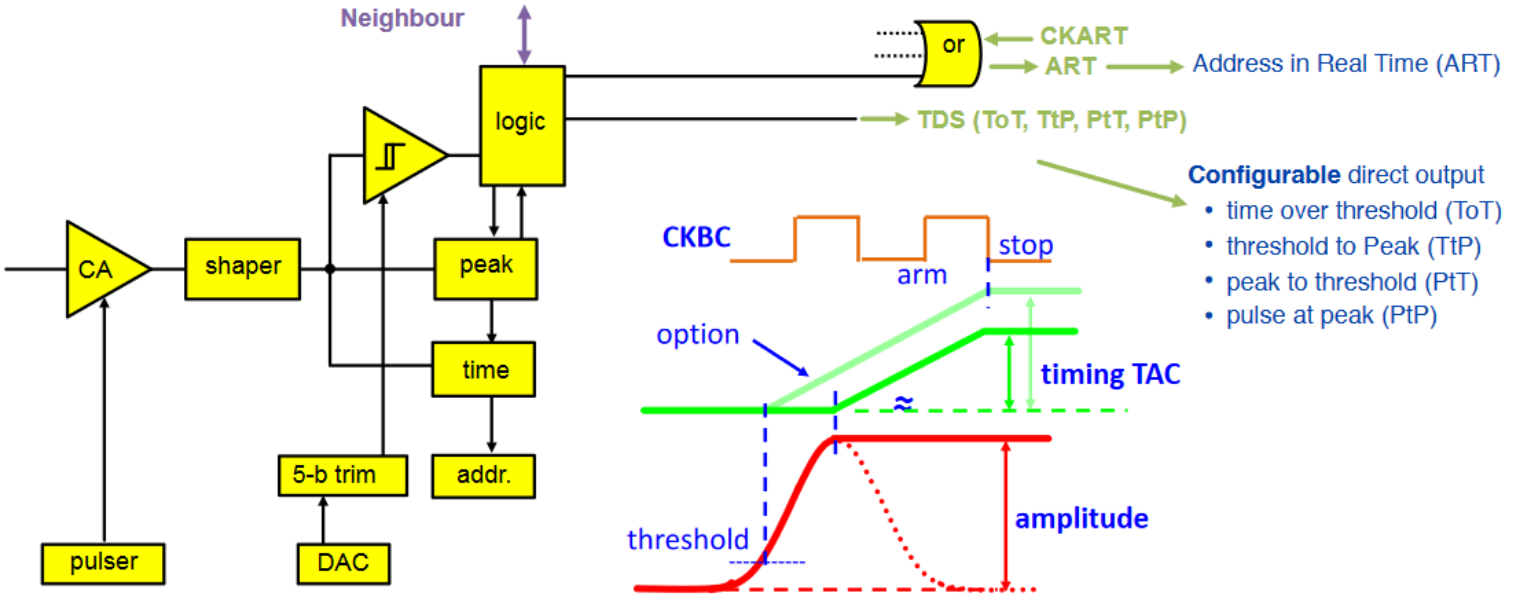
VMM **Amplifier & Shaper**



- Input transistor: **PMOS** 180 nm x 20 nm, 3 stage amplifier,
  - 2 stages used for **adjustable gain**: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
  - 1 for **adjustable charge polarity**: positive or negative
- Input **capacitance**: can operate from sub-pF to several nF
- Maximum **charge**: 2 pC in **linear range**, **fast recovery** from 50 pC
- Semi gaussian DDF c-**shaper 3rd order**
  - **Configurable** ion tail **suppression**: none, mild or strong
  - **Adjustable peaking** time: 25, 50, 100, 200 ns
  - Leakage-adaptive, **BGR-stabilised baseline**

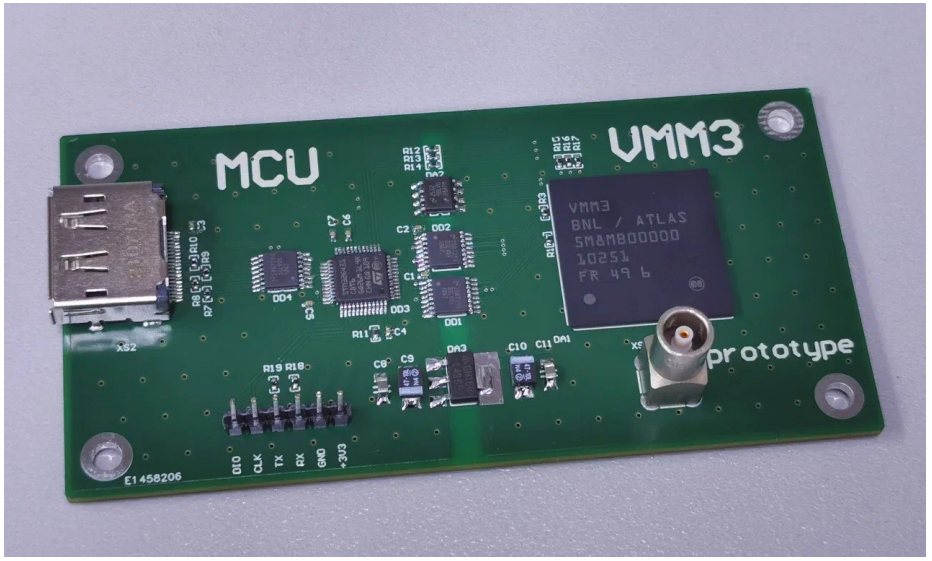


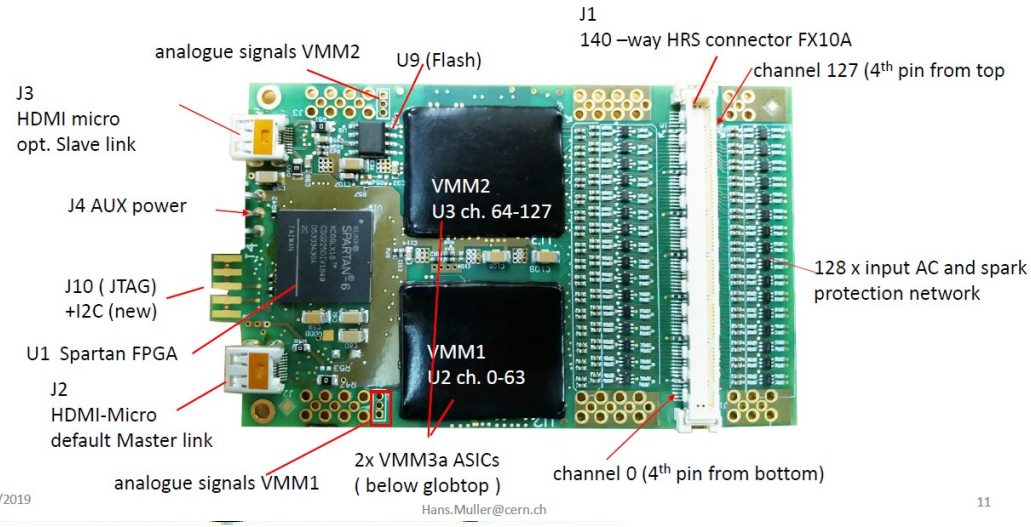
VMM3a **Discrimination, Charge and Time**

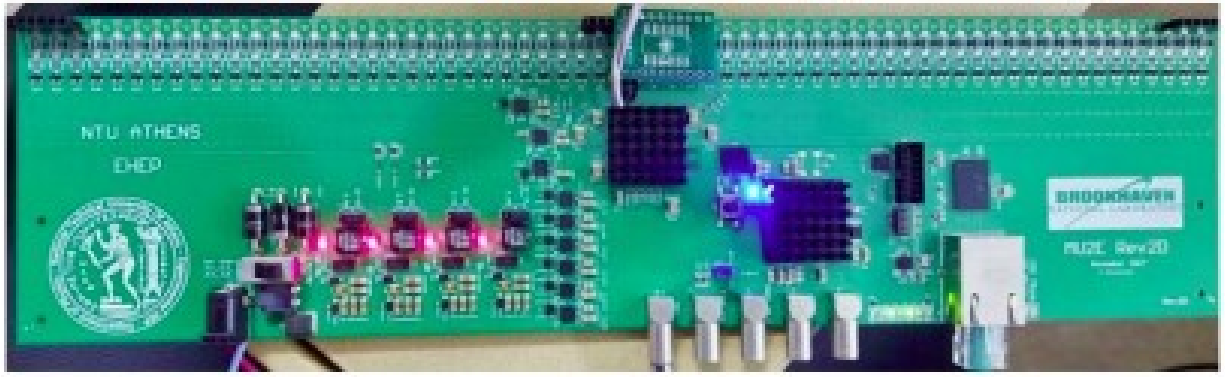


- Global 10-bit DAC for adjusting the **threshold** - **Discrimination** with sub-hysterisis (effective 2mV)
- Adjustable **5-bit discrimination** threshold **per channel** to adjust at ~mV level
- **Neighbour** logic to trigger sub-threshold channels with inter-chip communication
- Configurable **direct output** per channel and serial fast output of address as an OR of all channels
- **Peak detection**: measurement of peak **amplitude** and storage in analog memory
- **Time detection**: measurement of **peak/threshold** timing through a configurable time to amplitude converter (**TAC**: 60, 100, 350, 650 ns) and storage in analog memory
  - Clock working mode on **synchronous** machines but also as strobe for **asynchronous** operations

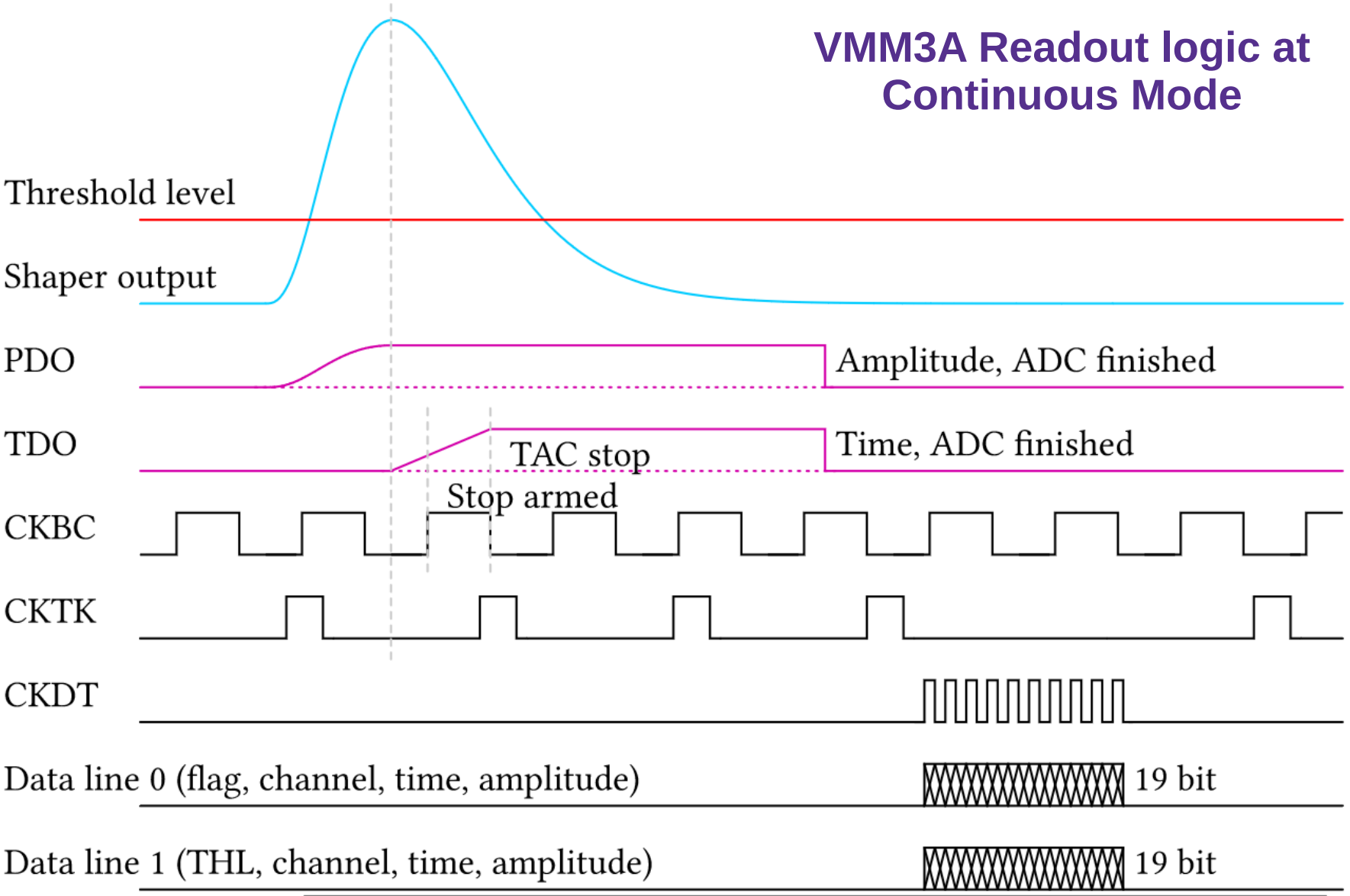
First FEB prototype, as well as existing Mu2E board and SRS Hybrid boards was tested at several SPS Testbeams and in the lab. Issues were found.



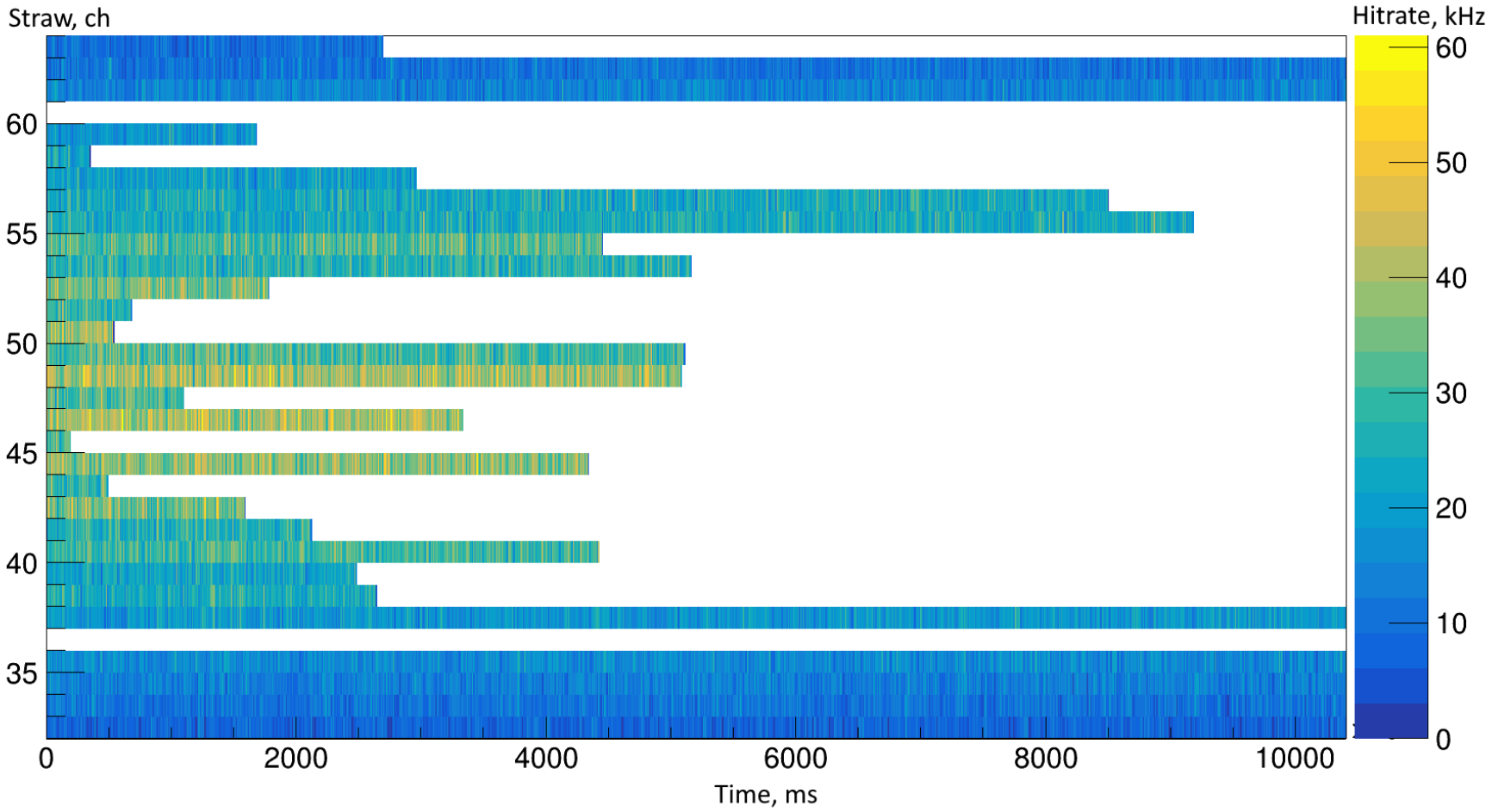




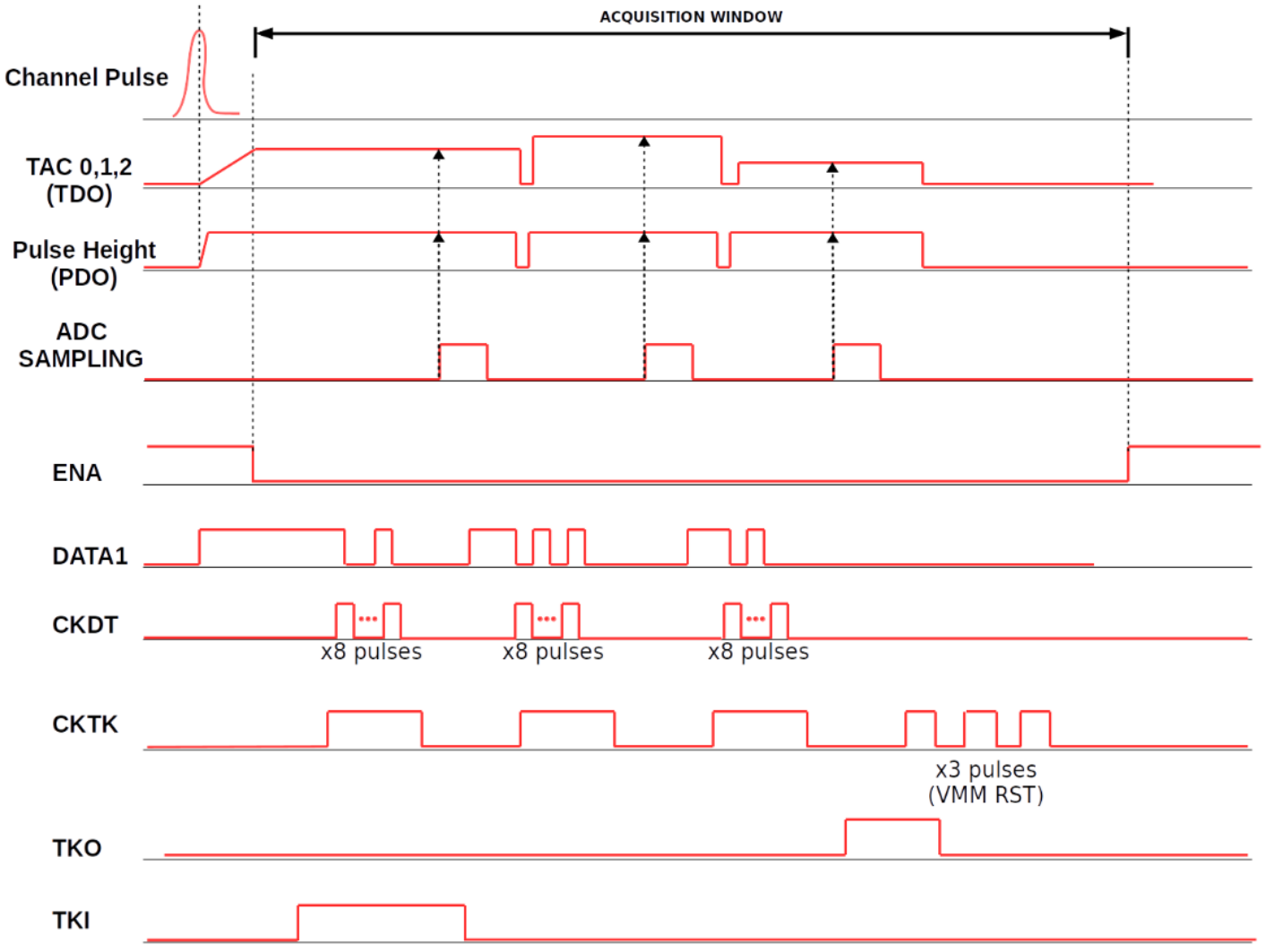
VMM3A Readout logic at Continuous Mode



Channels latch at T@T mode (VMM3A)

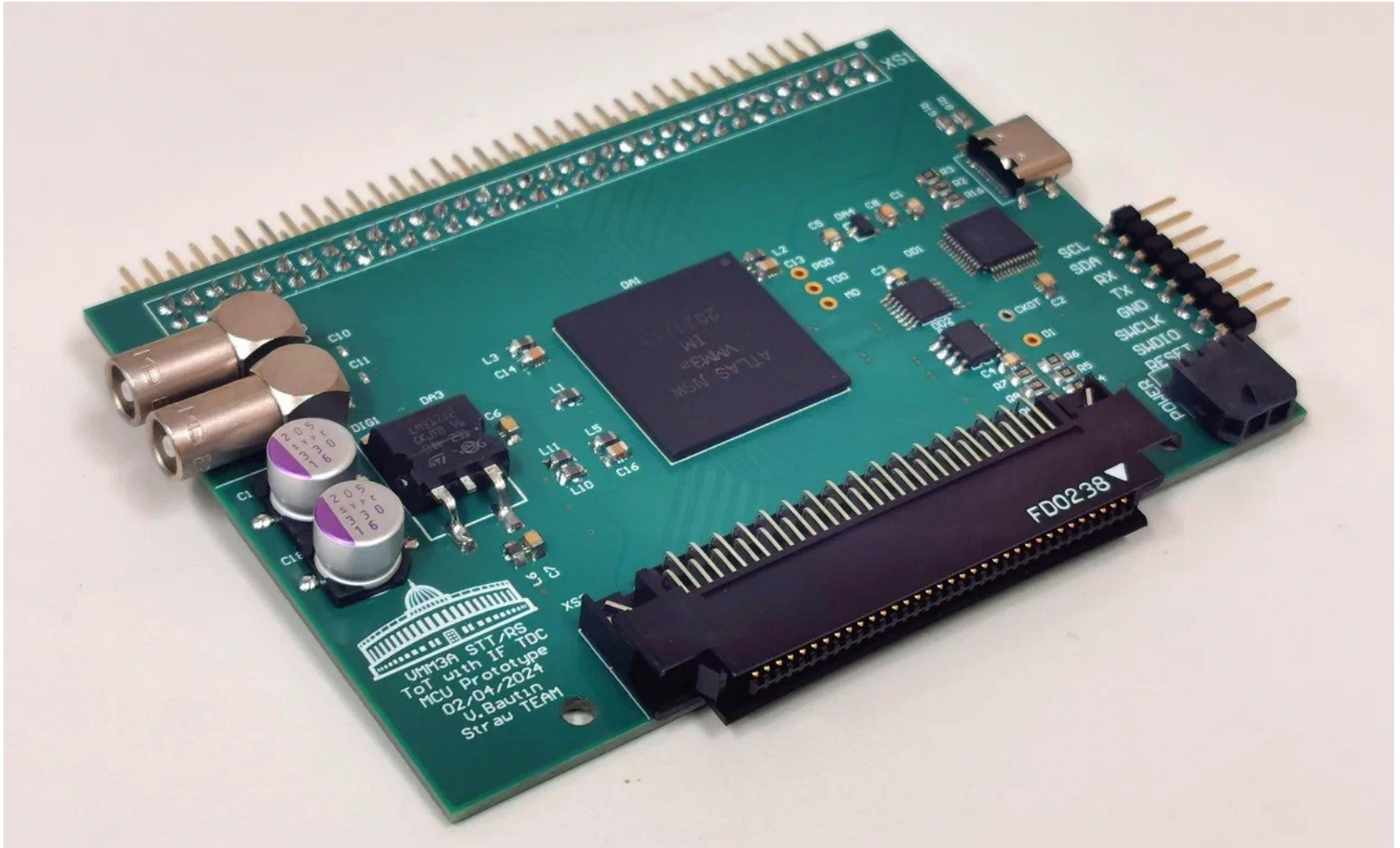


The VMM3/3A has alternative «External ADC» Mode which should handle both saturation issue, channel latching problem and ADC resolution

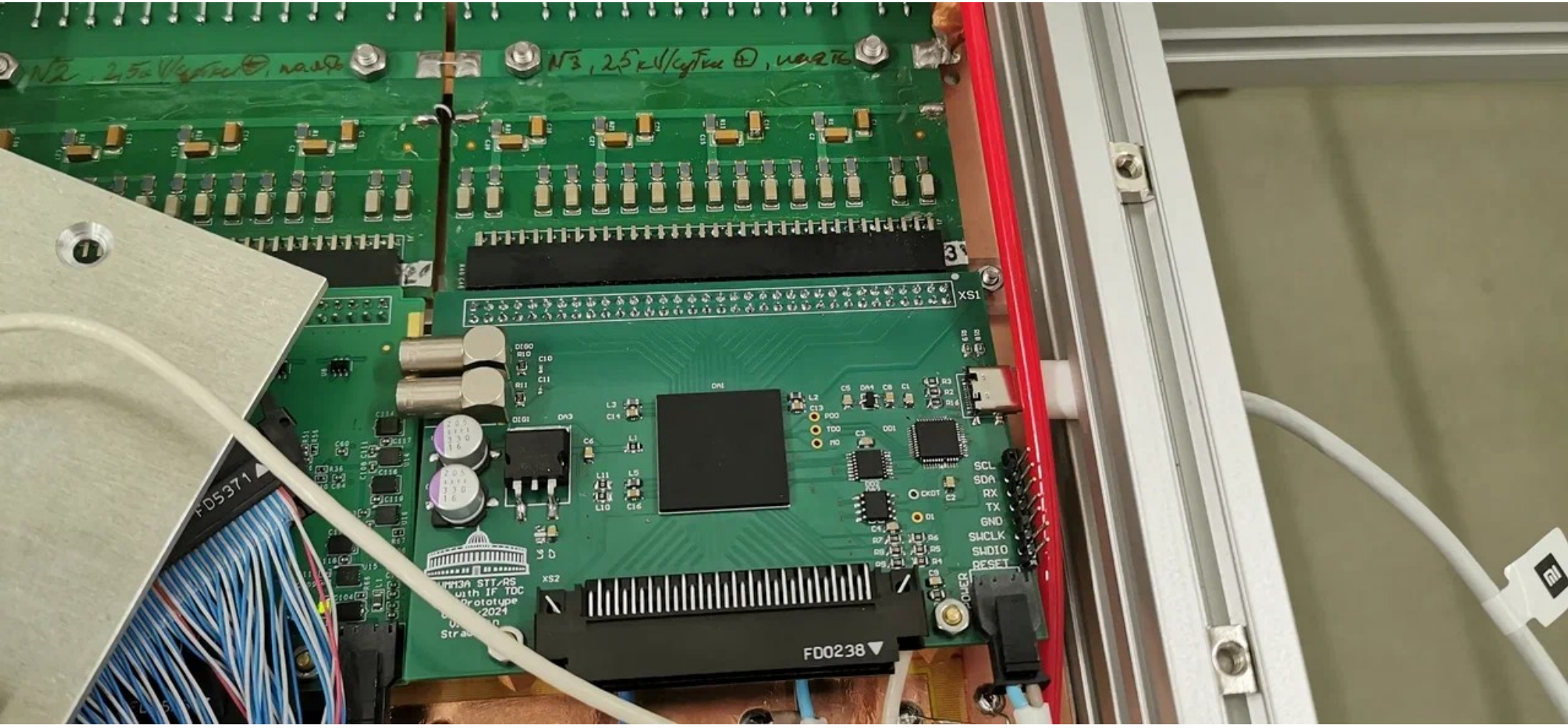


- Once the process is complete the **ASIC can be switched readout phase**. The first set of amplitude and time voltages is made available at the **analog outputs**. The **address of the channel is serialised** and made available at the digital output using **six data clocks**.

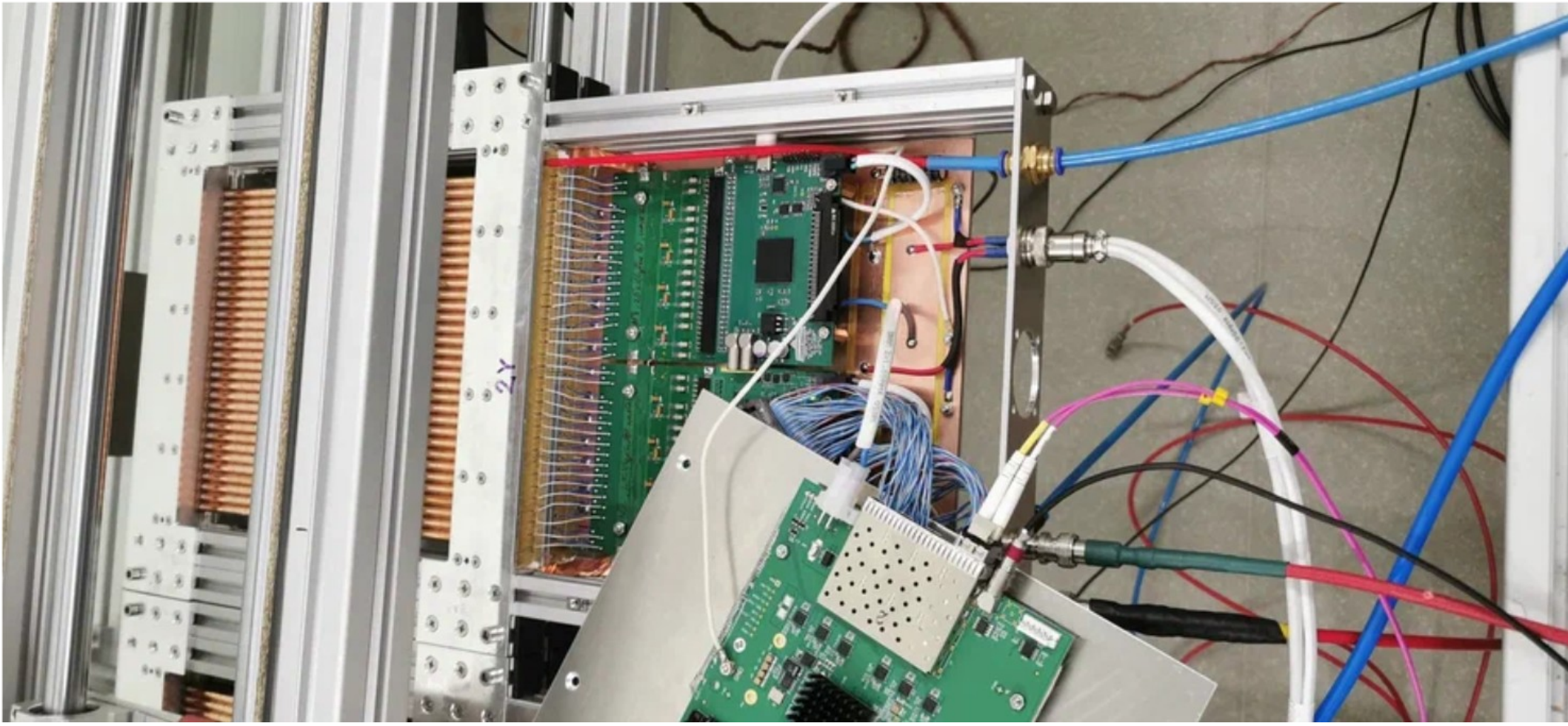
A **new FEB** based on **VMM3A** has been developed and assembled. It uses «new» external ADC Mode with **12-bit 4MSPS ADC**. First results on next slides. Testing is ongoing.



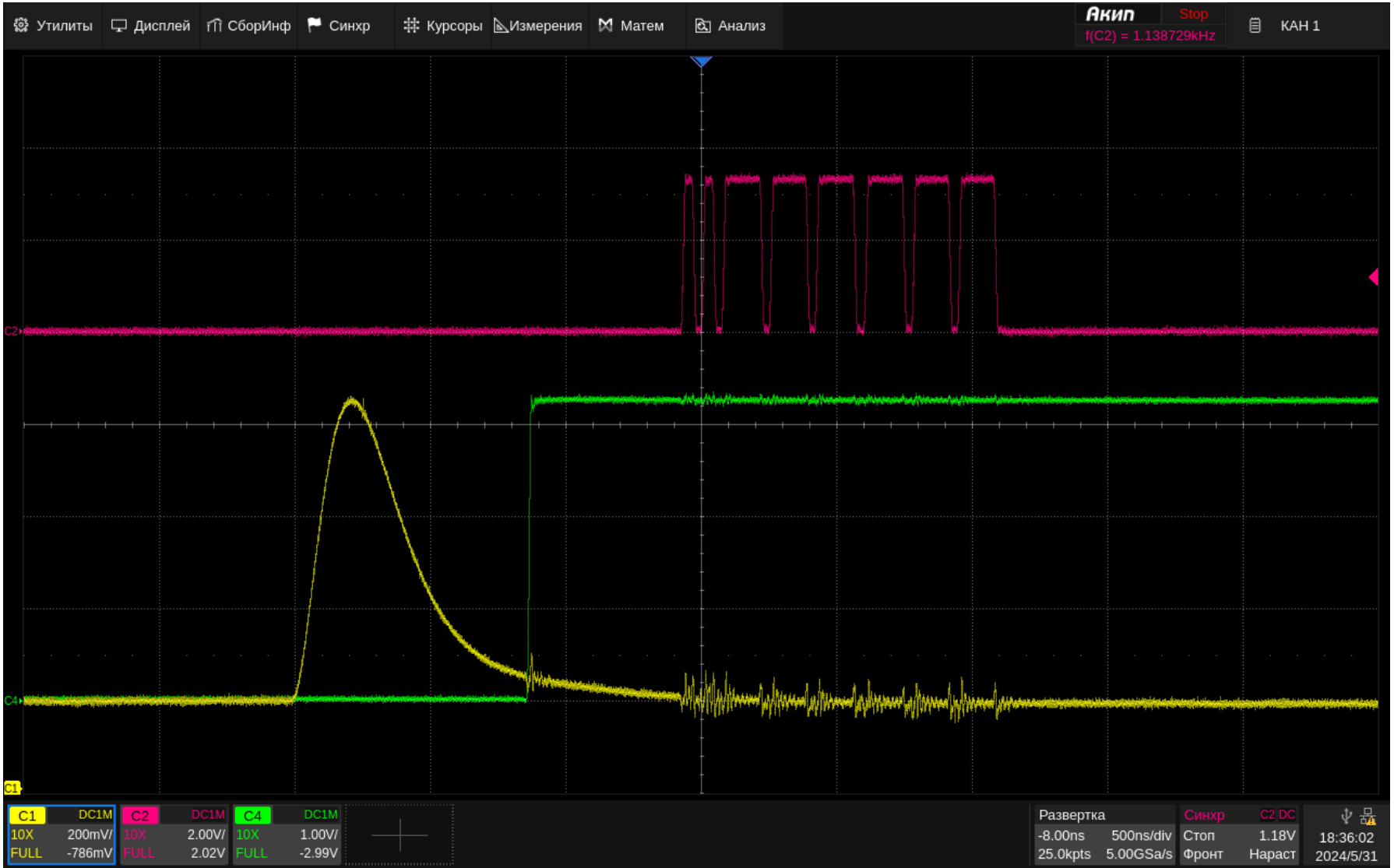
The board attached to a Straw Chamber



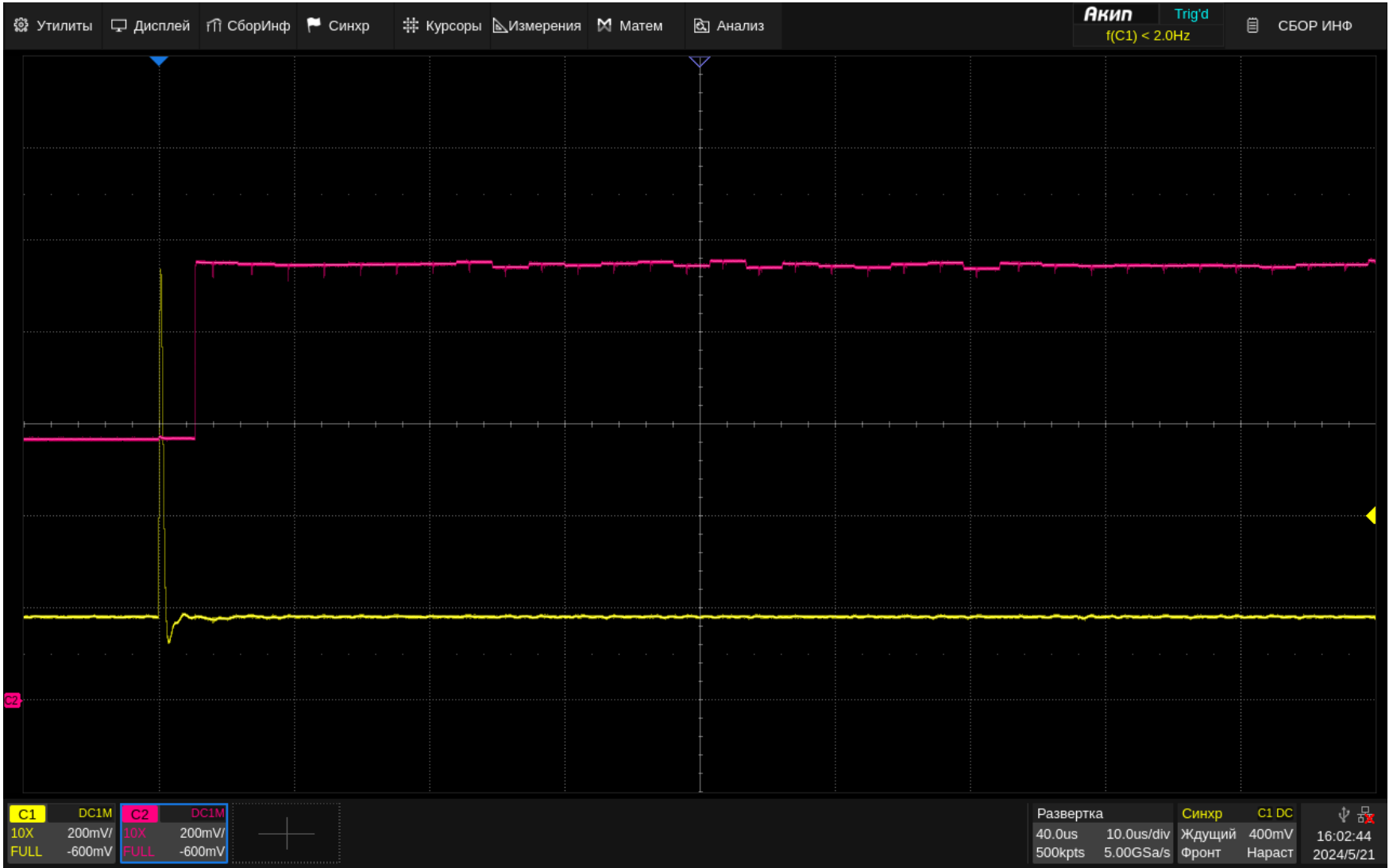
The board attached to a Straw Chamber



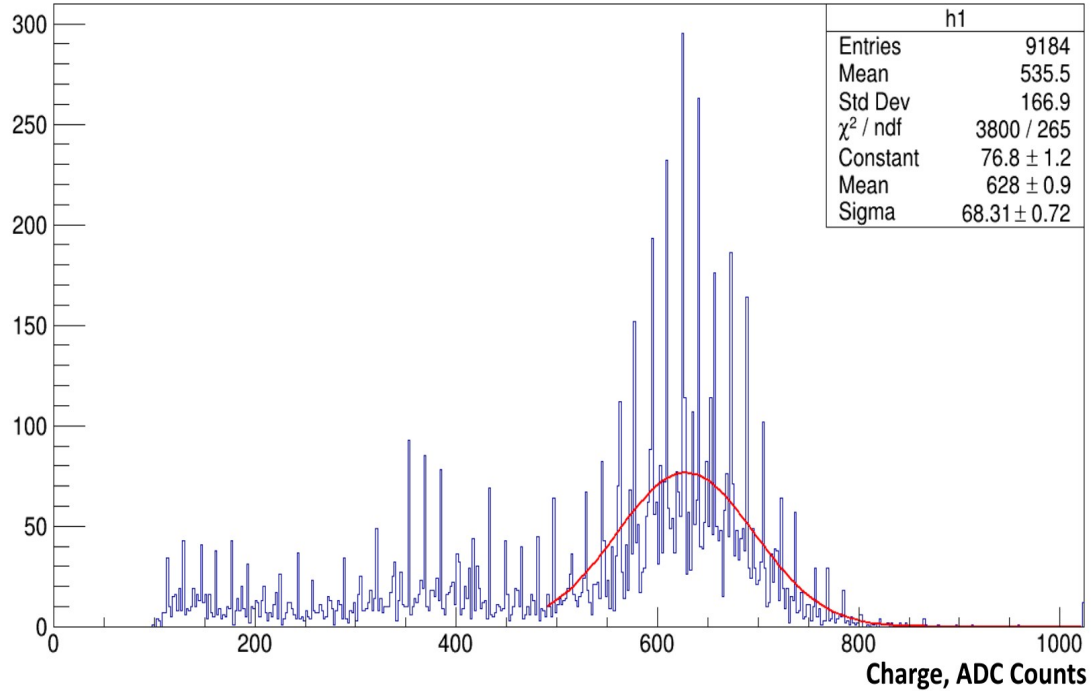
Readout of single event



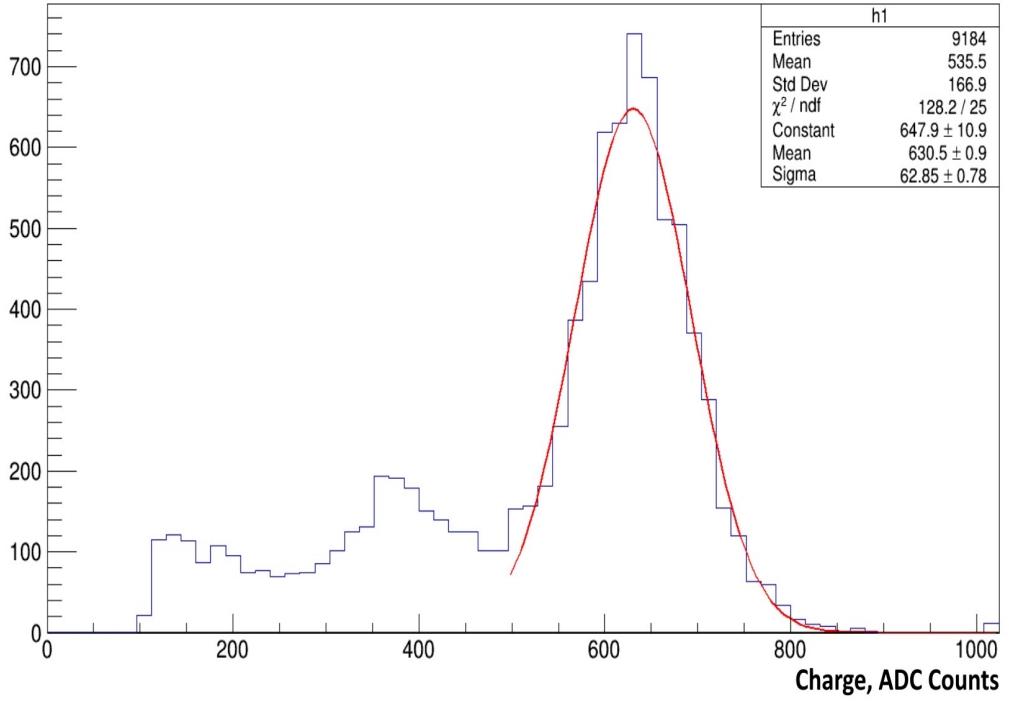
Readout of series of events



VMM3/3A has well known bad **ADC/TDC** perfomance in standard **Continuous Mode**

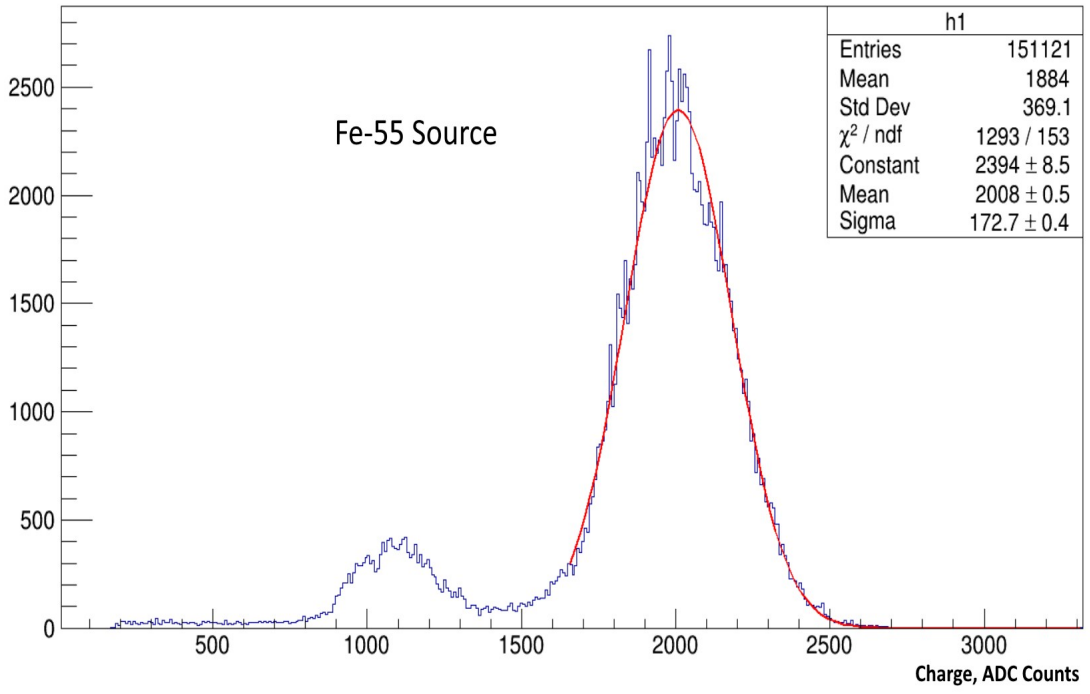


Fe55 Spectra, internal ADC

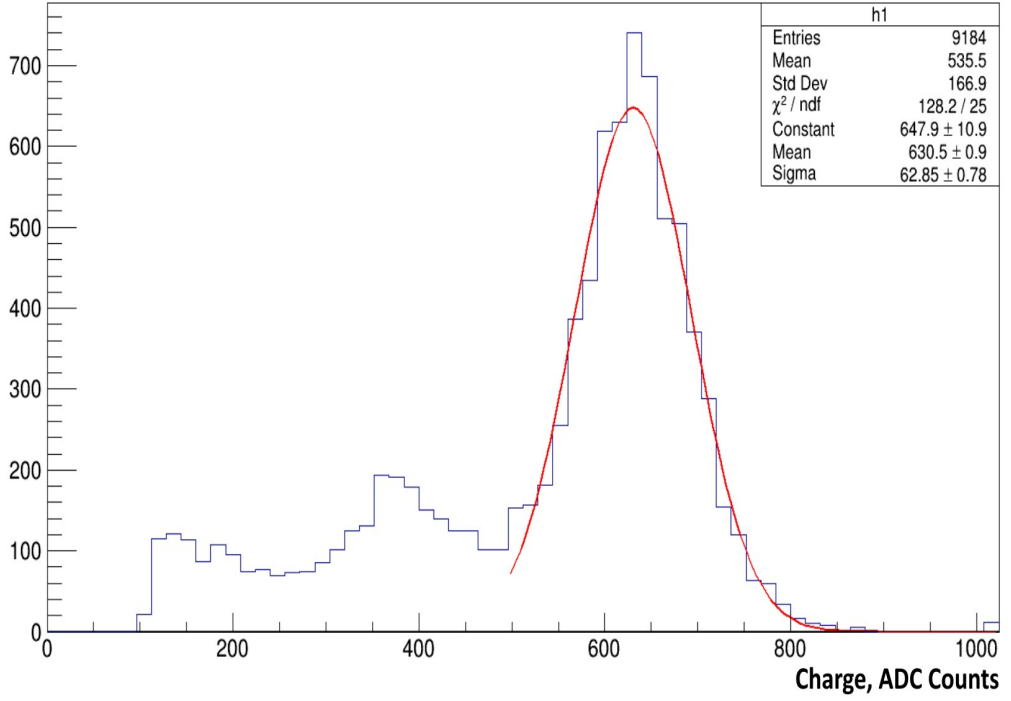


Fe55 Spectra, internal ADC
Hard rebin applied

VMM3/3A has well known bad **ADC/TDC** perfomance in standard **Continuous Mode**

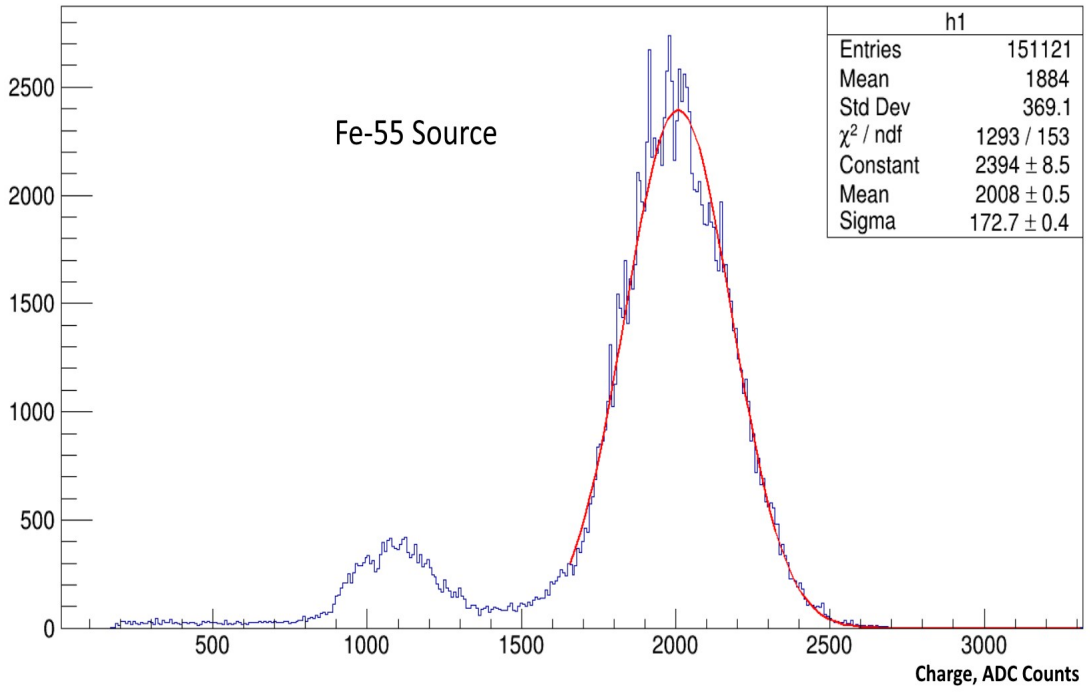


Fe55 Spectra, external ADC
Much better resolution

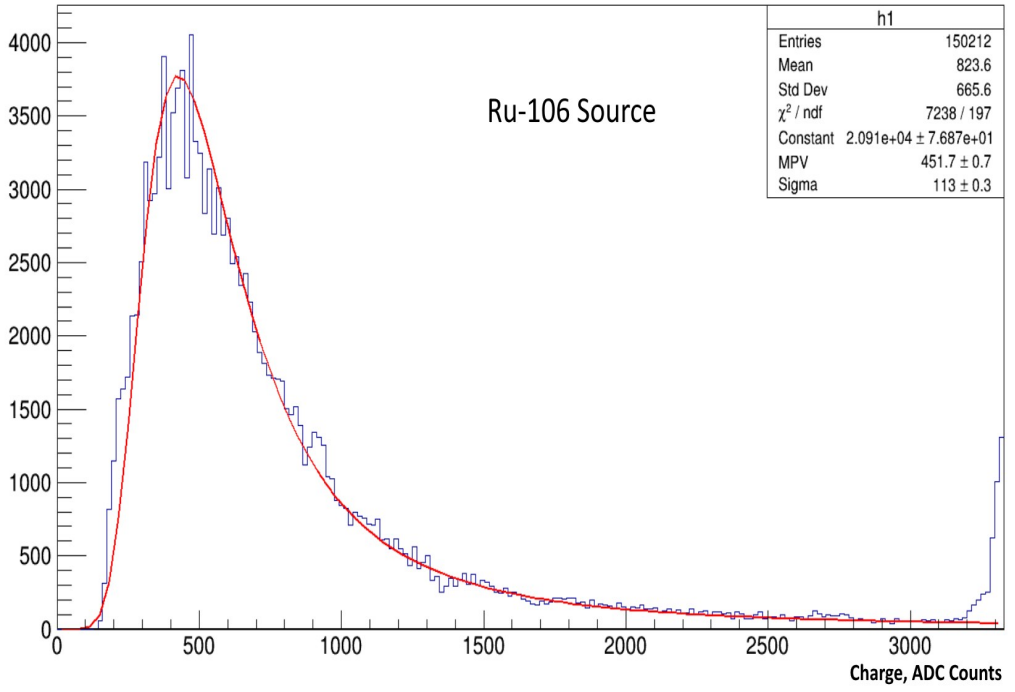


Fe55 Spectra, internal ADC
Hard rebin applied

VMM3/3A has well known bad **ADC/TDC** perfomance in standard **Continuous Mode**



Fe55 Spectra, external ADC
Much better resolution



Ru106 Spectra, external ADC
Much better resolution

Some current summary:

- «New» external ADC mode has been tested
- Much better ADC perfomance observed
- Still have some ADC issues, so new ADC is to be chosen
- Rate perfomance of the whole system to be tested
- Time resolution and PLL stability to be tested
- L1 interface logic to be implemented

Backlog

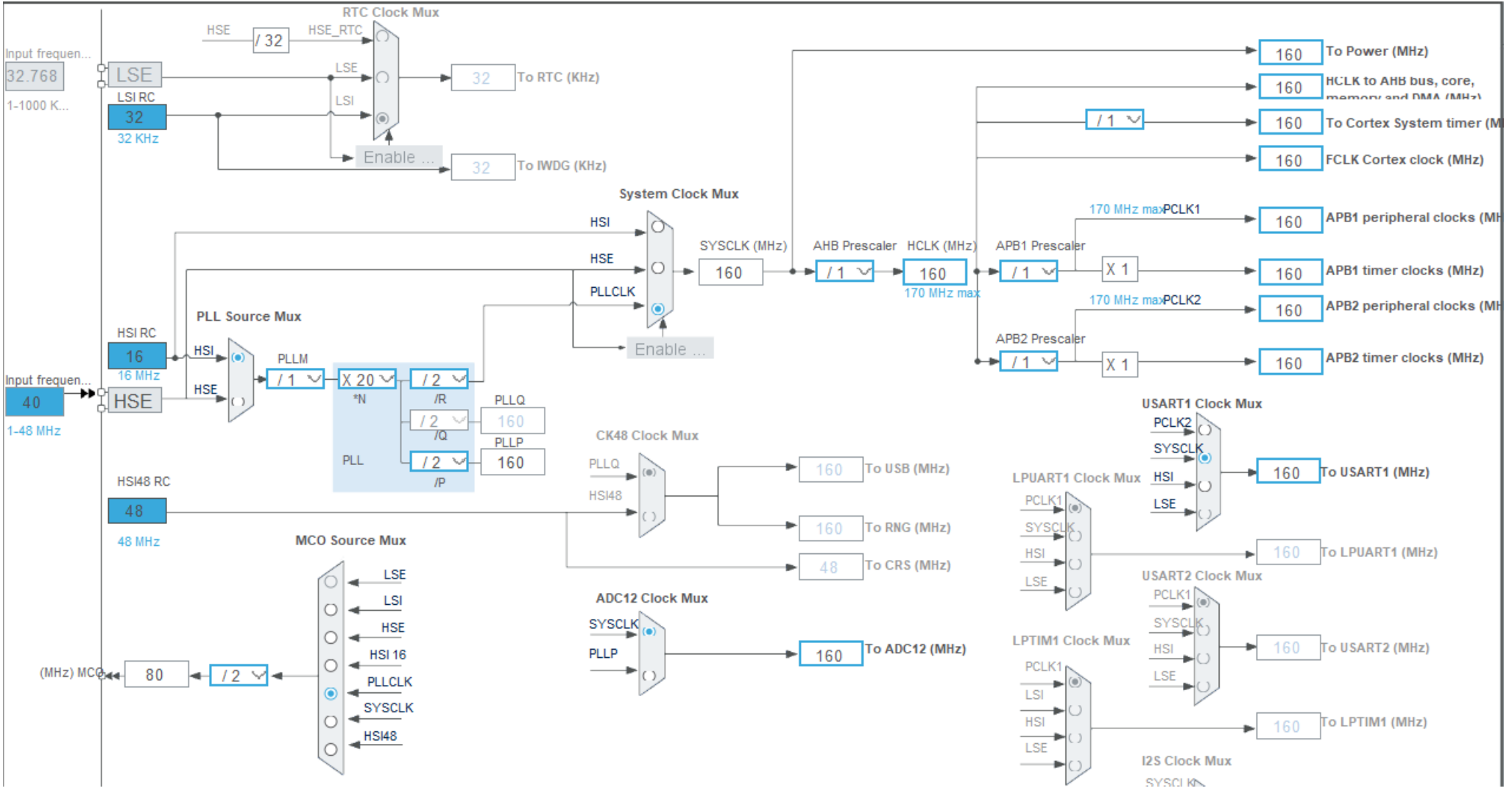

RTC Clock Mux
HSE
/ 32
HSE_RTC
LSE
LSI
32
To RTC (KHz)
Input frequen...
32.768
1-1000 K...
LSE
LSI RC
32
32 KHz
Enable ...
32
To IWDG (KHz)
System Clock Mux
HSI
HSE
PLLCLK
Enable ...
SYSCLK (MHz)
160
AHB Prescaler
/ 1
HCLK (MHz)
160
170 MHz max
160
To Power (MHz)
160
HCLK to AHB bus, core,
/ 1
160
To Cortex System timer (M
160
FCLK Cortex clock (MHz)
APB1 Prescaler
/ 1
X 1
170 MHz max
PCLK1
160
APB1 peripheral clocks (MH
160
APB1 timer clocks (MHz)
APB2 Prescaler
/ 1
X 1
170 MHz max
PCLK2
160
APB2 peripheral clocks (MH
160
APB2 timer clocks (MHz)
PLL Source Mux
HSI RC
16
16 MHz
HSI
HSE
PLLM
/ 1
X 20
*N
/ 2
/R
/ 2
/Q
/ 2
/P
PLL
PLLQ
160
PLLP
160
Input frequen...
40
1-48 MHz
HSE
CK48 Clock Mux
PLLQ
HSI48
160
To USB (MHz)
160
To RNG (MHz)
48
To CRS (MHz)
HSI48 RC
48
48 MHz
MCO Source Mux
LSE
LSI
HSE
HSI 16
PLLCLK
SYSCLK
HSI48
(MHz) MCO
80
/ 2
ADC12 Clock Mux
SYSCLK
PLLP
160
To ADC12 (MHz)
USART1 Clock Mux
PCLK2
SYSCLK
HSI
LSE
160
To USART1 (MHz)
LPUART1 Clock Mux
PCLK1
SYSCLK
HSI
LSE
160
To LPUART1 (MHz)
USART2 Clock Mux
PCLK1
SYSCLK
HSI
LSE
160
To USART2 (MHz)
LPTIM1 Clock Mux
PCLK1
LSI
HSI
LSE
160
To LPTIM1 (MHz)
I2S Clock Mux
SYSCLK

Table 1. ADC features on STM32G4 Series

Features	Values for STM32G4 Series
Number of ADCs	Up to 5
Resolution	12 bits (or 10, 8, 6 bits), 16 bits with oversampling
Number of input channels	Up to 42
ADC principle	Successive approximation register (SAR)
ADC clock frequency	Up to 60 MHz (up to 52 MHz in multiple-ADC operation case)
Sampling rate	Up to 4 Msps (up to 3.46 Msps in multiple-ADC operation case)
Sampling time	2.5 to 640.5 [ADC clock periods]
Supply voltage	V_{DDA} = 1.62 V to 3.6 V
Reference voltage	On dedicated VREF+ pin(1) (internal or external), V_{REF+} = 1.62 V to V_{DDA} (see datasheet)
Triggers	From external pins or internal peripherals (timers)
Conversion modes	Single, continuous, scan-selected channels, discontinuous mode
Others	Offset calibration, analog watchdog, hardware oversampling, offset compensation, gain compensation, interleaved mode (two ADCs coupled), sampling time controlled by trigger edges, bulb mode sampling

1. *In the LQFP128-pin packages, two VREF+ pins are available.*

Compare	Mfr Part #	Quantity Available	Price	Series	Package	Product Status	DigiKey Programmable	Core Processor	Core Size	Speed	Connectivity	Peripherals
☐	**STM32F030R8T6** Mainstream Arm Cortex-M0 Value l *STMicroelectronics*	**209,651** In Stock	1 : **$2.86000** Tray	STM32F0	Tray	Active	Not Verified	ARM® Cortex®-M0	32-Bit Single-Core	48MHz	I²C, SPI, UART/USART	DMA, POR, PWM, WDT
☐	**STM32G030K8T6** IC MCU 32BIT 64KB FLASH 32LQFP *STMicroelectronics*	**103,554** In Stock	1 : **$1.96000** Tray	STM32G0	Tray	Active	Not Verified	ARM® Cortex®-M0+	32-Bit Single-Core	64MHz	I²C, IrDA, LINbus, SPI, SmartCard, UART/USART	DMA, I²S, POR, PWM, WDT
☐	**STM32G030F6P6** IC MCU 32BIT 32KB FLASH 20TSSOP *STMicroelectronics*	**94,495** In Stock	1 : **$1.61000** Tray	STM32G0	Tray	Active	Not Verified	ARM® Cortex®-M0+	32-Bit Single-Core	64MHz	I²C, IrDA, LINbus, SPI, SmartCard, UART/USART	DMA, I²S, POR, PWM, WDT
☐	**STM32G474CBT6** Mainstream Arm Cortex-M4 MCU 170 *STMicroelectronics*	**0** In Stock **82,500** Marketplace	1,500 : **$4.13999** Tray 1,500 : **$3.15000** Tray	STM32G4	Tray Tray	Active	Not Verified	ARM® Cortex®-M4F	32-Bit Single-Core	170MHz	CANbus, I²C, IrDA, LINbus, QSPI, SPI, UART/USART	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
☐	**STM32L071CZT6TR** IC MCU 32BIT 192KB FLASH 48LQFP *STMicroelectronics*	**78,580** In Stock	1 : **$5.34000** Cut Tape (CT) 2,400 : **$2.67868** Tape & Reel (TR)	STM32L0	Tape & Reel (TR) Cut Tape (CT) Digi-Reel®	Active	Not Verified	ARM® Cortex®-M0+	32-Bit Single-Core	32MHz	I²C, IrDA, SPI, UART/USART	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
☐	**STM32G031K8U6** IC MCU 32BIT 64KB FLASH 32UFQFPN *STMicroelectronics*	**66,389** In Stock	1 : **$2.86000** Tray	STM32G0	Tray	Active	Not Verified	ARM® Cortex®-M0+	32-Bit Single-Core	64MHz	I²C, IrDA, LINbus, SPI, SmartCard, UART/USART	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
☐	**STM32L071CZY6TR** IC MCU 32BIT 192KB FLASH 49WLCSP	**57,017** In Stock	1 : **$5.23000** Cut Tape (CT) 5,000 : **$2.52755**	STM32L0	Tape & Reel (TR) Cut Tape (CT)	Active	Not Verified	ARM® Cortex®-M0+	32-Bit Single-	32MHz	I²C, IrDA, SPI, UART/USART	Brown-out Detect/Reset,