Seminar on the Chinese-Russian Cooperation within the NICA MPD-ITS Project Meeting on 23/07/2024

Participants:

- Andreev Denis (JINR),
- Arteche Dias Raul (JINR),
- Babkin Vadim (JINR),
- Belov Oleg(JINR),
- Ceballos Sanchez Cesar (JINR),
- Dementiev Dmitry (JINR),
- Di Guo, remotely (USTC),
- Gaganova Maria (JINR),
- Herrera Barrera Maribel (JINR),
- Jiajun Qin (USTC),
- Kolozhvari Anatoly (JINR),
- Kondratiev Valery (SPbSU),
- Le Xiao (CCNU),
- Leontiev Vladimir (JINR),
- Murin Yuri (JINR),
- Peres Miranda Margarita (JINR),
- Peshekhonov Dmitry (JINR),
- Reyes Penya Solne (JINR),
- Rodriguez Alvares Alejandro (JINR),
- Rufanov Igor (JINR),
- Sheremetev Aleksei (JINR),
- Shitenkov Mikhail. (JINR),
- Tsapulina Ekaterina(JINR),
- Vereschagin Stepan (JINR),
- Voronin Aleksey (JINR),
- Xiangming Sun (CCNU),
- Yaping Wang (CCNU),
- Zamiatin Nikolay (JINR).

Meeting minutes:

- **Topics discussed**,
- Decisions made / Next steps defined,

- **Welcome words** (presenter: Dr. Dmitry Peshekhonov):
  Welcome words for the involved parties together with the importance of China-Russia collaboration were raised and announced as the starting point of the seminar.

- **Six layers MPD ITS performance for D meson identification** (presenter: Prof. Valery Kondratiev):

  Physical motivation in using the MAPS based MPD-ITS in combination with TPC that makes it possible to detect short-lived products of Au-Au interactions with maximum efficiency due to the best spatial resolution, high counting-rate and high level of pixel segmentation, was described.

  Quality assessment of the MPD tracking system (TPC + ITS-6-40) has been investigated when reconstructing charmed particles formed in Au-Au collisions at NICA energies. Simulation shows also the feasibility of D mesons reconstruction in central Bi+Bi collisions at $\sqrt{S_{NN}}$ = 11 GeV. Estimated meson yields opens up prospects for studying the heavy flavors physics at the NICA-MPD facility.

- **MPD ITS mechanics, cooling and communications** (presenter: Dr. Yurii Murin):

  The status of the main areas of works for ITS mechanics which are: Installation Container, communications and cooling plant was presented in the report.

  - Installation Container (IC).

    The importance of the Installation Container to integrate the ITS into TPC addressing the narrow and long sizes of the ITS was described. Solution for the Installation Container (IC) proposed by Sergei Igolkin (SPbSU), further adapted and finalized by Denis Andreev et al. (JINR) was presented.

    The current status of the IC production was shown on real parts at JINR assembly room. It is planned to complete the IC full assembly by the end of 2024 year.

  - Communication structure.

    Communications structure, namely the power cables for installation of 42 OB staves (two layers) was presented and described. Handmade data cables produced at VB LHEP, ready for serial production were developed as a result of this work.

  - Cooling plant.

    The scheme for the Cooling Plant for leak-less water cooling of the ITS being produced for JINR by DSSE was presented. Delivery of the instrumentation and control equipment together with installation materials is planned in October 2024, production and tests are planned for January 2025.

- **The research and development of MICA chip** (presenter: Dr. Le Xiao):

  The key milestones of the MICA chip development were presented and discussed, namely the advantages of MAPS technology, the R&D steps performed, the current status of the MICA chip prototype production.

  - Advantages of MAPS technology:

    The advantages on the MAPS technology, mainly integration of sensors and readout circuits on the same chip, low material budget, low cost and low power consumption achieved due to low input capacitance, were described during the presentation.

  - R&D steps performed:

    The CMOS 130 nm Bulk Silicon process suitable for MAPS in cooperation with the foundry was developed in China. Based on this CMOS process, a pixel test chip and evaluation system were developed. The high resistance substrate and negative bias effect were

found to be significant on this process using the ^{90}Sr source to test the pixel chip.

- Current status of MICA chip production:
  A fully functional MAPS MICA chip was designed based on this process and one MICA wafer was already received from the foundry. The test system for the MICA chip is ready. Submodule functional testing is planned to be started in the near future. There might be some changes to the MICA chip identified during testing which will result in changes in the MICA chip prototype design. One of the specific tests to be performed and analyzed is ability to assemble the module due to the changes in the MICA chip pinout design in comparison to the ALPIDE chip.

- **Roundtable discussion**:
  The major issue to be investigated is the impact of the changes in the MICA chip design in comparison to the ALPIDE chips to understand the module assembly ability as well as the functioning of the chips, especially regarding the implementation of the surface bonding pads.

- **Readout electronics design for ITS of MPD at NICA** (presenter: Dr. Jiajun Qin):
  The key milestones for the Readout Electronics for the MPD-ITS Outer Barrel were presented and discussed, mainly the Readout Unit (RU) system scale and R&D status, Power Unit (PU) system scale and R&D status of the NICA_ROC ASIC. The major challenges for readout electronics design are the high-speed data transmission and real-time pre-processing and high reliability in radioactive environments.

  - Readout Unit (RU) system scale and R&D status:
    42 RU modules, each controls/reads out 196 MAPS chips. Design and testing of the FPGA-based RU version 1 was completed. The hardware design of RU version 2 is complete and ready for testing.

  - Power Unit (PU) system scale and R&D status:
    42 Power Boards (each consists of two independent PUs (PUR and PUL).
    Prototype of the PB was produced and successfully tested. All mechanical parts (cooling plate, front panel) were fabricated. There was a voltage drop in power cable defined during testing that cannot be ignored. The voltage compensation algorithm was proposed and confirmed to be capable of addressing the issue of voltage drop loss across power cable.

  - R&D status of the NICA_ROC ASIC
    The main functions of the chips are to readout and control the MAPS chips, replacing the function of FPGA. NICA_GBT acts as assembler, buffer, aggregator, and data packet processor for the pixel detectors, while the NICA_ROC essentially optimizes the bandwidth utilization and reduces the number of required data links. At present two versions (NICA ROC_V0 ASIC, NICA ROC_V1 ASIC) of the chip were completed.

- **GBT-like series ASICs development** (presenter: Dr. Di Guo):
  The background of GBT-Series ASICs was presented. The current status of the NICA-GBT ASIC and NICA_LD/NICA_TIA/Optical module developments were reported:

- NICA-GBT ASIC development:
  Functions of High-speed Serializer, High-speed Deserializer, PLL, CDR and High-speed Tx/Rx were completed. The digital part (Encode, Decode functions), Clock Phase control functions are under design, Data Phase Control (Phase Aligner) function was designed and under testing now.

- NICA_LD/NICA_TIA/Optical module developments:
  NICA_LD, NICA_TIA core design was completed and tested. As part of works for next year (2025) it is planned to optimize the design and the final version integration (for the NICA_LD). The prototype for the optical module was design and tested which is planned to be further optimized to prepare the final version.

- **JINR options for the in-beam tests of MICA chips, MICA HICs and their readout**:

Nuclotron@JINR and SC-1000@PNPI were proposed to be used for the tests of MICA ASICs, HICs and readout electronic. Beam telescope with the full chain of ALPIDE readout and dedicated software was developed by JINR team and successfully tested at SC-1000 in 2024. Same mechanics and DAQ system could be used for the future tests of the MICA chips. In addition, light projectile fragments were proposed for the in-beam tests of MICA prototypes at BM@N area with the help of the fragment tagging hodoscope currently under construction at LHEP.

- **Modules and supermodules assembly readiness at CCNU and JINR** (presenters: Dr. Yaping Wang, Aleksei Sheremetiev):
  The MAPS-based ITS detector is planned to be constructed for the MPD experiment with the use of joint collaboration efforts from CCNU, USTC (China) and JINR (Russia).
  - Two construction sites for the ITS OB HIC/stave module assembly are being prepared at CCNU/Wuhan and JINR/Dubna respectively, and the infrastructure is under construction as planned.
  - The Chinese side should carry-out part of the HIC module and stave supermodule production for
    the MPD ITS. Assembly site readiness is as follows:
    - ITS2 OB HIC module production line is ready.
    - ITS2 supermodule (“stave”) production line is under construction.
    - Equipment for the module quality assurance testing is ready.
  - The JINR assembly site should carry-out part of the HIC module and stave production. The site readiness is as follows:
    - Infrastructure for assembly HICs will be ready for production provided the gripper of ALICIA 8 will be replaced.
    - Test bench of Electrical test for HIC are scheduled to be ready.
    - Technical staff trained in HIC assembly stages.
    - Benches of QA test for carbon part of STAVE has been ready.
    - Sets of jigs for the HIC and STAVE production on storage.
    - Infrastructure for assembly STAVE not yet ready due to delays of assigning the production area. Measures for remedy engaged.