The Research and Development of MICA Chip

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Contents

- Monolithic Active Pixel Sensor
- A 130 nm Bulk Silicon Process in China
- Pixel Test Chip and Process Evaluation
- MICA Chip and Test System
- Summary

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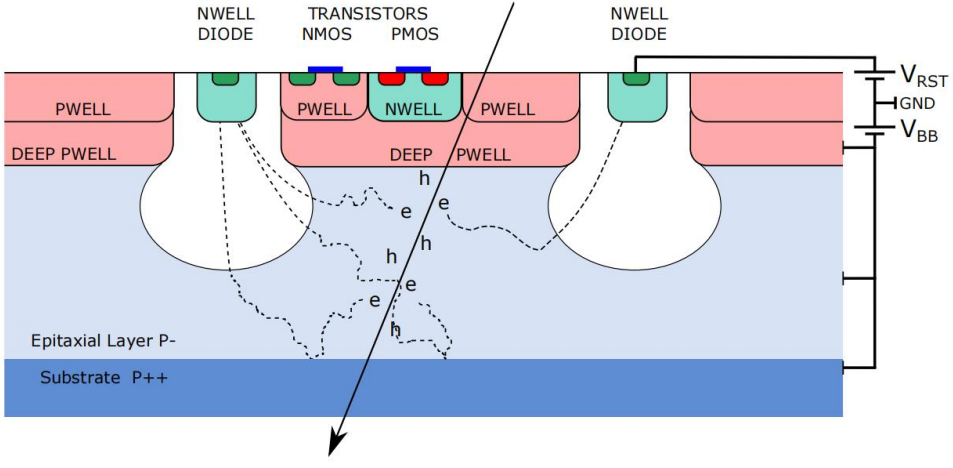
Monolithic Active Pixel Sensor



Cross section of a MAPS

Advantages of MAPS:

1. It integrates sensors and readout circuits on the same chip;
2. It has low material buget
3. It has low cost
4. Low input capacitance ->It can achieve low power consumption

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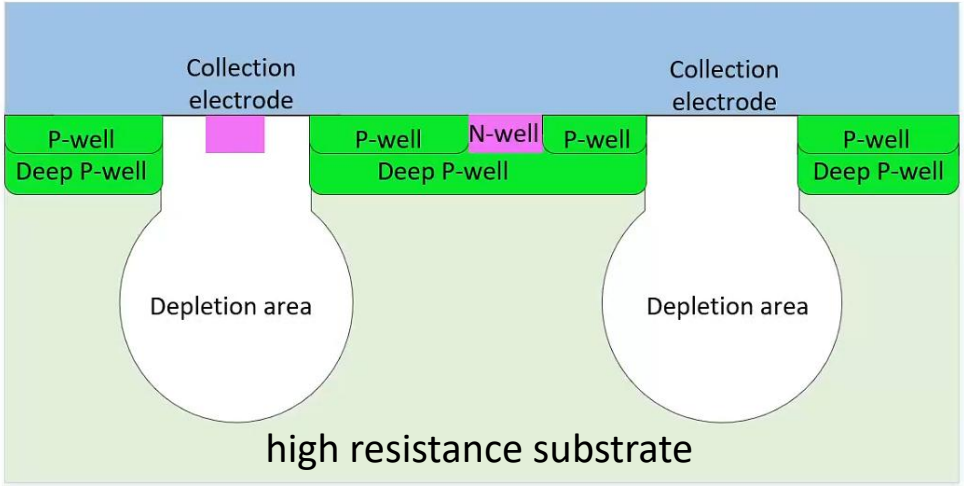
A 130 nm Bulk Silicon Process in China



Cross section of the process

130 nm bulk silicon process:

- We developed DPW together with the process factory
  (NW, PW, DNW) -> (NW, PW, DNW, DPW)
- It supports 6 layers of metal
- It supports high resistance substrate

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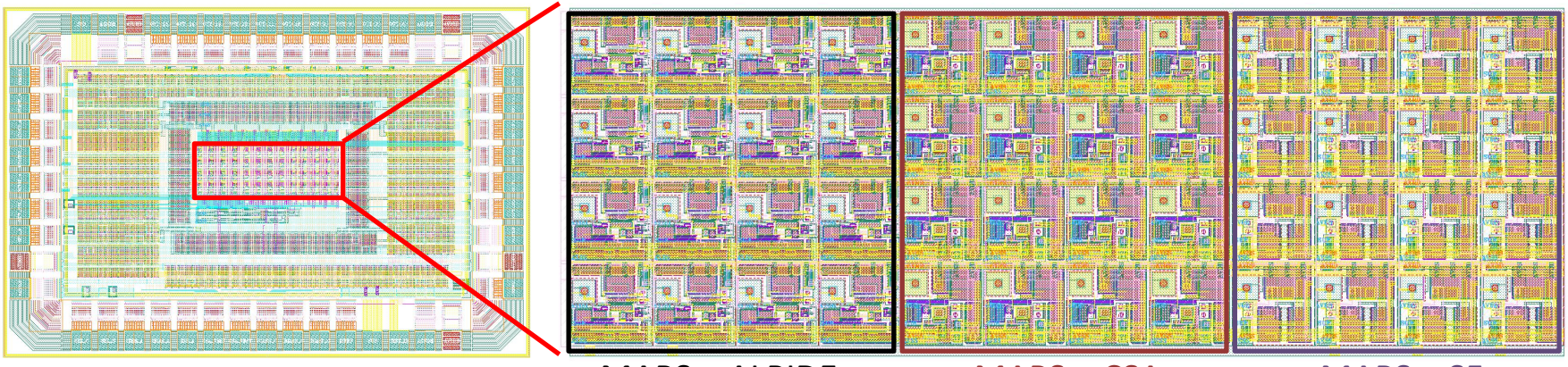
Pixel Test Chip and Process Evaluation

Pixel Test Chip Design



MAPS + ALPIDE | MAPS + CSA | MAPS + SF

Pixel Structure：
- MAPS + ALPIDE
- MAPS + CSA
- MAPS + SF

Array Size：（4 × 4）× 3

Chip Size：1.8mm × 1.2mm

- Sensor: Diode
- ENC < 8e-
- FE Power: 40nA * 3.3V
- Threshold < 1ke-
- Integration Period < 10us
- Pixel pitch: 40um

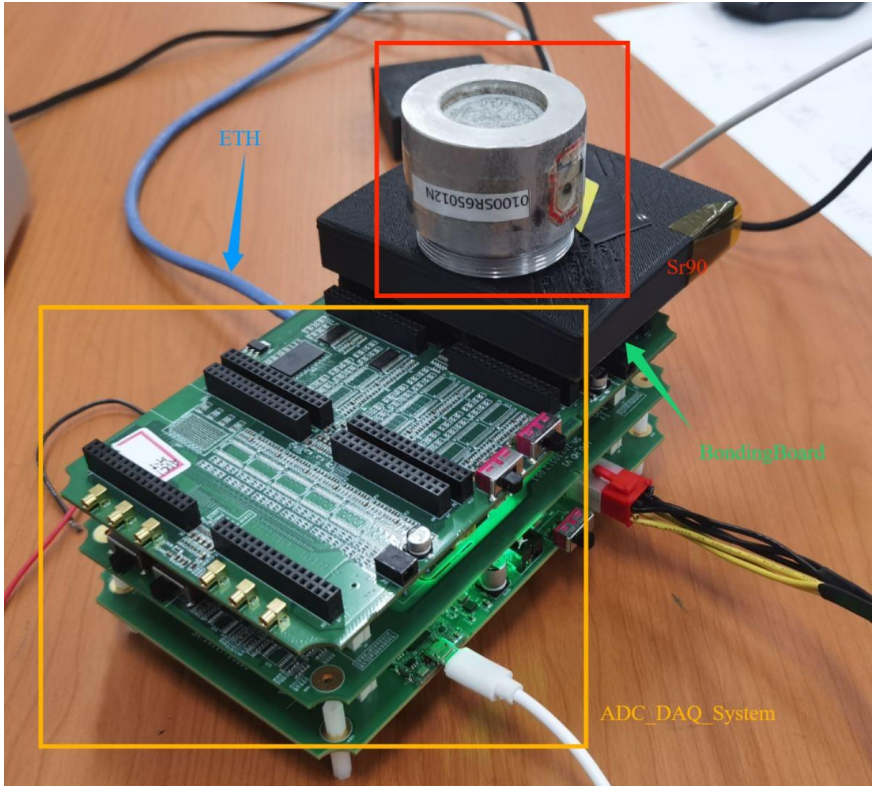
- Sensor: Diode
- ENC < 50e-
- CSA_Av ~ 80mV/ke-
- PeakingTime < 10us
- FE Power: 300nA × 3.3V
- Pixel pitch: 40um

- Sensor: Diode
- Pixel pitch: 40um
- SFP BIAS: 1uA

- We developed a pixel test chip based on the 130 nm bulk silicon process.
- It has three different pixel structures.
- Each pixel structure has a 4x4 matrix.

Pixel Test Chip and Process Evaluation

Test System for Process Evaluation

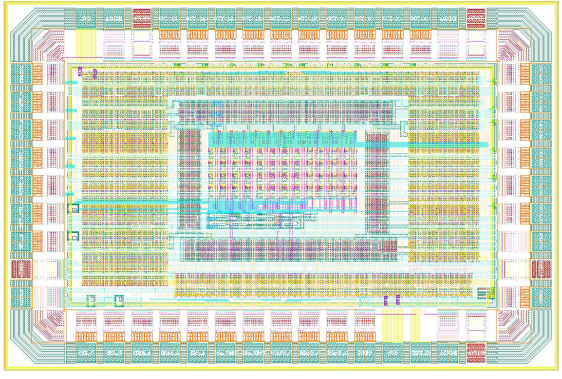


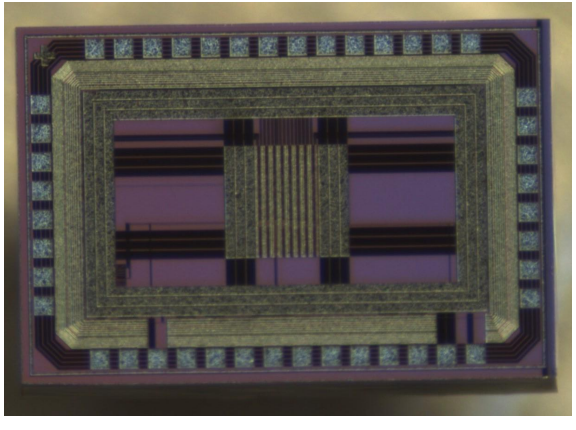
System Features:

- It has 16 channels ADC (sampling rate of 20MHz, 12 bits).
- It can provide 8 channels of analog voltage through DAC.
- It achieves data transmission and control through Gigabit Ethernet.
- It implements trigger in the firmware to reduce data.
- It has DDR3 cache (256M).

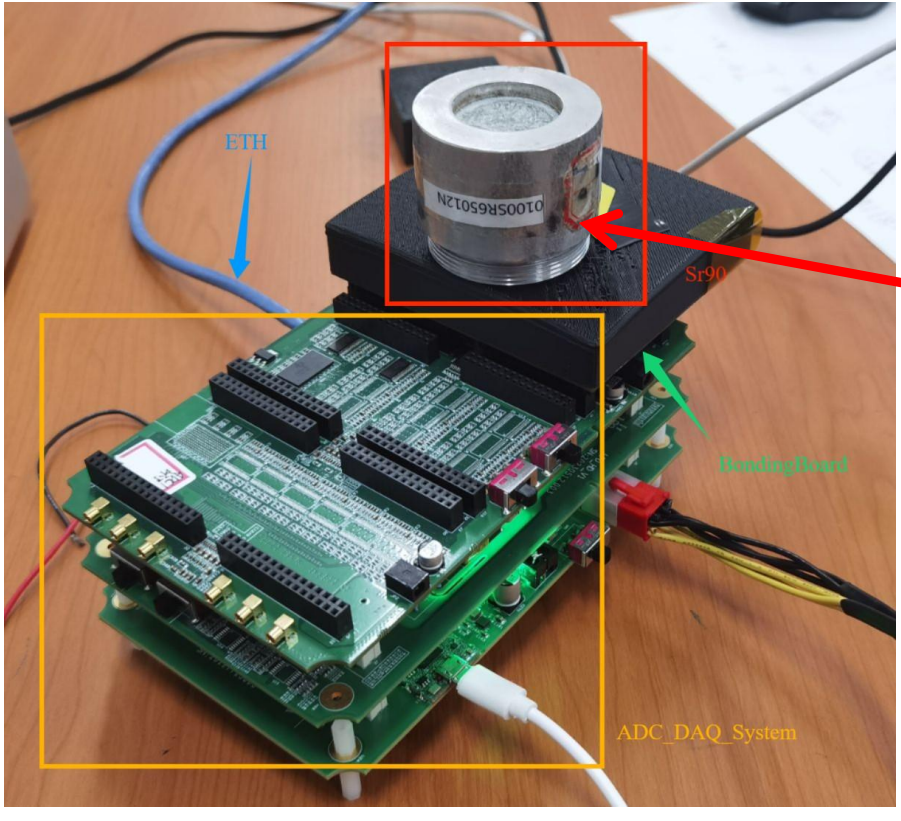
Pixel Test Chip and Process Evaluation

^{90}Sr Test





Layout and picture of the Pixel test chip

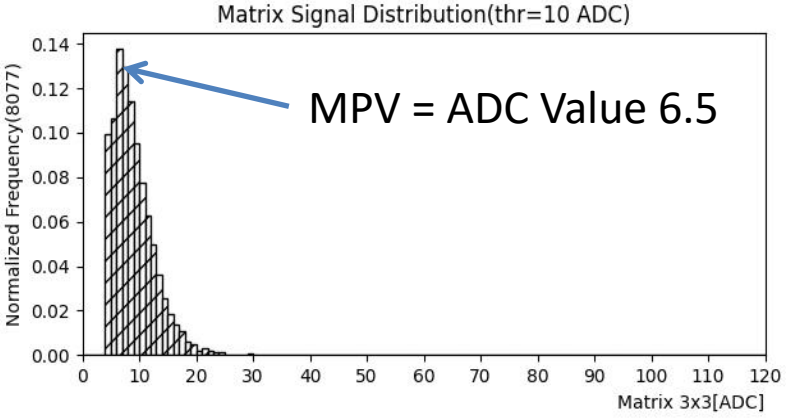


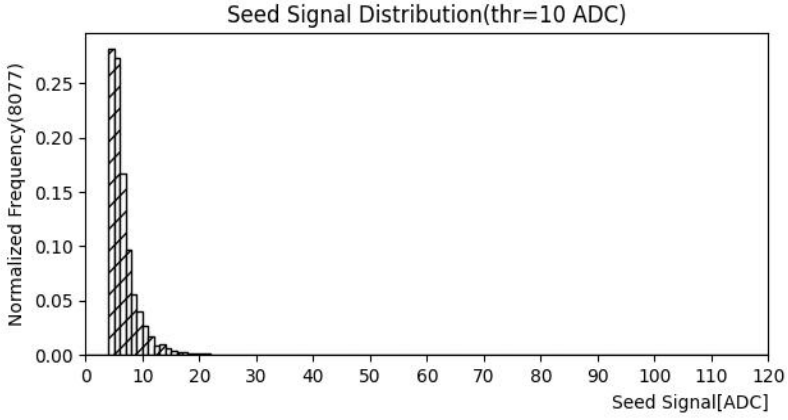
^{90}Sr

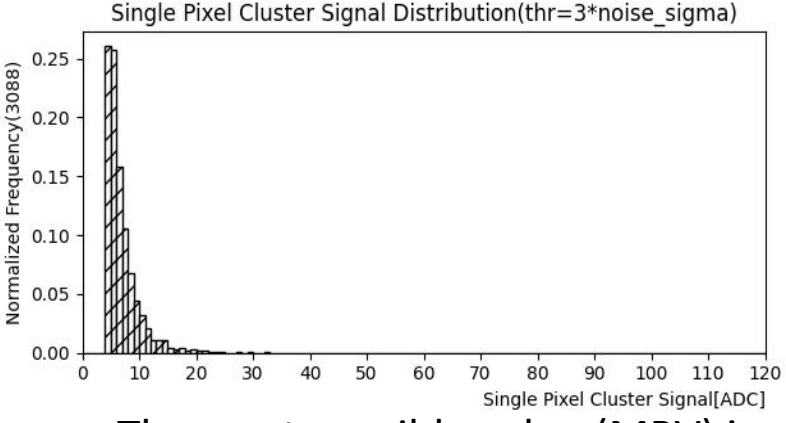
Test System

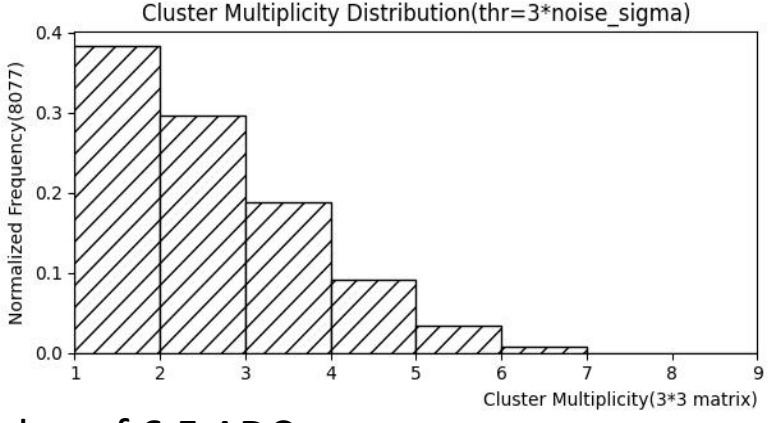
Pixel Test Chip and Process Evaluation

^{90}Sr Test (Low Resistance Substrate Chip)





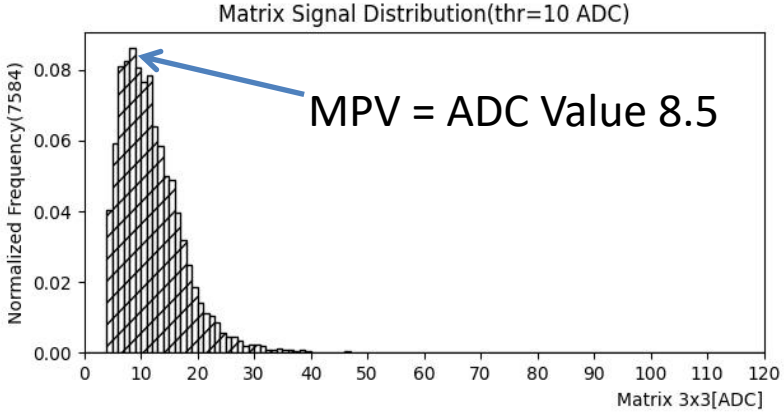


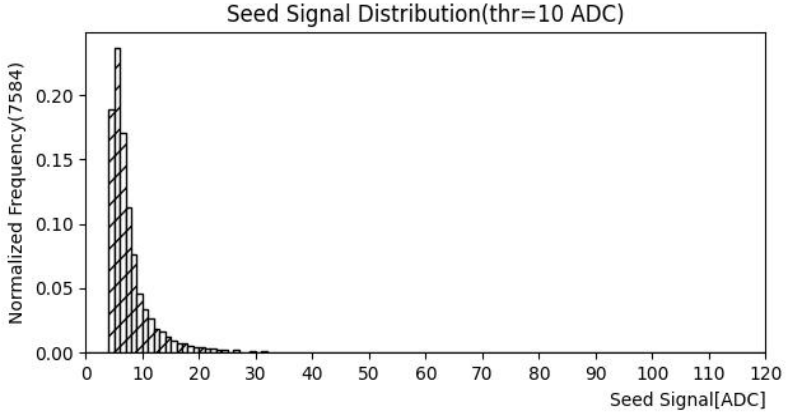


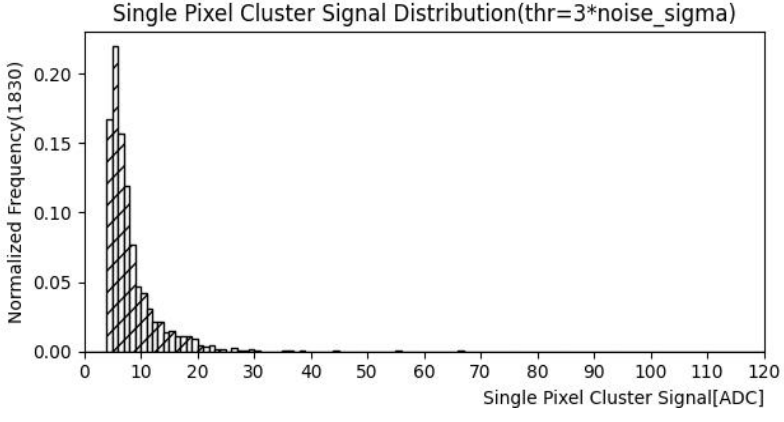
- The most possible value (MPV) is a value of 6.5 ADCs
- The event rate is 840 per hour.

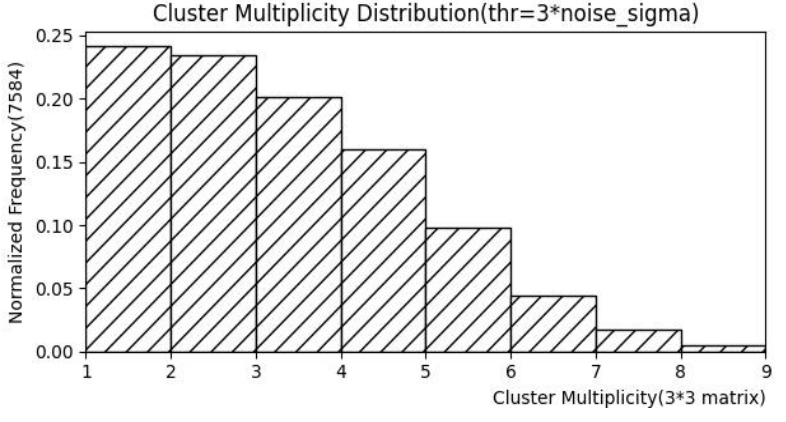
Pixel Test Chip and Process Evaluation

^{90}Sr Test (High Resistance Substrate Chip, 0V Bias)





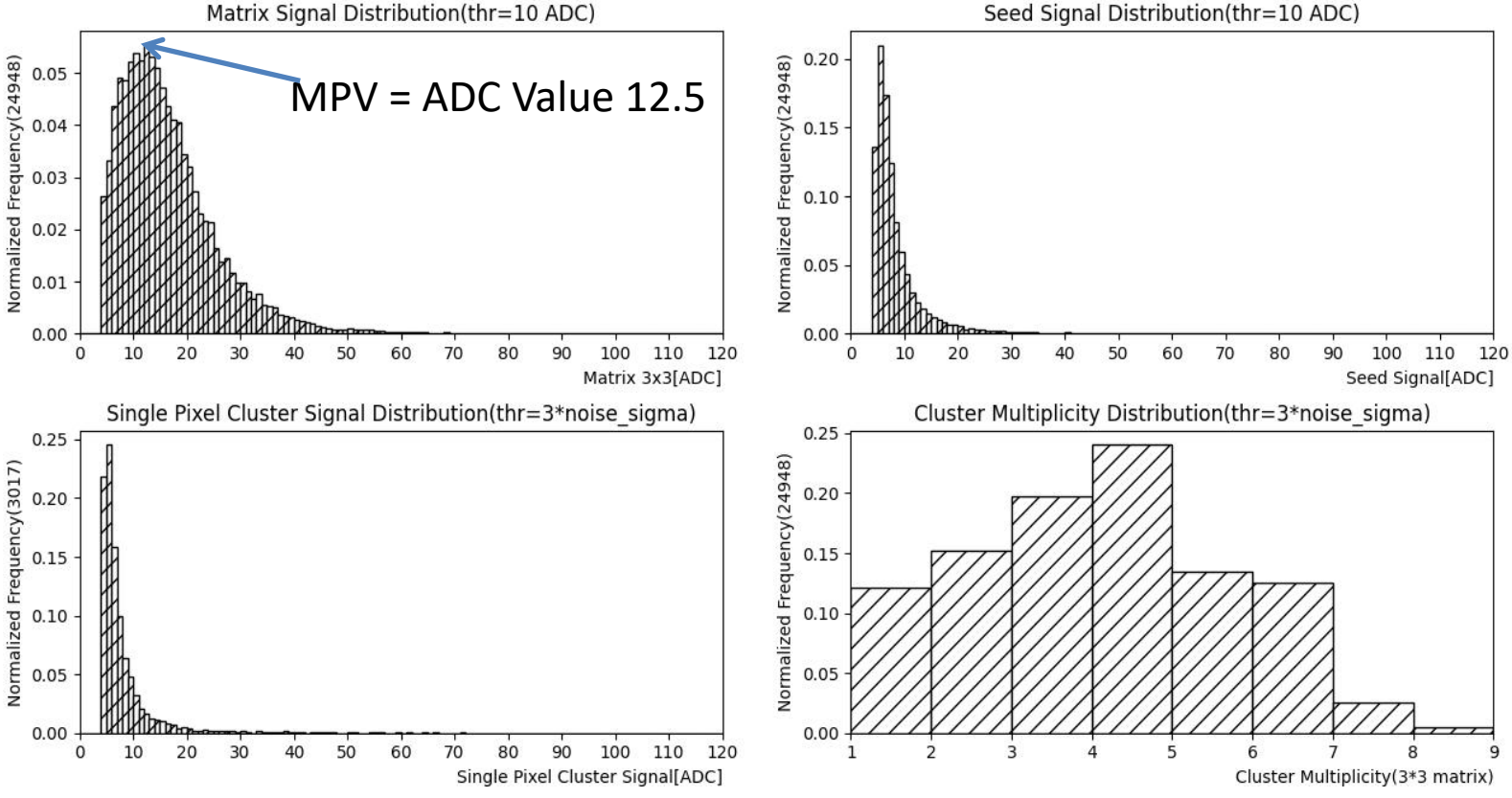




- The most possible value (MPV) is a value of 8.5 ADCs
- The event rate is 2760 per hour.

Pixel Test Chip and Process Evaluation

^{90}Sr Test (High Resistance Substrate Chip, -9V Bias)



- The most possible value (MPV) is a value of 12.5 ADCs
- The event rate is 11700 per hour.

Pixel Test Chip and Process Evaluation

^{90}Sr Test

^{90}Sr test	• Low Resistance Substrate • 0V Bias	• High Resistance Substrate • 0V Bias	• High Resistance Substrate • -9V Bias
MPV (ADC Value)	6.5	8.5	12
Event Rate (per hour)	840	2760	11700
Pixel Size	40u x 40u		

- The effect of high resistance substrate and negative bias is very obvious
- both for MPV and event rate.

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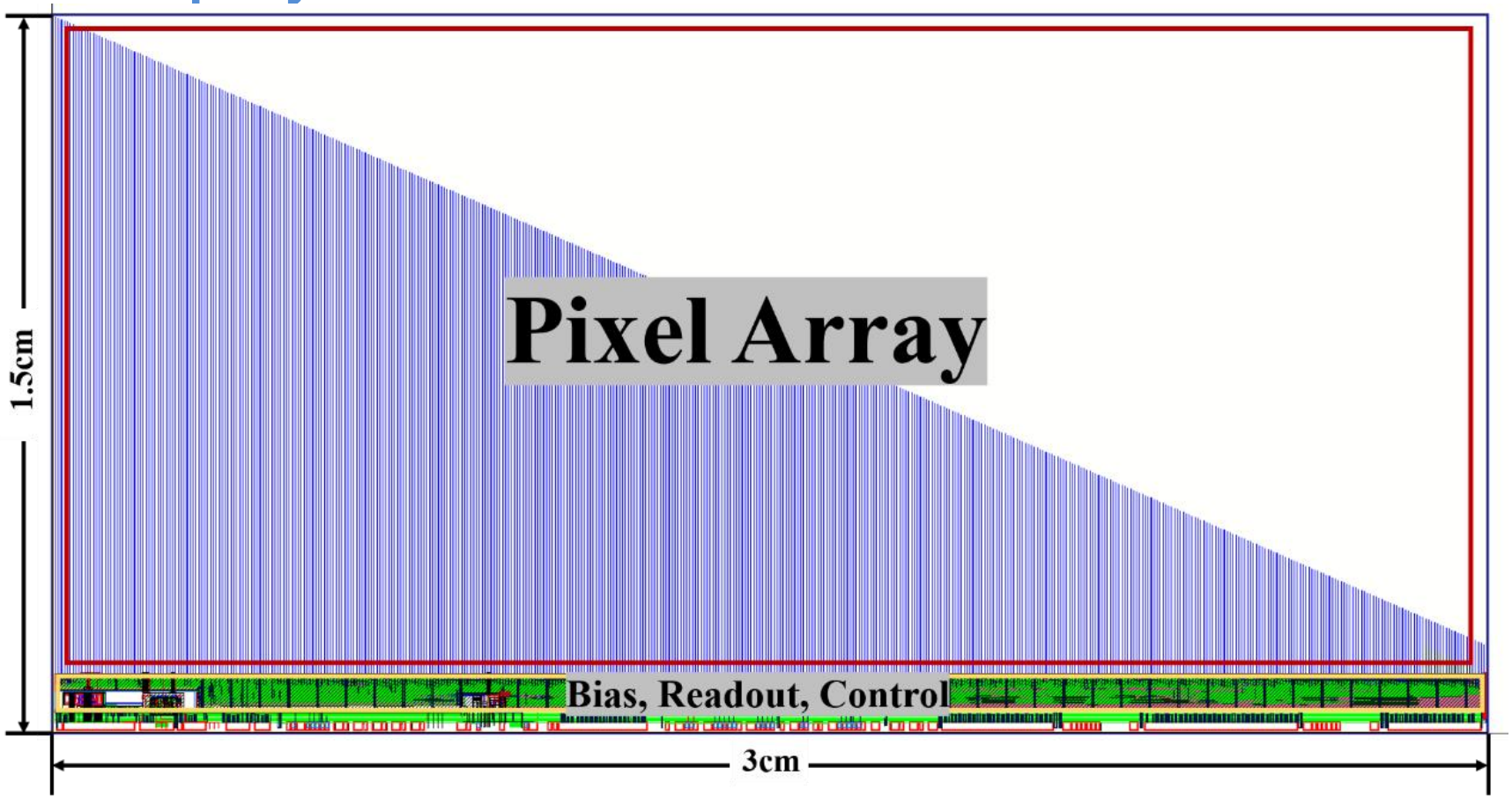
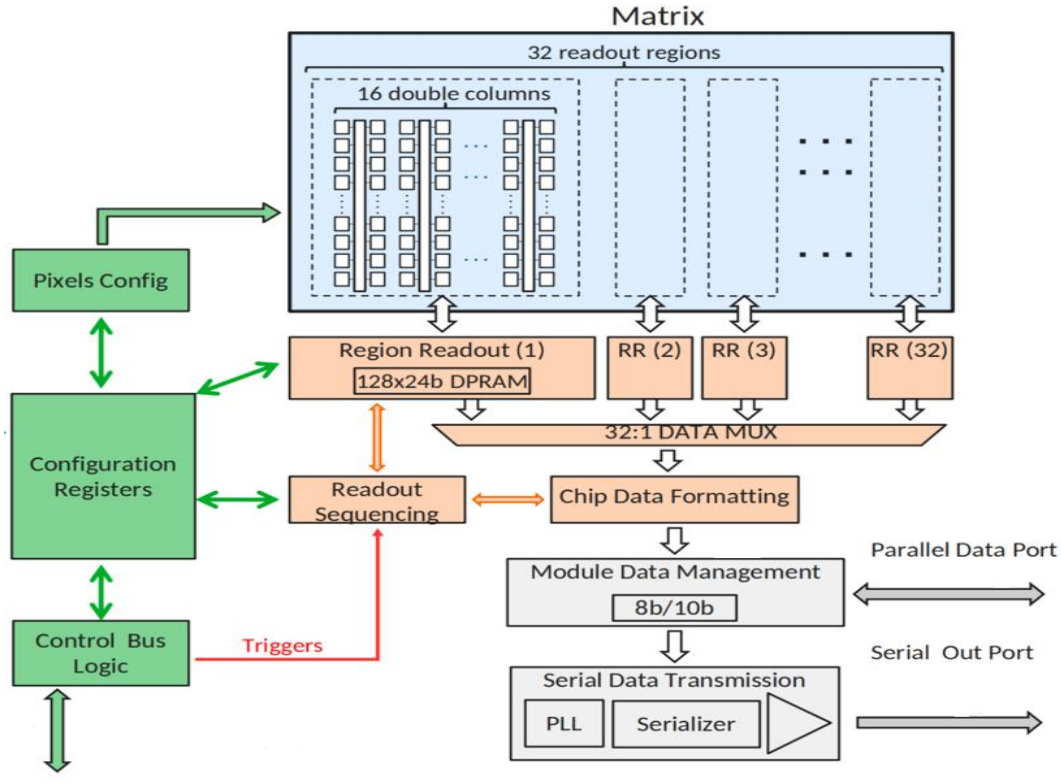
MICA Chip and Test System

MICA Chip Layout



MICA Chip and Test System

MICA Chip

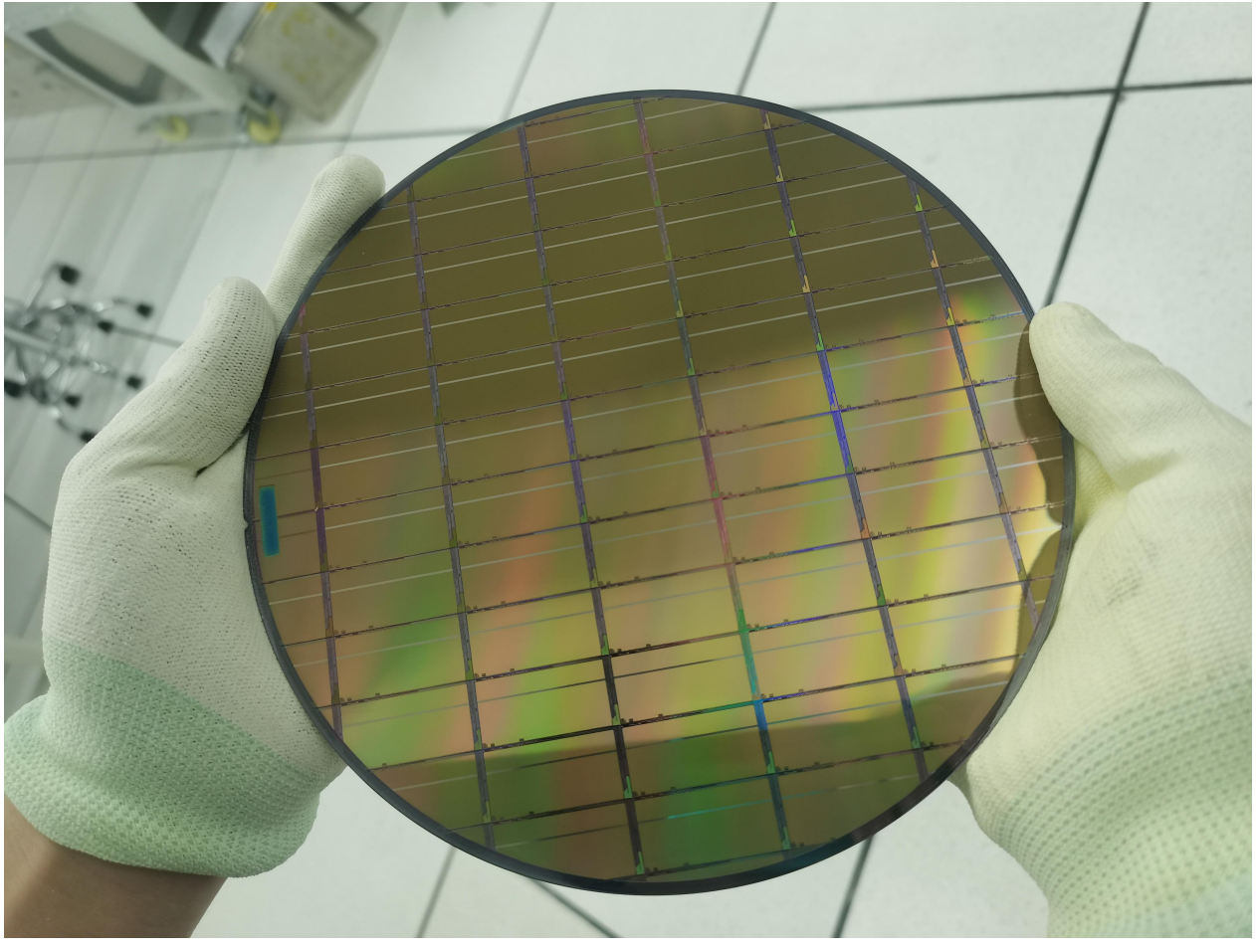


MICA chip block diagram

- The 130 nm bulk silicon process
- Chip Size: 15 mm × 30 mm
- Pixel Matrix: 512 × 1024
- Pixel Size: 30.53 μm × 26.8 μm
- Peaking time: < 1us
- Integration time: 5-10 us
- Parallel data port: 80 MHz I/O CMOS 3.3 V
- High speed serial data port: 1.1 Gb/s
- 8B10B encoder
- Configuration interface: SPI
- Two readout modes: trigger mode and continuous mode
- Zero compression readout (AERD)

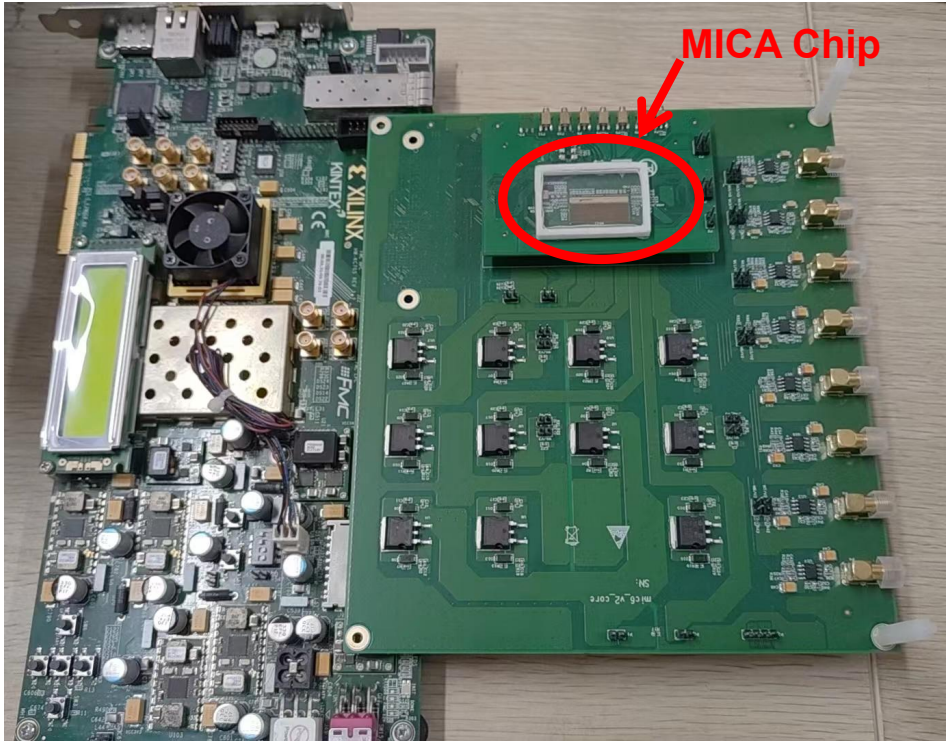
MICA Chip and Test System

Wafer of MICA Chip



MICA Chip and Test System

Test System



- KC705 FPGA ✓
- Mother board ✓
- Bonding board ✓
- Firmware ✓
- Software ✓
- Submodule Function test
- Submodule Performance test
- Full Chip Function test
- Full Chip Performance test

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- A CMOS process suitable for MAPS was developed in cooperation with the foundry.
- Based on this CMOS process, a pixel test chip and a evaluation system are developed.
- The ^{90}Sr source was used to test the pixel test chip.
- The high resistance substrate and negative bias effect are significant on this process.
- A fully functional MAPS chip MICA was designed based on this process.
- We have received the MICA wafer and the test system is ready.
- Submodule functional testing is underway.

Спасибо !