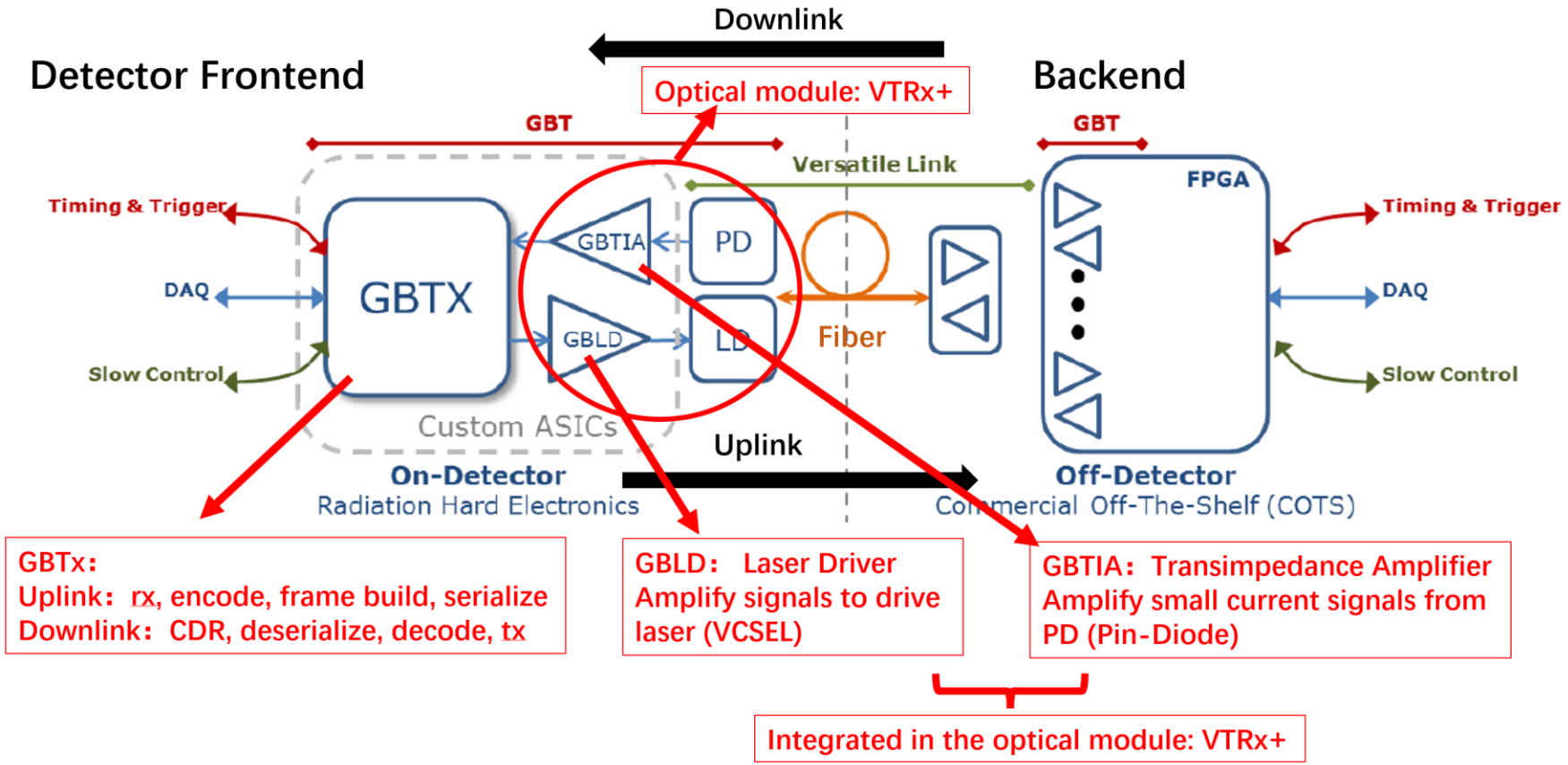
NICA_GBT Series ASICs Development

On behalf of the NICA_GBT family group,

July 23th, 2024

1. Background of GBT-Series ASICs
2. NICA_GBT Development
3. NICA_LD/NICA_TIA/Optical Module Development
4. Summary

GBT Series ASICs Developed by CERN

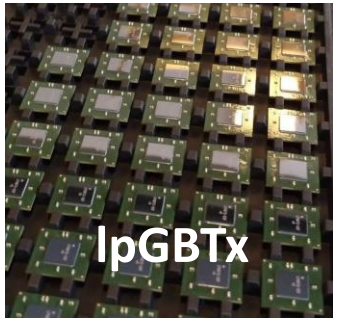


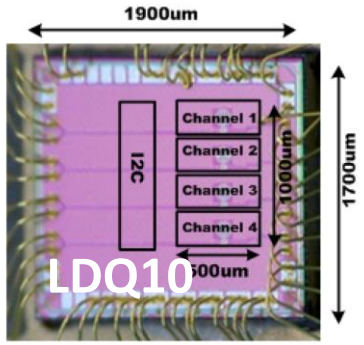
- **GBT : GigBit Transceiver**
- **GBT Project: aims to build a high-speed, bi-directional optical data transmission system between the detector front-end and the back-end. The GBT architecture is started by CERN from 2007**
- **GBT Series ASICs: GBTx, GBLD, GBTIA**

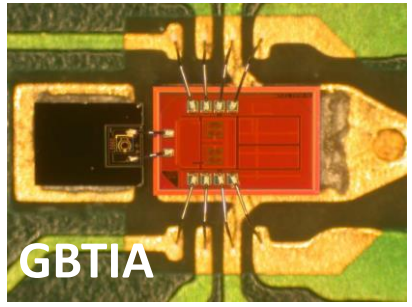
GBT Series ASICs by CERN

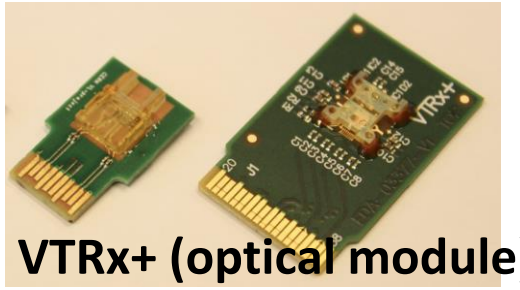
- The first generation GBT ASICs by CERN were based on 130nm CMOS technology, 2011
  - GBTx: uplink 5.12 Gbps, downlink 2.56 Gbps
  - GBLD: 5.12 Gbps/ch
  - GBTIA: 2.56 Gbps/ch
  - VTRx: 1Tx + 1Rx optical module (single-channel form)

- The second generation GBT ASICs by CERN were based on 65nm CMOS technology, 2019
  - lpGBTx: uplink 10.24/5.12 Gbps, downlink 2.56 Gbps
  - GBLD: 10.24 Gbps/ch x 4 ch (array form, this chip is also called LDQ10)
  - lpGBTIA: 2.56 Gbps/ch
  - VTRx+: 4Tx + 1Rx optical module (array form)



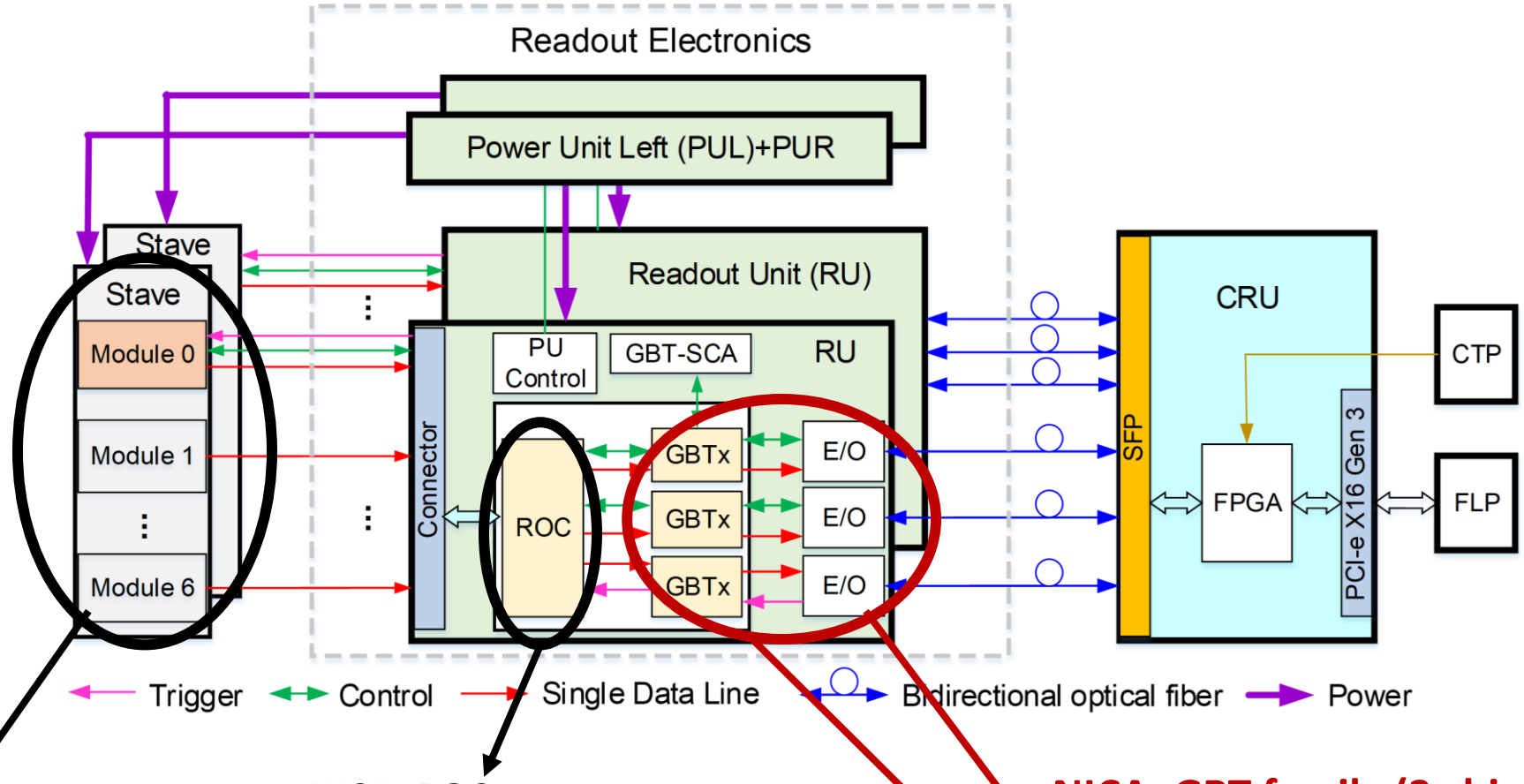






GBT series ASICs and optical module pictures developed by CERN

NICA_GBT ASICs in the Readout Electronics System



NICAMOST:
Monolithic Active Pixel Sensor (MAPS) ASIC

NICA_ROC:
Data collection and control distribution ASIC

NICA_GBT family (3 chips + optical module)

NICA_ LD : Laser Driver ASIC

NICA_TIA : Transimpedance Amplifier ASIC(Receiver)

NICA_GBTx: Bi-directional data interface ASIC

Note: NICA_LD and NICA_TIA are inside the optical module

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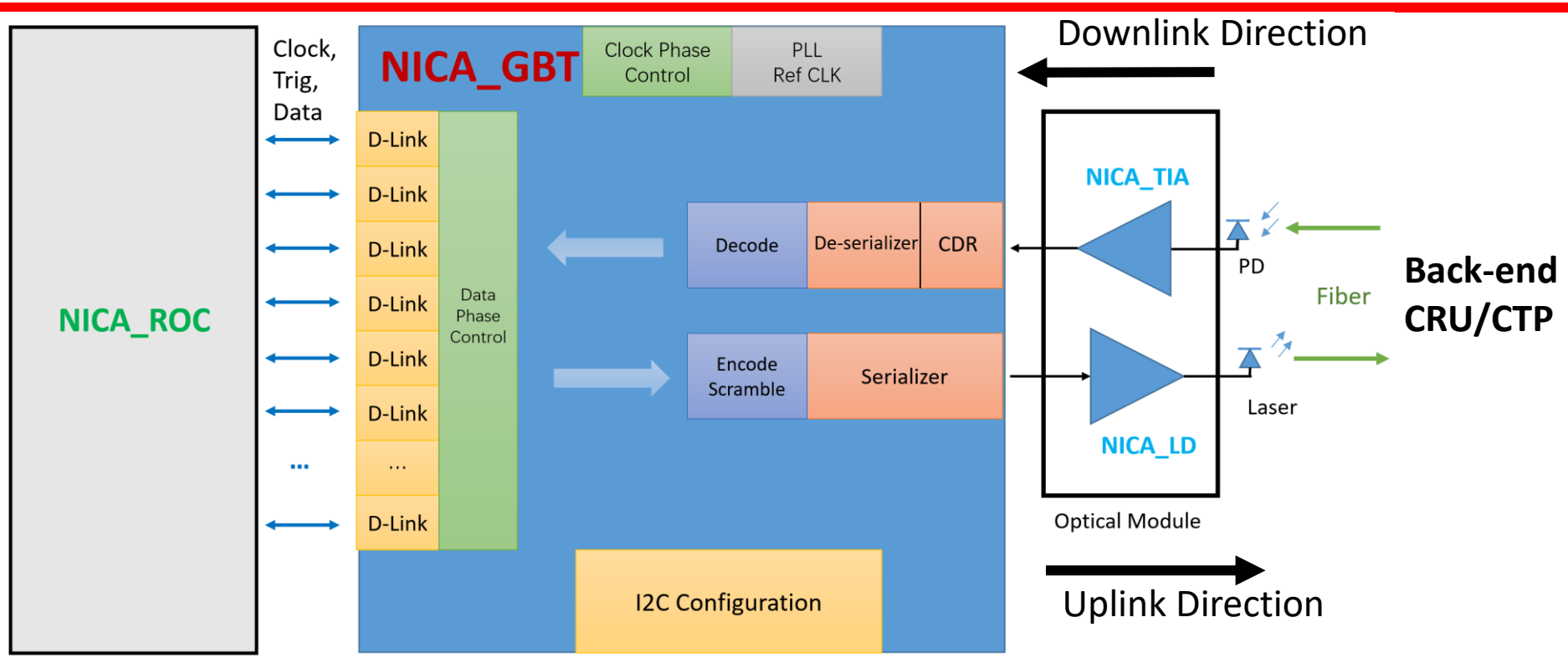
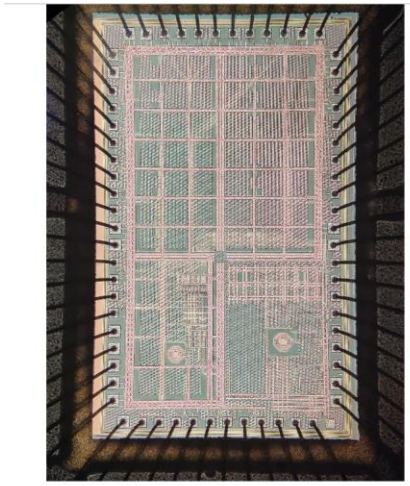
NICA_GBT ASIC Development



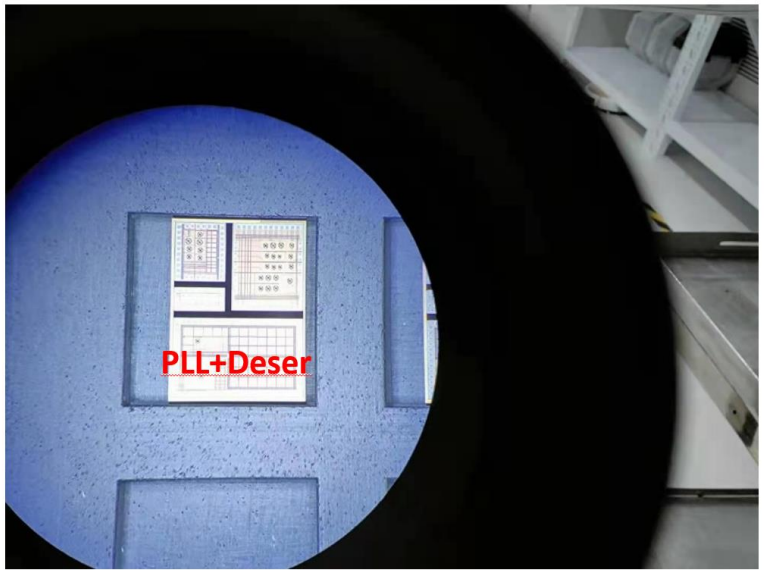
- **NICA_GBT ASIC includes:**
  - **High-speed Serializer 16:1 10.24 Gbps**
  - **High-speed Deserializer 1:16 2.56 Gbps**
  - **PLL (Phase-Lock-Loop) 5.12 GHz** — **generate precise clock**
  - **CDR (Clock Data Recovery) 2.56 Gbps** — **recover clock from high-speed serial data**
  - **Encode, Decode (Digital part)**
  - **High-speed Tx/Rx**
  - **Data Phase Control (Phase Aligner)** — **automatically adjust the delay of the multi-channel data**
  - **Clock Phase control** — **adjust the phase (delay) of the output clock**

NICA_GBT ASIC Development in 2021~2022

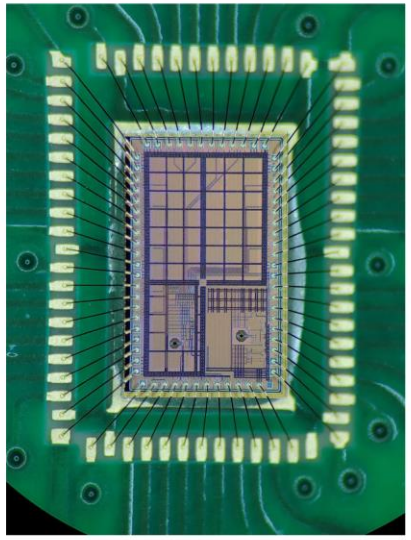
- **Firstly designed and tested the 5.12 GHz PLL module and the Deserializer module in 2021 (the first design related to NICA_GBT)**



PLL + Deserializer ASIC after wire-bonding

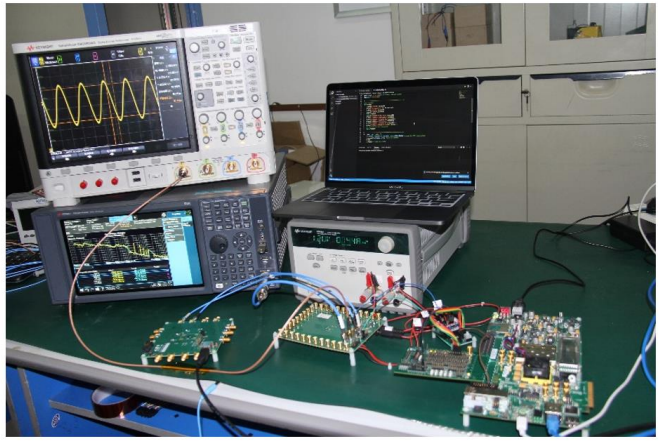


PLL + Deserializer ASIC practical picture under the microscope



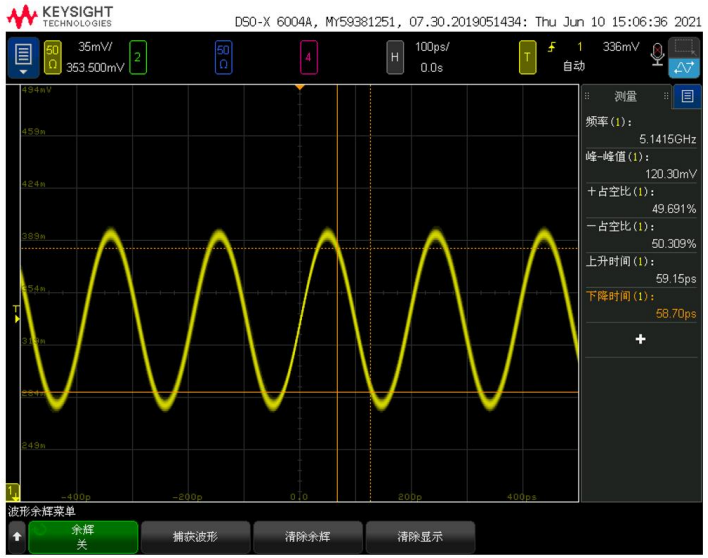
PLL + Deserializer ASIC after wire-bonding on the test board

NICA_GBT ASIC Development in 2021~2022

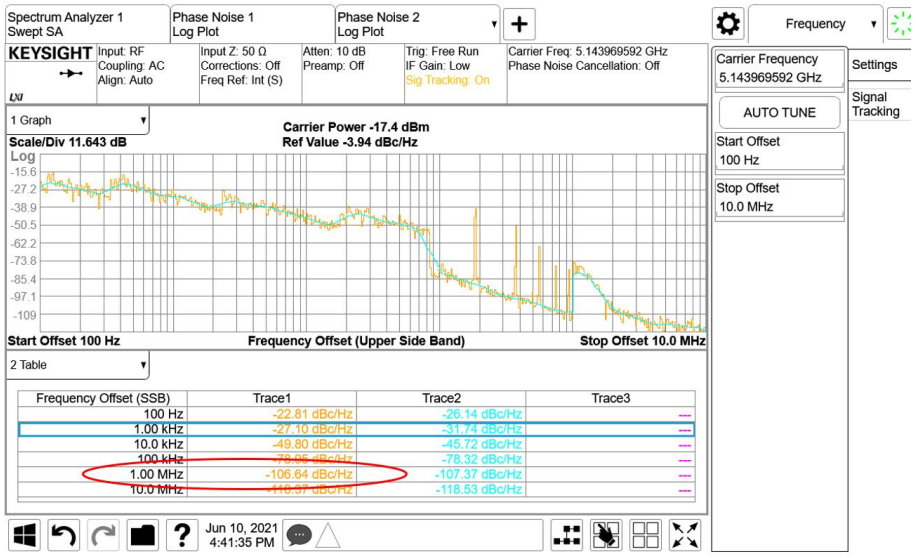


PLL locks at the targeted frequency with an adjustable range, and the tested phase noise is -106.6 dBc/Hz @1Mhz

- **Successfully verified the function of the PLL and Deseiralizer Module in NICA_GBT ASIC**



PLL output clock in a real-time scope



PLL output clock noise analysis

NICA_GBT ASIC Development in 2021~2022

Published by IOP Publishing for Sissa Medialab

Received: *November 26, 2021*
Accepted: *July 19, 2022*
Published: *September 6, 2022*

12th International Conference on Position Sensitive Detectors
12–17 September, 2021
Birmingham, U.K.

PLL in NICA_GBTx
JINST 2022

A low noise 5.12 GHz PLL ASIC in 55 nm for NICA multi purpose detector project

C. Zhao,[a] D. Guo,[a,*] Q. Chen,[a] Z. Guo,[a] R. Arteche,[b,c] C. Ceballos,[b] N. Fang,[a] Y. Gan,[a] Y. Murin,[b] L. Yi[a] and X. Sun[a] for the MPD ITS collaboration

[a] *PLAC, Key Laboratory of Quark and Lepton Physics (MOE), Central China Normal University, Wuhan, Hubei 430079, China*
[b] *Joint Institute for Nuclear Research, Dubna, Russia*
[c] *Center for Technological Applications and Nuclear Development, Havana, Cuba*

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Received: *November 26, 2021*
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12th International Conference on Position Sensitive Detectors
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Deserializer in NICA_GBTx
JINST 2022

A 13 Gbps 1:16 deserializer ASIC for NICA multi purpose detector project

Q. Chen,[a] D. Guo,[a,*] C. Zhao,[a] Z. Guo,[a] R. Arteche,[b,c] C. Ceballos,[b] N. Fang,[a] Y. Gan,[a] Y. Murin,[b] L. Yi[a] and X. Sun[a] for the MPD ITS collaboration

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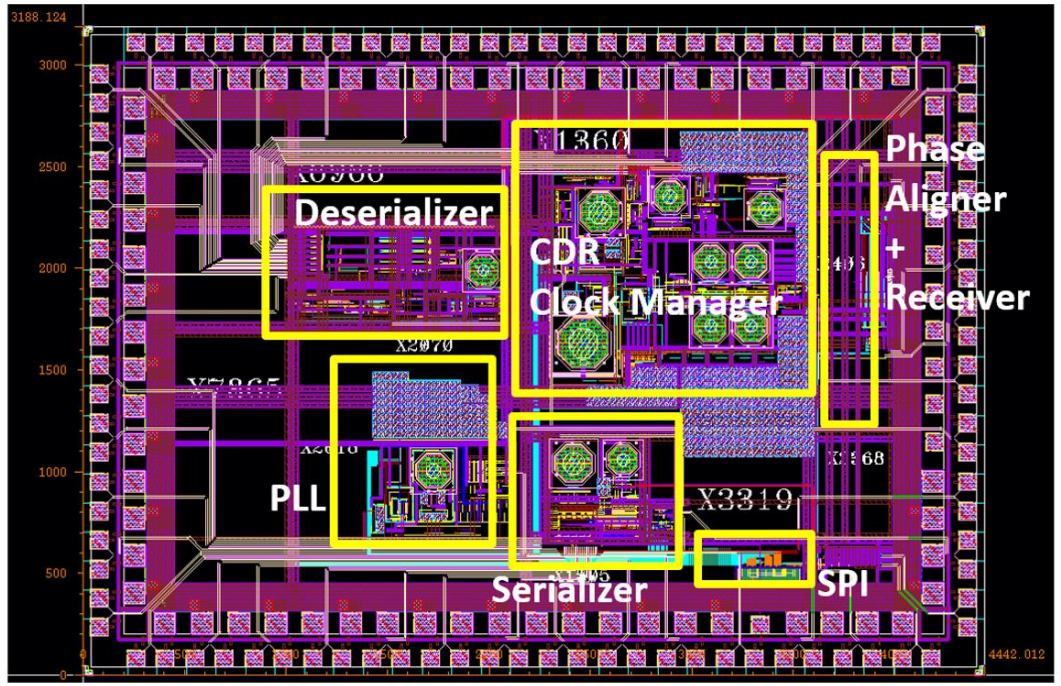
[b] *Joint Institute for Nuclear Research, Dubna, Russia*
[c] *Center for Technological Applications and Nuclear Development, Havana, Cuba*

- **The PLL and Deserializer work has been published on behalf of the MPD ITS collaboration in JINST 2022.**

NICA_GBT ASIC Development in 2022~2023



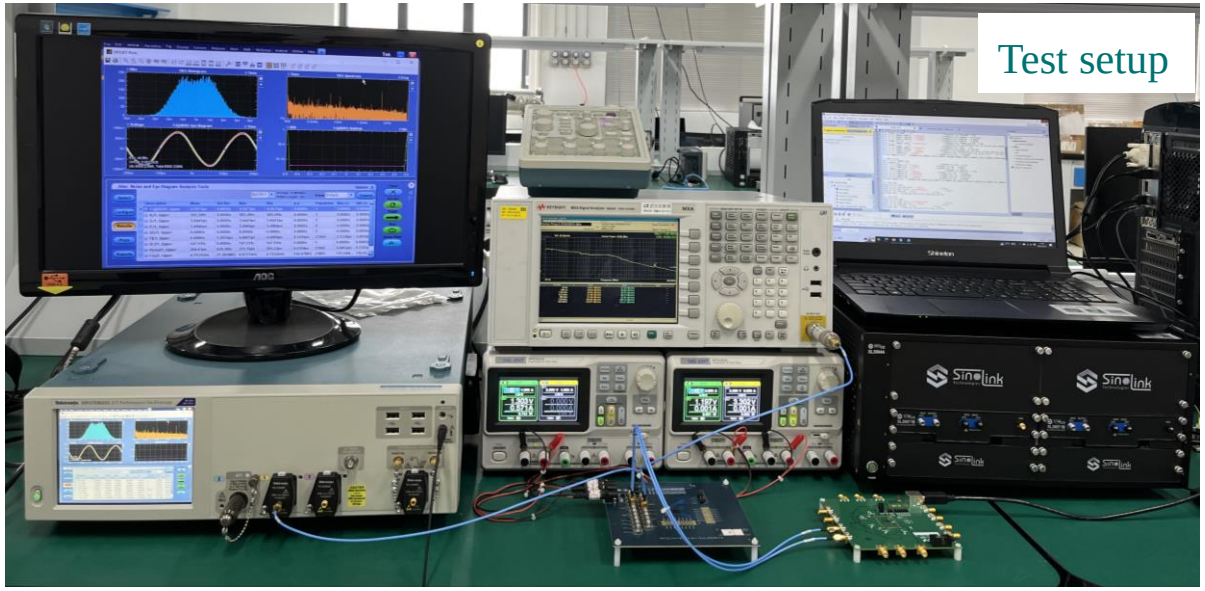
NICA_GBT_v1 overall layout

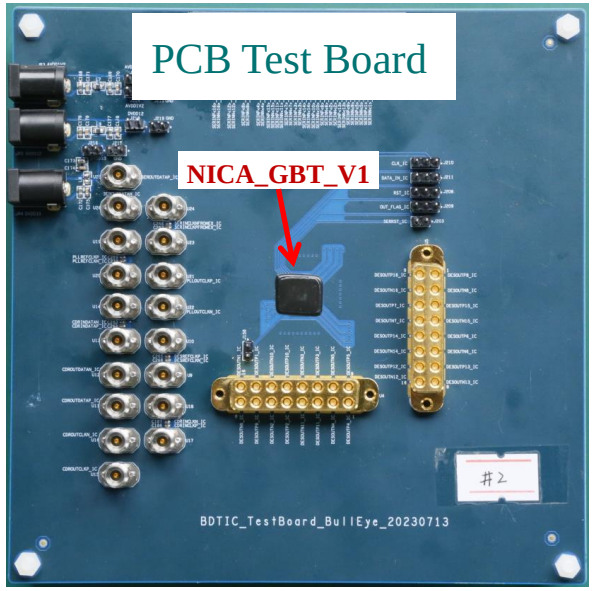
NICA_GBT_v1 includes the following sub-modules:

- **5.12Gbps/10.24 Gbps 16:1 Serializer**
- **2.56Gbps/10.24 Gbps 1:16 Deserializer**
- **2.56 Gbps/10.24 Gbps CDR**
- **5.12 GHz PLL**
- **Clock manager module**
- **160M/320M/640M/1.28Gbps Phase Aligner**
- **Up to 1.28 Gbps rail-to-rail Receiver(to front-end)**
- **10.24 Gbps three-tap pre-emphasis**

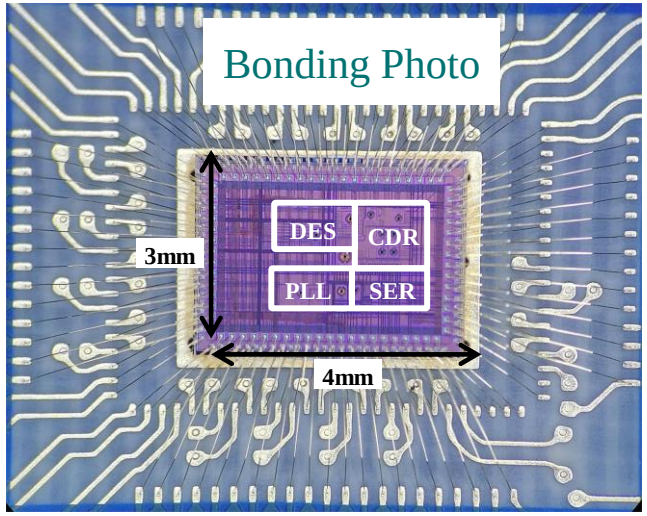
- NICA_GBT_v1: the first prototype version of NICA_GBT with core analog sub-modules.
- Total pins: 166
  Die size: 3333 um x 4444 um
  (Dimensions shown in the picture will shrink to 90%)
- Dual-row wire-bonding pads used in this version for test, and will be replaced by BGA package in the next run.
- This ASIC submitted on October 16th 2022, tested in 2023.

NICA_GBT ASIC Development in 2022~2023



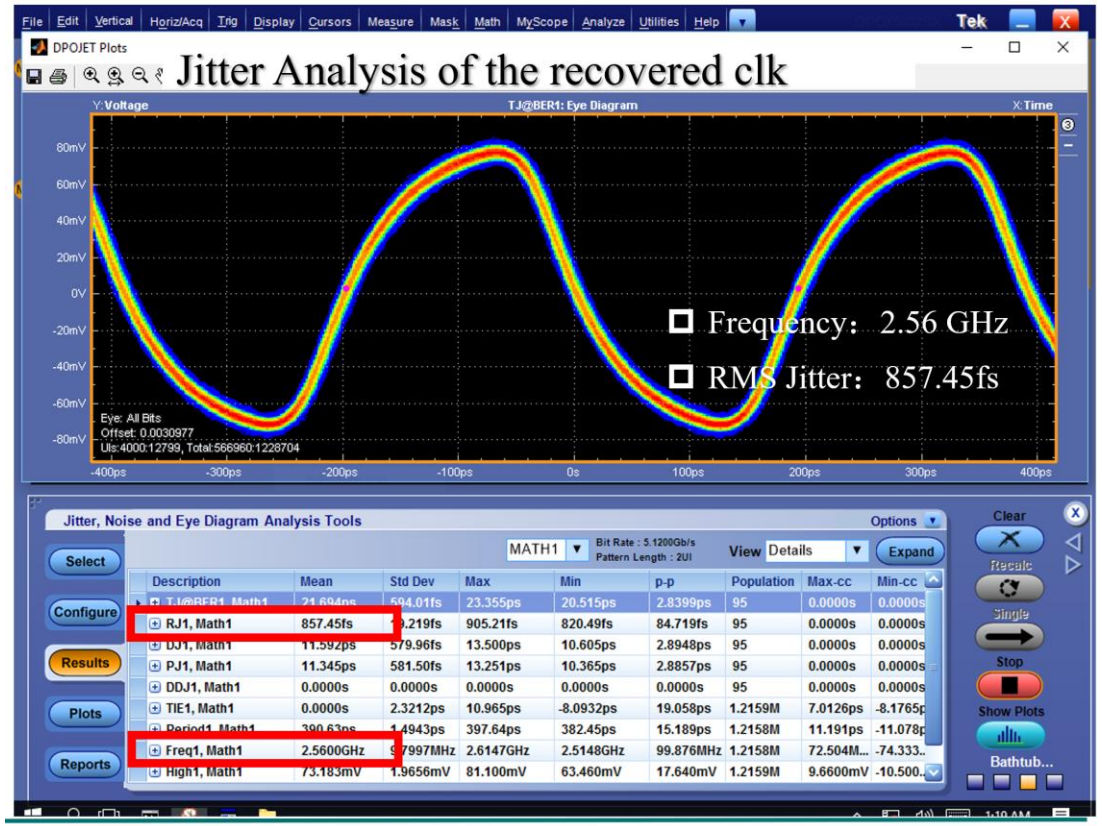


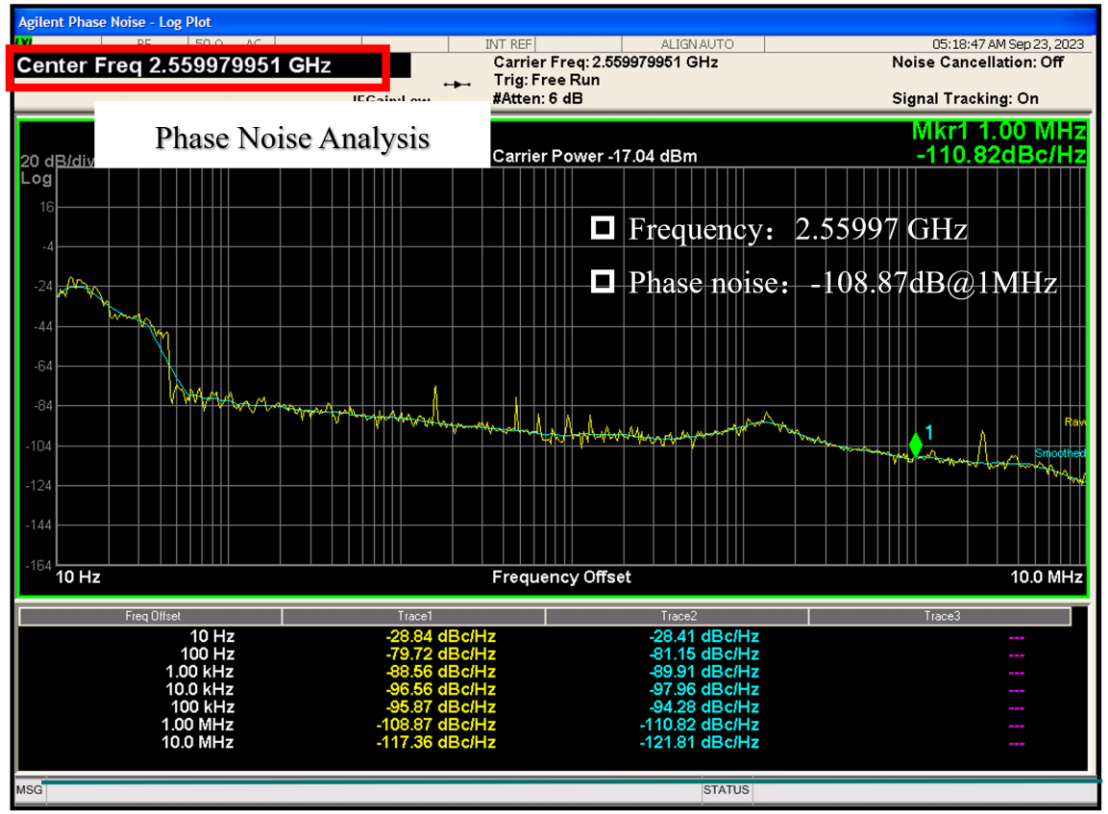
- **Process： 55nm CMOS Technology**
- **Chip Size： 3 mm × 4 mm**
- **CDR core size: 1000μm × 700μm**
- **CDR power consumption:200 mW**
  including Rx and CML driver



NICA_GBT_V1 practical pictures under microscope

NICA_GBT ASIC Development in 2022~2023



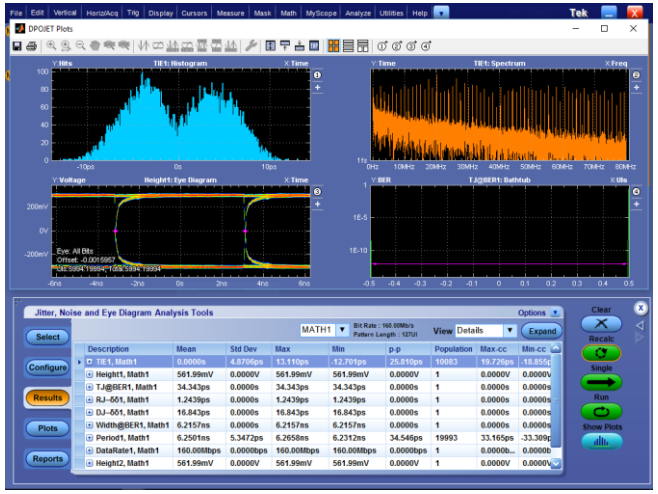


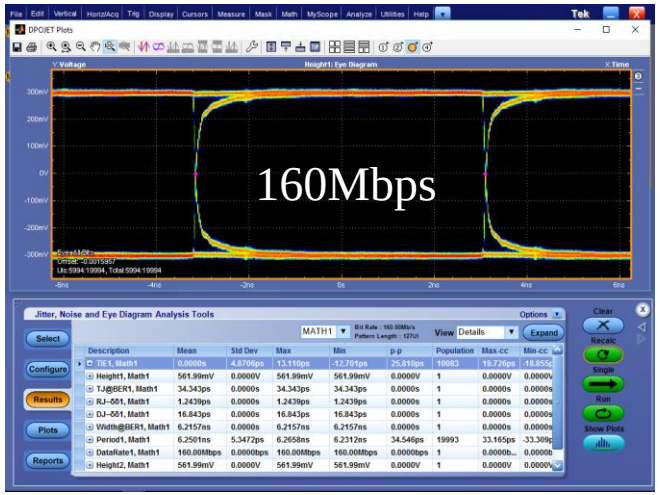
- **2.56 Gbps Clock-Data-Recovery (CDR) function was tested and verified. √**

2.56 Gbps CDR Test Verified √

NICA_GBT ASIC Development in 2022~2023

OUT1-OUT5-OUT9-OUT13 OUT2-OUT6-OUT10-OUT14 OUT3-OUT7-OUT11-OUT15 OUT4-OUT6-OUT12-OUT16



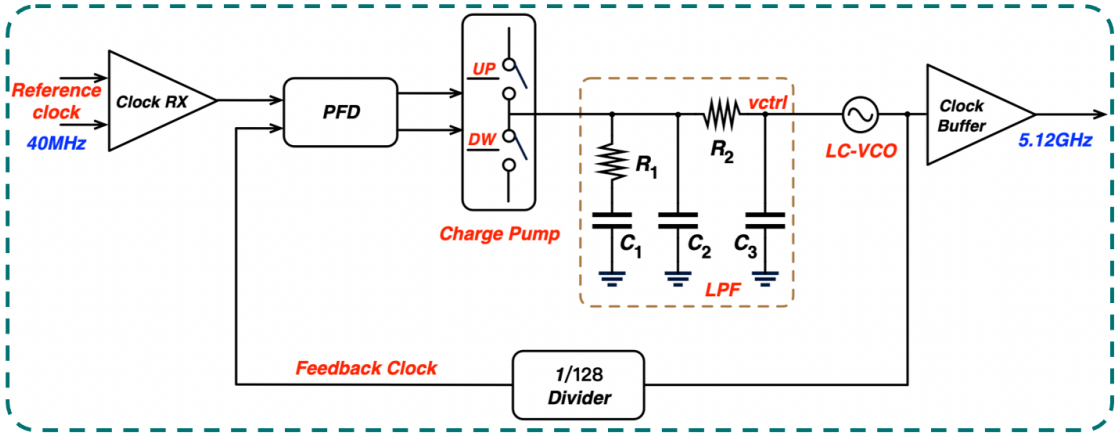


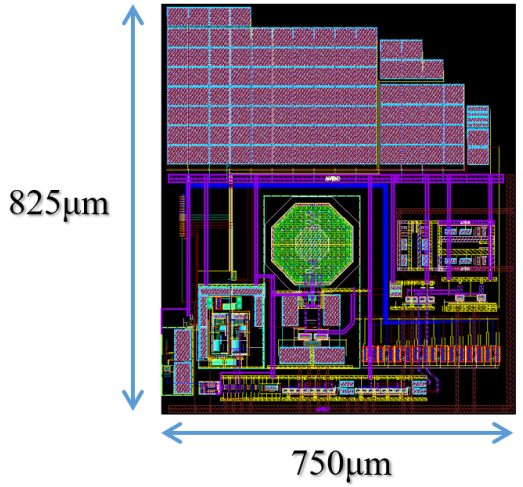
1	OUT1	10110111	9	OUT3	00010100
2	OUT5	10110001	10	OUT7	01111001
3	OUT9	10100101	11	OUT11	00010110
4	OUT13	11011100	12	OUT15	01110101
5	OUT2	11001010	13	OUT4	00111110
6	OUT6	10111111	14	OUT8	10000111
7	OUT10	10000001	15	OUT12	00010010
8	OUT14	00000110	16	OUT16	01101100

Deserializer + CDR Test Verified √

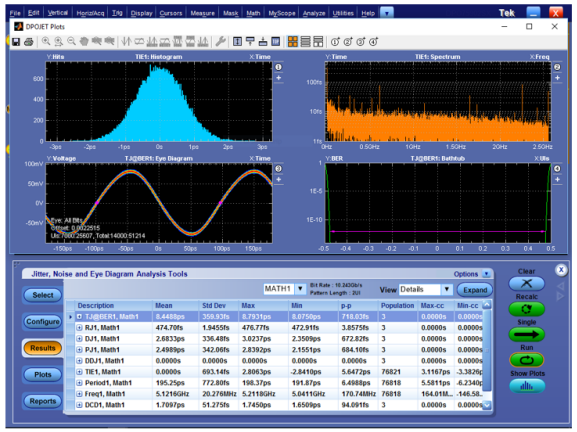
- **2.56 Gbps 1: 16 Deserializer + CDR were tested and verified. √**

NICA_GBT ASIC Development in 2022~2023

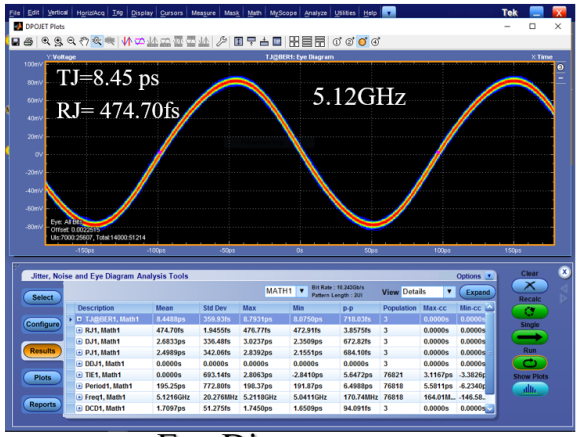




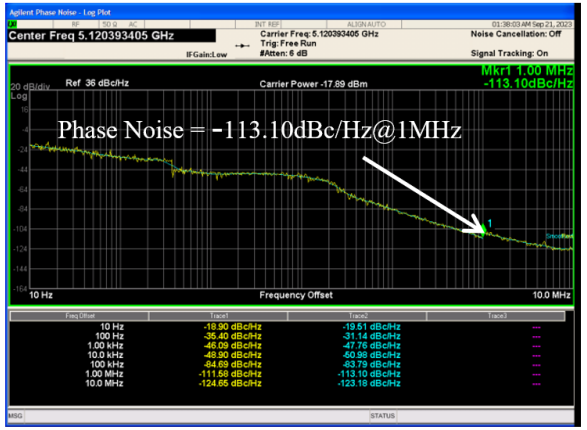
PLL Structure



Jitter analysis



Eye Diagram



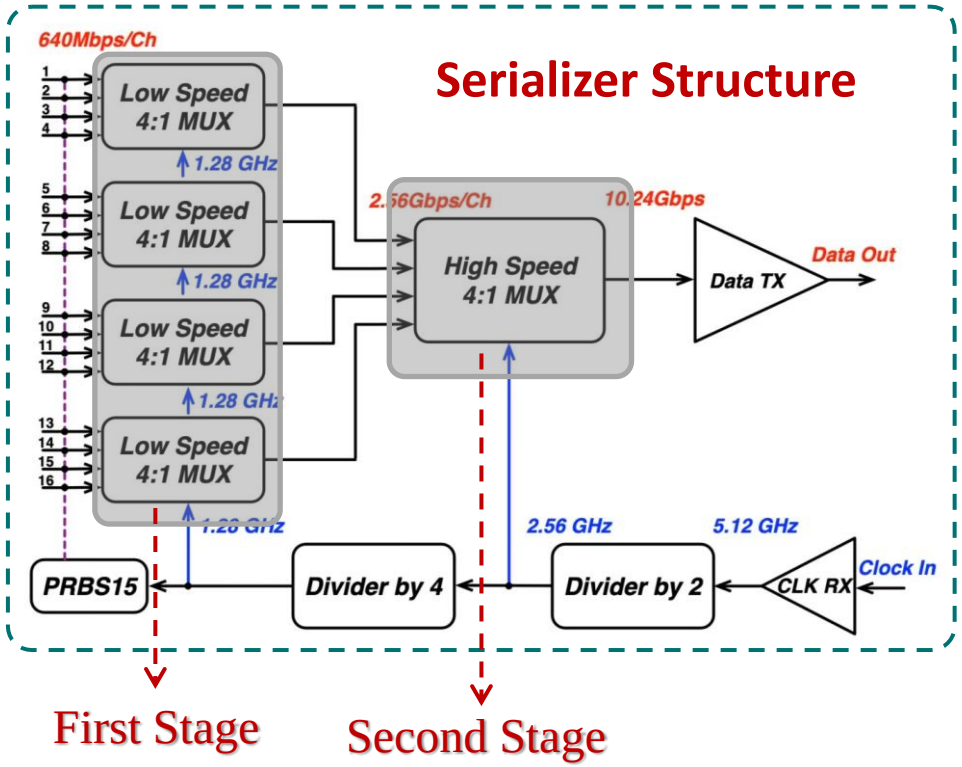
Phase Noise Curve

5.12 GHz PLL Test Verified √

- ✓ **Frequency： 5.12 GHz**
- ✓ **RMS Jitter： 474.70 fs**
- ✓ **Total Jitter： 8.45ps**
- ✓ **Phase noise： -113dB@1MHz**

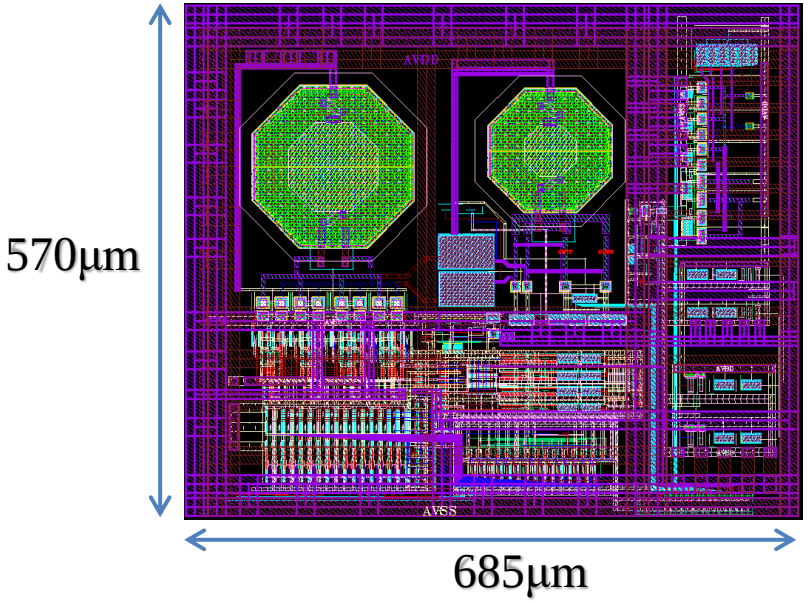
Improve the PLL design (2021), get better performance

NICA_GBT ASIC Development in 2022~2023



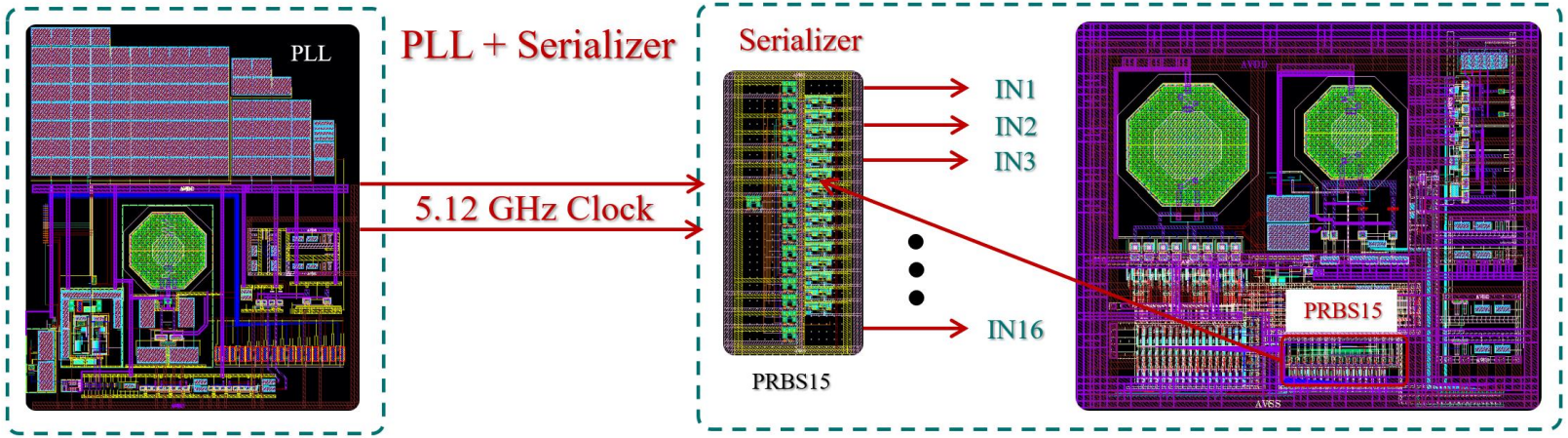
- ✓ Input Data： 640 Mbps/Ch × 16
- ✓ Input Clock： 5.12 GHz
- ✓ Output Data： 10.24 Gbps
- ✓ Serializer core size: 685μm × 570μm

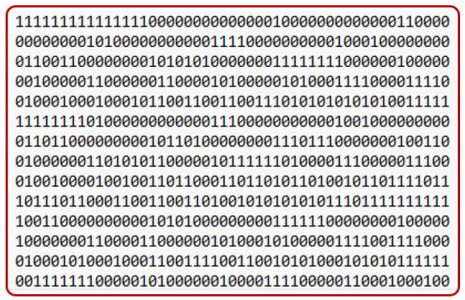
- ✓ First Stage: 16→4
- ✓ Second Stage: 4→1
- ✓ PRBS15: Self-test module



16:1 10.24Gbps Serializer Design

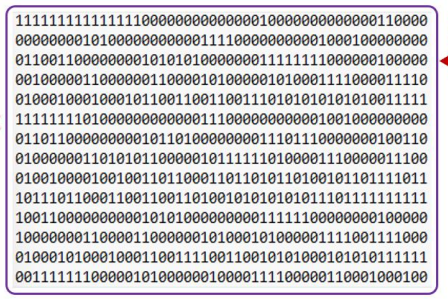
NICA_GBT ASIC Development in 2022~2023





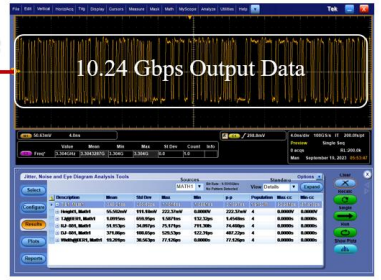
Standard PRBS15 Data

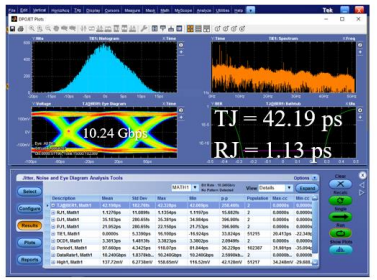
Logic Correct



Measured Data

Capture

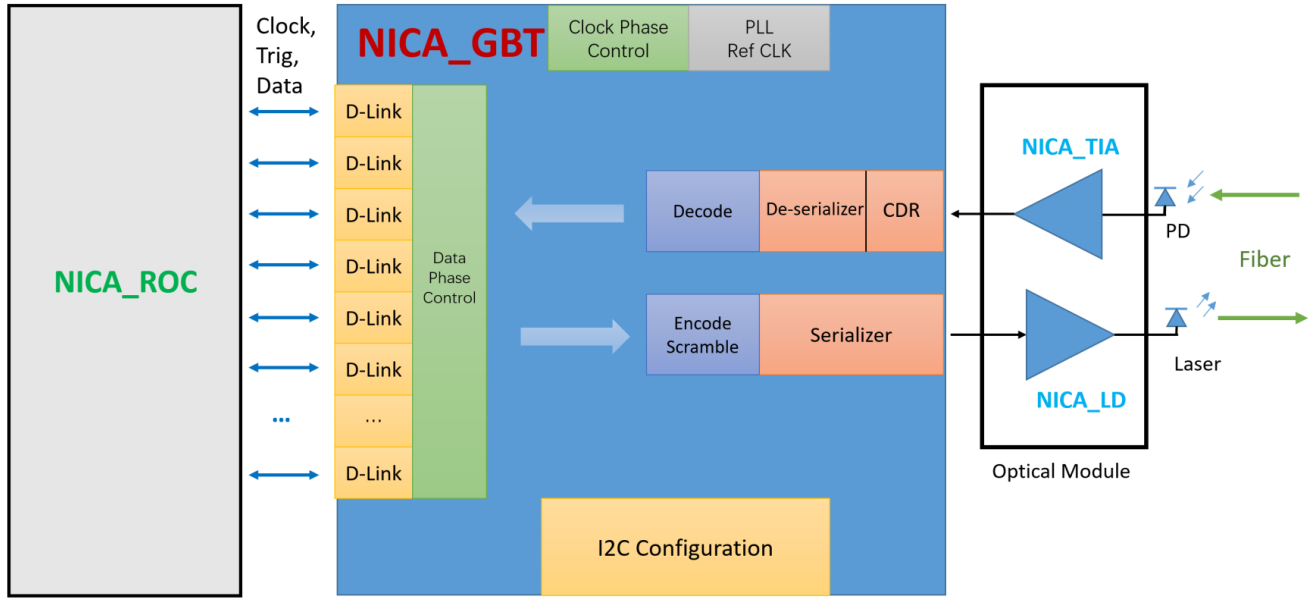




- ✓ **Total Jitter = 42.19 ps**
- ✓ **The logic of output data is correct**

PLL+ Serializer Test Verified √

Summary about NICA_GBT ASIC Development



- **NICA_GBT ASIC includes:**
  - **High-speed Serializer** — **Done √**
  - **High-speed Deserializer** — **Done √**
  - **PLL (Phase-Lock-Loop)** — **Done √**
  - **CDR (Clock Data Recovery)** — **Done √**
  - **Encode, Decode (Digital part)** — **under design (first version will be submitted within 2024)**
  - **High-speed Tx/Rx** — **Done √ (function verified, need to be replicated in each ch)**
  - **Data Phase Control (Phase Aligner)** — **Designed and under testing (need to be replicated after verification)**
  - **Clock Phase control** — **To be designed (first version will be submitted within 2024)**

1. Background of GBT-Series ASICs
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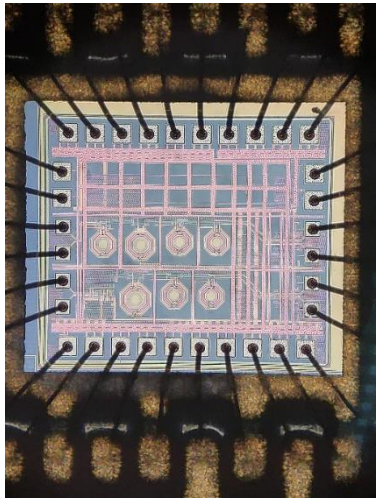
NICA_LD and NICA_TIA ASICs Development

- **Two ASICs have been designed and tested in 2021~2022.**
  - **NICA_LDLA:**
  - **10 Gbps single-channel Laser Driver (Tx) + TIA +LA (Rx)**

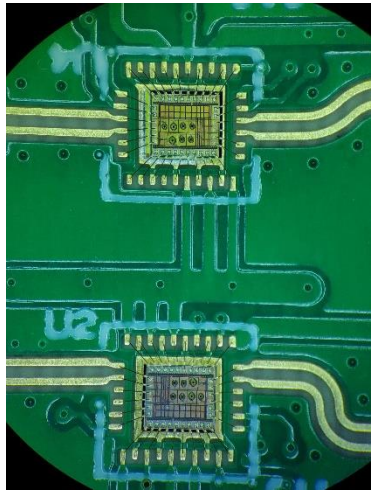
    --corresponding to the VTRx(1Tx, 1Rx) single-channel form

  - **NICA_LDAr:**
  - **10 Gbps/ch Laser driver array(multi-channel Tx)**

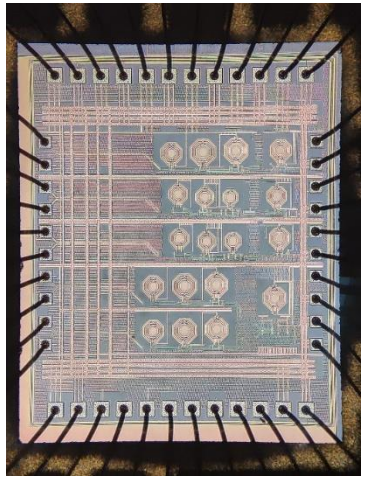
    --corresponding to the VTRx+(3Tx, 1Rx) array form



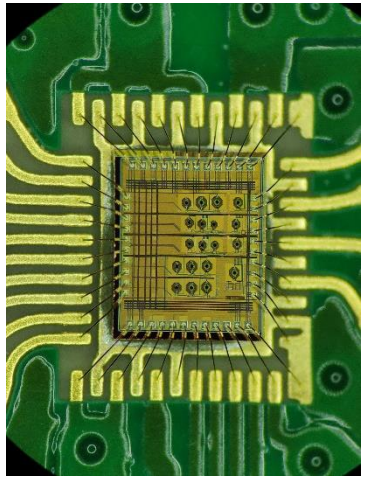
LDLA Chip



LDLA Chip on the board

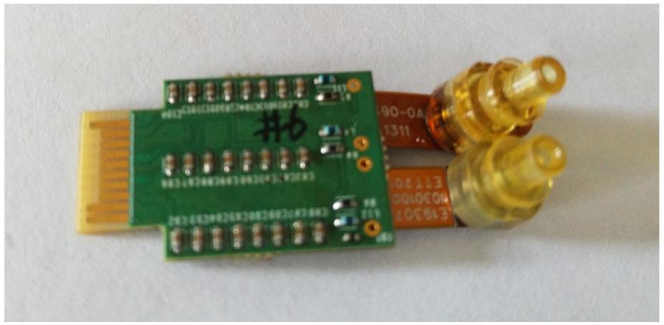


LDAr Chip

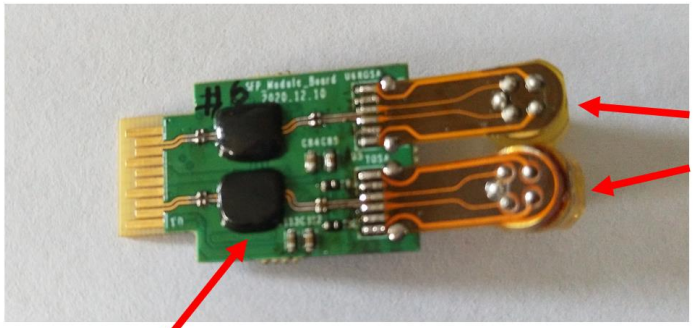


LDAr Chip on the board

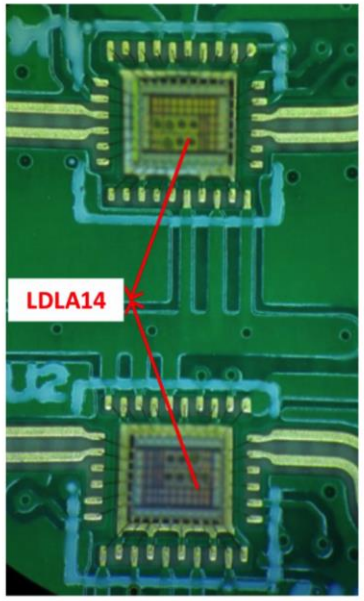
LDLA ASIC Test

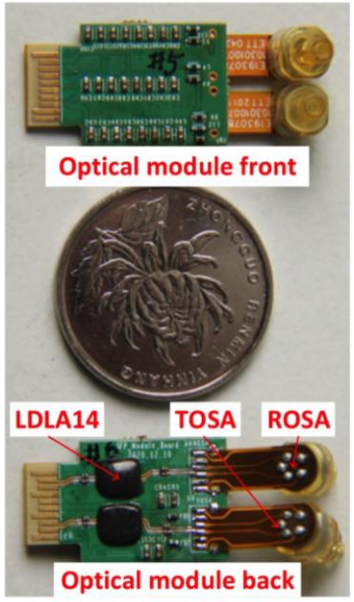


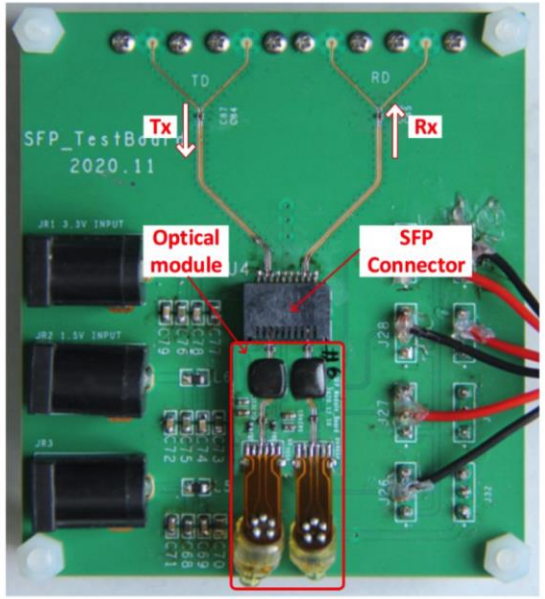
Optical test board for LDLA chip



LDLA chip
drives TOSA to emit optical signal (Tx direction)
receives small signal from ROSA (Rx direction)

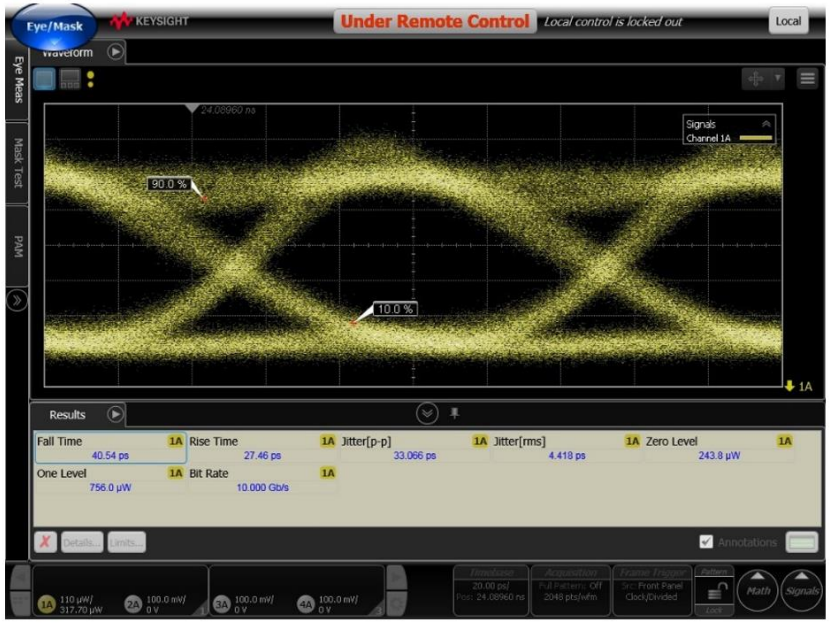




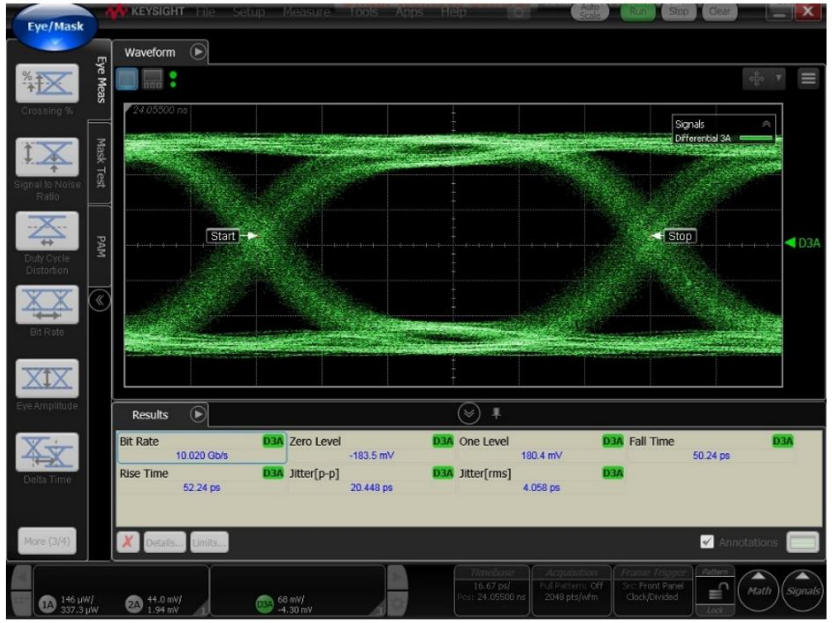


- LDLA ASIC was integrated into a customized optical module based on TOSA/ROSA. (similar to VTRx)
- However we will not use this TOSA/ROSA based optical module. The optical module shown here is only for the test of the ASIC.

LDLA ASIC Test



10 Gbps optical eye diagram
of laser driver (Tx direction)



10 Gbps electrical eye diagram
of TIA + Limiting Amplifier (Rx direction)

- 10 Gbps eyes have all passed the eye mask test.
- Tx + Rx loop back BER (bit error) test has also been conducted, BER better than 1E-12 has been achieved.

LDLA ASIC Test

- **The LDLA ASIC work has been published on behalf of the MPD ITS collaboration in JINST 2022.**

Jinst

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *September 29, 2021*
ACCEPTED: *November 24, 2021*
PUBLISHED: *January 7, 2022*

22ND INTERNATIONAL WORKSHOP ON RADIATION IMAGING DETECTORS
JUNE 27–JULY 1, 2021
GHENT, BELGIUM

NICA_LD+TIA_v1
JINST 2022

LDLA14: a 14 Gbps optical transceiver ASIC in 55 nm for NICA multi purpose detector project

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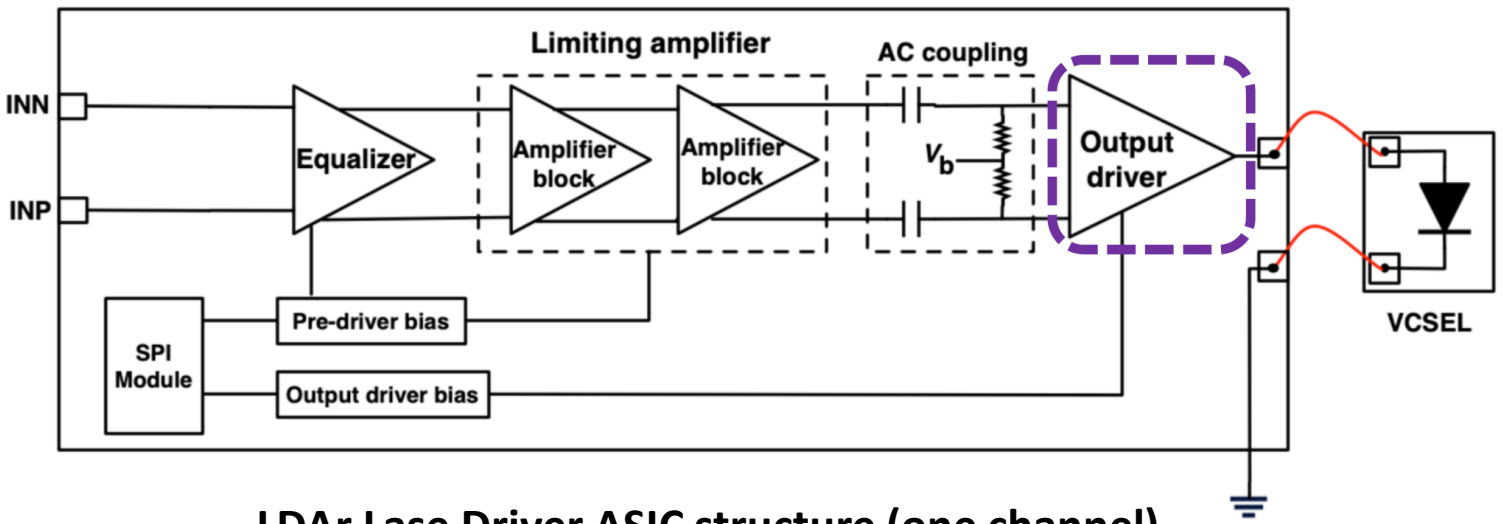
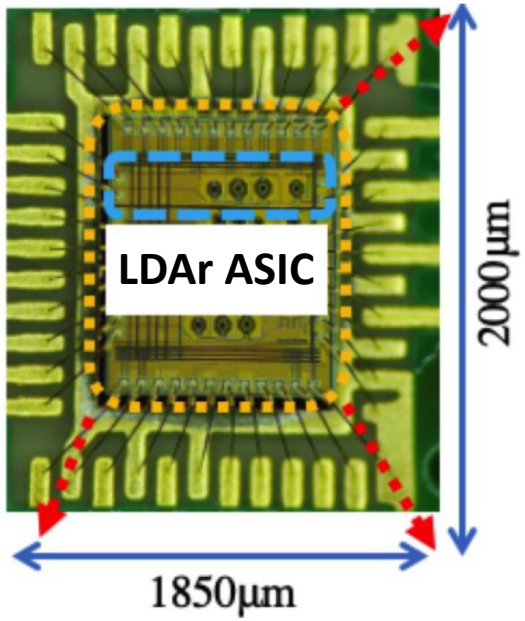
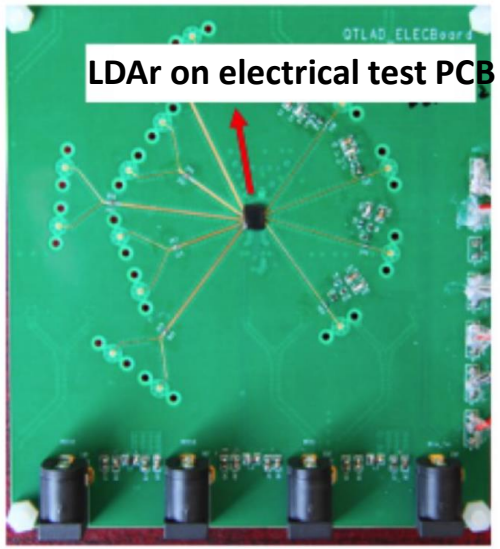
LDAr ASIC Test

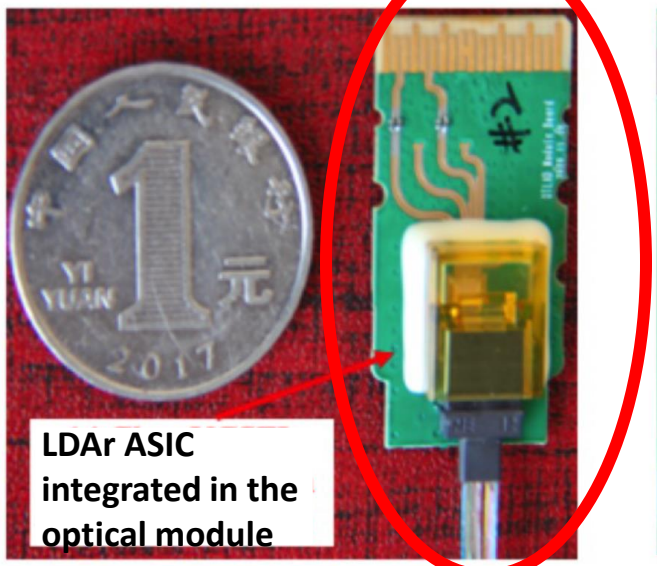


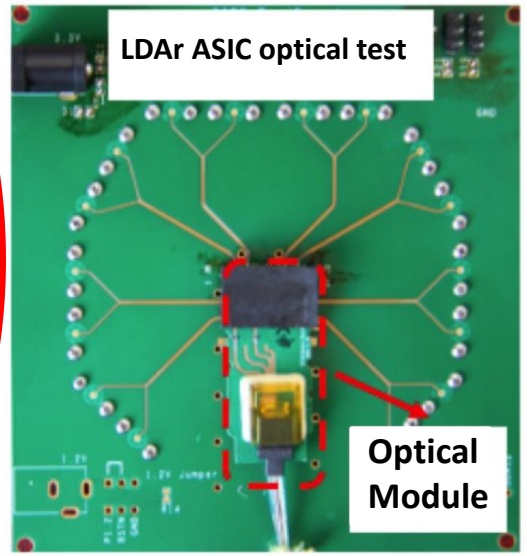
- Customized array optical module (similar to VTRx+)
- This will be targeted optical module form. However, what is shown here is not the final version.

LDAr Lase Driver ASIC structure (one channel)

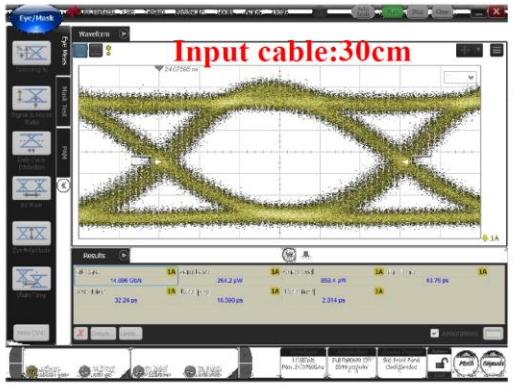








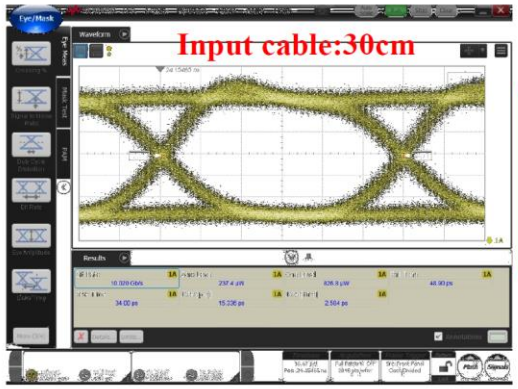
LDAr ASIC Test



14 Gbps optical eye

Bit Rate	14Gbps	RMSJ	2.6ps
Rise Time	32.2ps	PPJ	16.6ps
Fall Time	43.8ps	Amp	594.2μW

◆ 两种速率下眼图张开且清晰



10 Gbps optical eye

Bit Rate	10Gbps	RMSJ	2.6ps
Rise Time	34.0ps	PPJ	15.3ps
Fall Time	48.9ps	Amp	589.4μW

- **Clear and wide-open 10 Gbps optical eye has been captured in the LDAr ASIC optical test.**

JINST

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 26, 2022*
ACCEPTED: *July 19, 2022*
PUBLISHED: *August 23, 2022*

12TH INTERNATIONAL CONFERENCE ON POSITION SENSITIVE DETECTORS
12–17 SEPTEMBER, 2021
BIRMINGHAM, U.K.

NICA_LDAr
JINST 2022

A 14 Gbps VCSEL driving ASIC in 55 nm for NICA multi purpose detector project

C. Zhao,[a] Q. Chen,[a] Z. Guo,[a] R. Arteche,[b,c] C. Ceballos,[b] N. Fang,[a] Y. Gan,[a] Y. Murin,[b] L. Yi,[a] D. Guo[a,*] and X. Sun[a,*] for the MPD ITS collaboration

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[b] *Joint Institute for Nuclear Research, Dubna, Russia*
[c] *Center for Technological Applications and Nuclear Development, Havana, Cuba*

- **LDAr ASIC work has been published on behalf of the MPD ITS collaboration in JINST 2022.**

1. Background of GBT-Series ASICs
2. NICA_GBT Development
3. NICA_LD/NICA_TIA/Optical Module Development
4. Summary

NICA_GBT ASIC

- **NICA_GBT ASIC includes:**
  - **High-speed Serializer** — Done √
  - **High-speed Deserializer** — Done √
  - **PLL (Phase-Lock-Loop)** — Done √
  - **CDR (Clock Data Recovery)** — Done √
  - **Encode, Decode (Digital part)** — under design (first version will be submitted within 2024)
  - **High-speed Tx/Rx** — Done √ (function verified, need to be replicated in each ch)
  - **Data Phase Control (Phase Aligner)** — Designed and under testing (need to be replicated after verification)
  - **Clock Phase control** — To be designed (first version will be submitted within 2024)

- **What else needs to be done:**
  - **Encode, Decode (Digital part) design, test and iterative design if needed**
  - **Phase Aligner test, iterative design(if needed) and integration**
  - **Clock Phase control design, test and integration**
  - **Overall ASIC integration (Large-scale anlog-digital-mixed ASIC)**

    The above work are planned to be achieved in 2025~2026
  - **BGA package (design, manufacture, test)**
  - **Chip test (BGA)**

NICA_LD, NICA_TIA ASICs and optical module

- **NICA_LD**
  - **Core design has been tested and verified** **Done √**
  - **What else needs to be done?**
    - **Optimize the design (chip area and the power consumption)**
    - **The final version integration (full four-channel form)**

- **NICA_TIA**
  - **Core design has been tested and verified** **Done √**
  - **What else needs to be done?**
    - **Optimize the design (data rate and the power consumption)**
    - **The final version design**

- **Optical module**
  - **Prototype has been designed and tested** **Done √**
  - **What else needs to be done?**
    - **Optimize the design (related to stable and reliable mechanics, assembly ..)**
    - **The final version.**

All the NICA_LD, NICA_TIA and optical module work is planned to be done in 2025.

Thanks!

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