SPD Range (muon) System Digital Electronics
Current status

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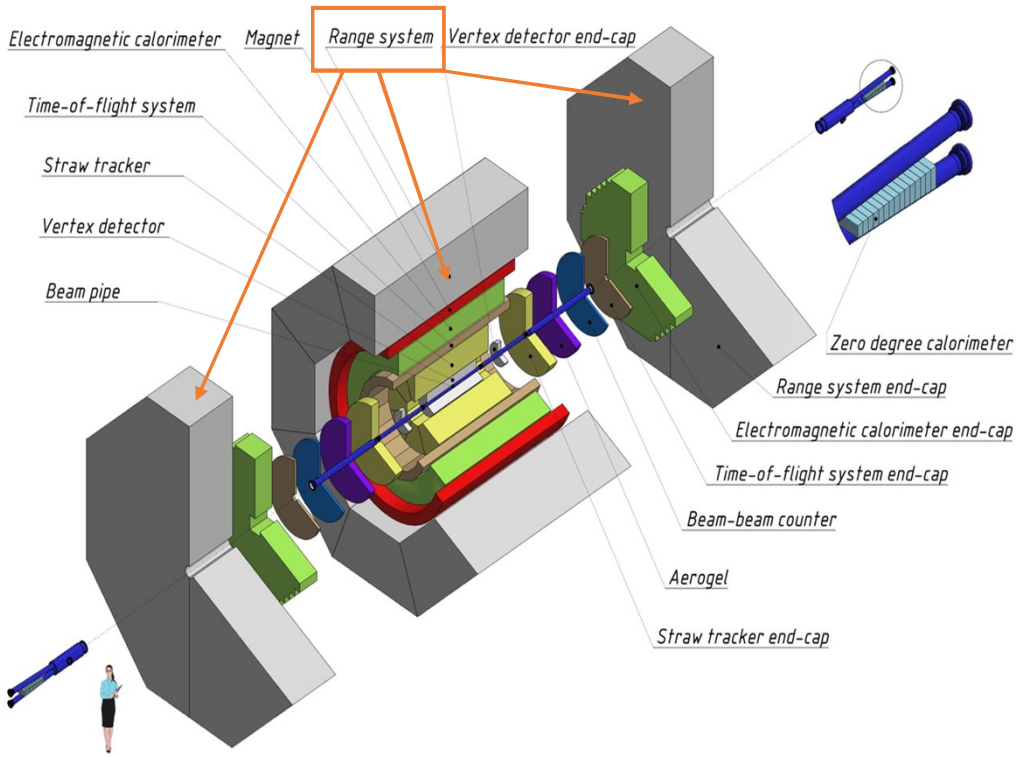
On behalf of the Muon System team

SPD Collaboration meeting, Dubna, April 24, 2023

Range System for detecting muons



- ~1000 ton weight;
- ~130k Read Out channels ;
- ~ 680 Read Out FEE cards;
- ~ 76 VME 6U crates;
- 16 racks (5 crates/rack);
- Total power consumption ~ 16 kW
- data flow estimation:

  ($3*10^6$ events/s *200 hit/event * 4 Bytes / hit) **3 GByte/s**

The prototype of the digital electronics for Muon System for SPD NICA

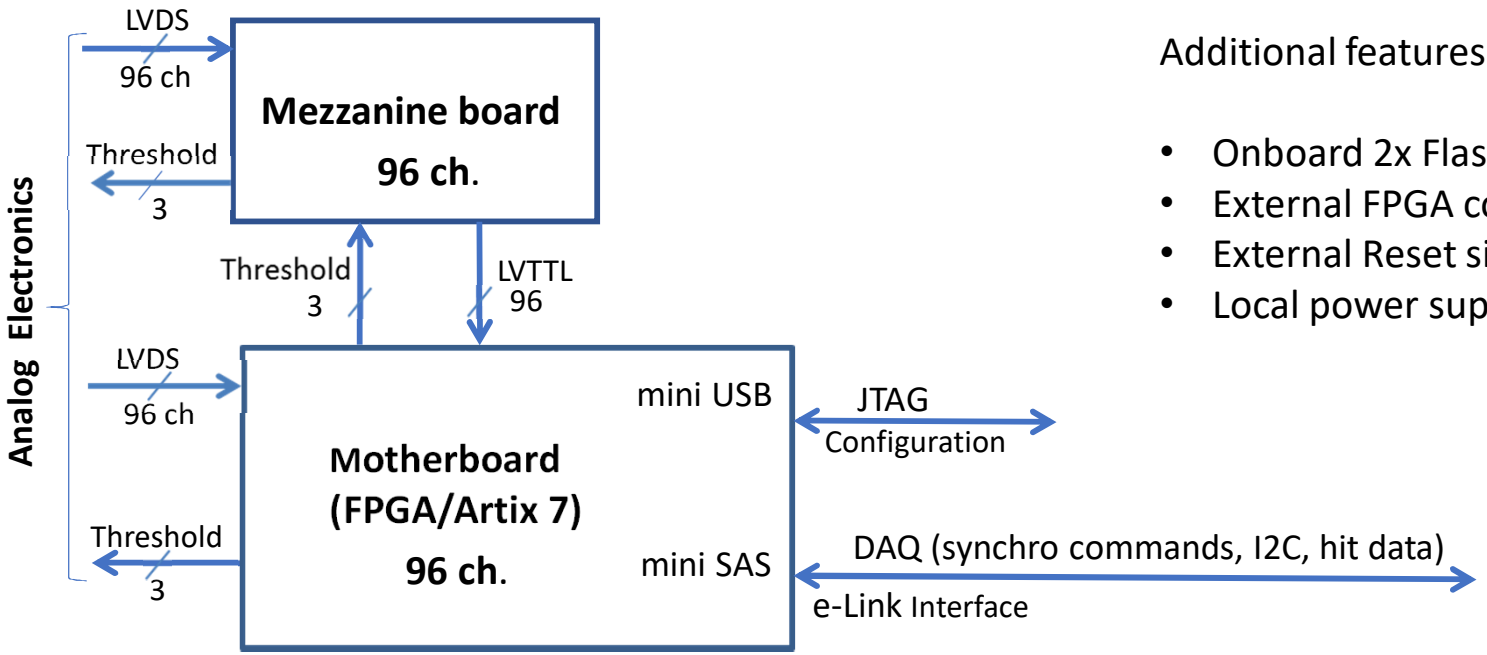
For readout data from the Muon System of the SPD experiment, we are currently developing a digital module FDM-192 based on the FPGA chip with the following technical parameters:

- mechanics - VME 6U 2M
- triggerless mode
- FPGA chip - Xilinx Artix7-200T
- the number registered channels – 192
- signals level from analog electronics – LVDS
- threshold range for input signals – 0 ÷ +3V
- Global Clock – 125 MHz
- discreteness of digitization the time arrival of the hit signal - 4 ns
- data interface – e-Link (LVDS)
- power consumption per unit - ~24W

By now, the module hardware has been developed and manufactured, the firmware is being developed.

FDM-192 UNIT STRUCTURE

Consists of 2 boards:



- Use FPGA as a time digitizer;
- 4ns time difference between “hit”;
- Fast Serial Interface (FSI) connection with DAQ through L1 concentrator (e-Link like);

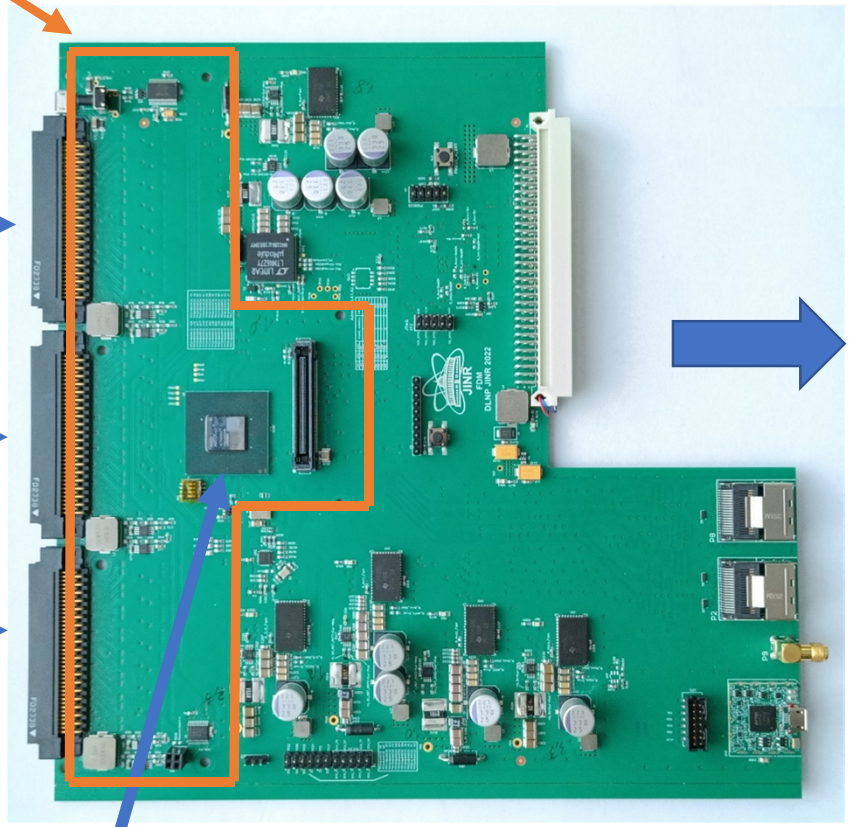
Additional features:

- Onboard 2x Flash Configuration Memory;
- External FPGA configuration loading using FSI;
- External Reset signal;
- Local power supply status self check.

FDM – 192 ch.

Mezzanine card

From Analog electronics

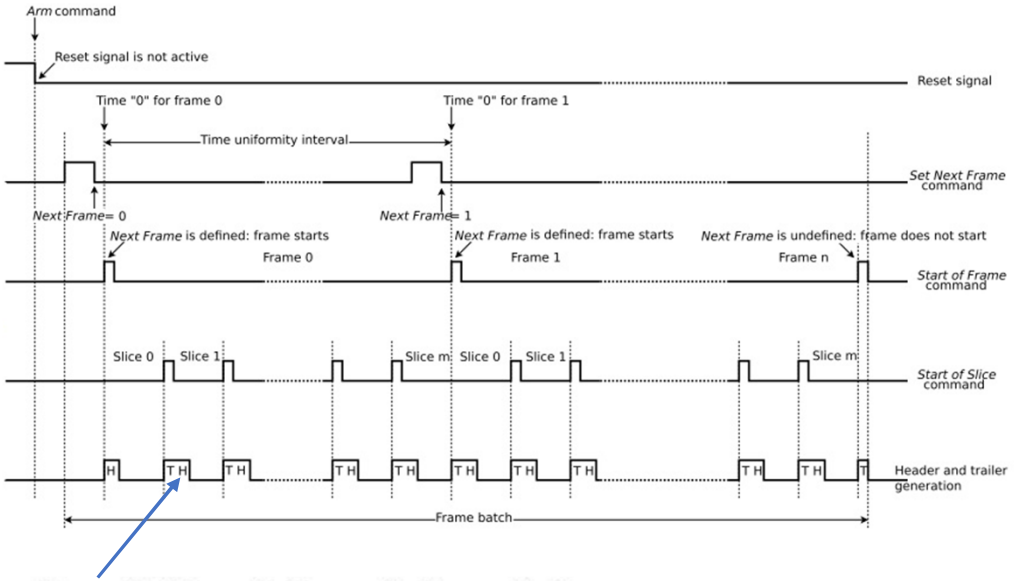


FPGA chip Artix 7

Modified VME CAEN crate 6U
(without bottom part of backplane)

9 x FEE read out FDM to one L1 concentrator

FDM-192 FSI structure



31 28	27 24	23 20	19 16	15
1 0 X X	Format ID	LSB of Frame Number		LSB of Slice Number
0 0 X X	Channel Number		Hit Time	
0 0 X X	Channel Number		Hit Time	
0 0 X X	Channel Number		Hit Time	
...				
0 0 X X	Channel Number		Hit Time	
1 1 X X	Error Code		Total Number of Hits (Data words)	

Data Format

Display Port - > SAS connector

FrontEnd DisplayPort Connector		
Signal Type	Pin Name	Pin
GND	GND	2
Out	ML_Lane 0 (p)	1
Out	ML_Lane 0 (n)	3
GND	GND	5
In	ML_Lane 1 (p)	4
In	ML_Lane 1 (n)	6
GND	GND	8
In	ML_Lane 2 (p)	7
In	ML_Lane 2 (n)	9
GND	GND	19
In	Hot Plug Detect	18
IO	CONFIG1	13
In	CONFIG2	14
GND	GND	11
In	ML_Lane 3 (p)	10
In	ML_Lane 3 (n)	12
GND	GND	16
In	AUX_CH (p)	15
In	AUX_CH (n)	17
	DP_PWR	20

Data e-link

Start of slice

Start of frame

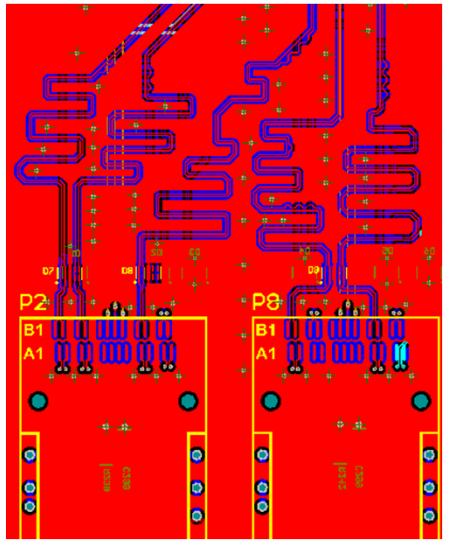
Reset

I2C SDA SCL

Set Next Frame

Global clock

spare signal



- LVDS type differential line
- Up to 1,25 Gb/s data flow
- Equal length for each line

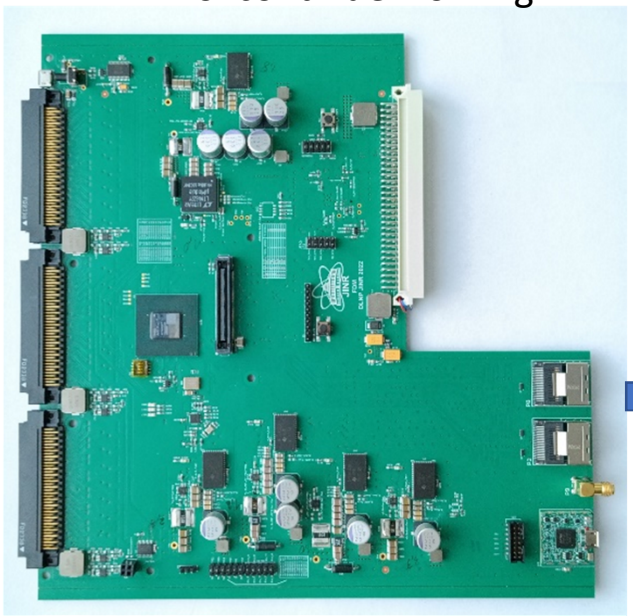
2 types of interface

- Using MGT transivers
- Using SerDes blocks

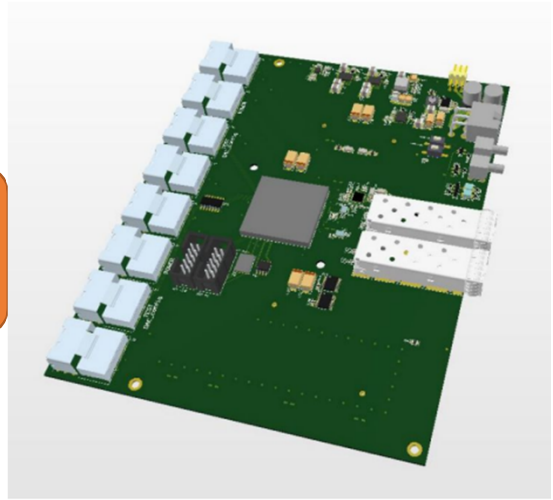
To Do List:

- Establish physical connection between FEE (FDM-192) and L1 concentrator;
- Determine what interface to use: MGT or SerDes;
- Configure protocol algorithm in FPGA from both FEE and L1 sides.

To continue working :



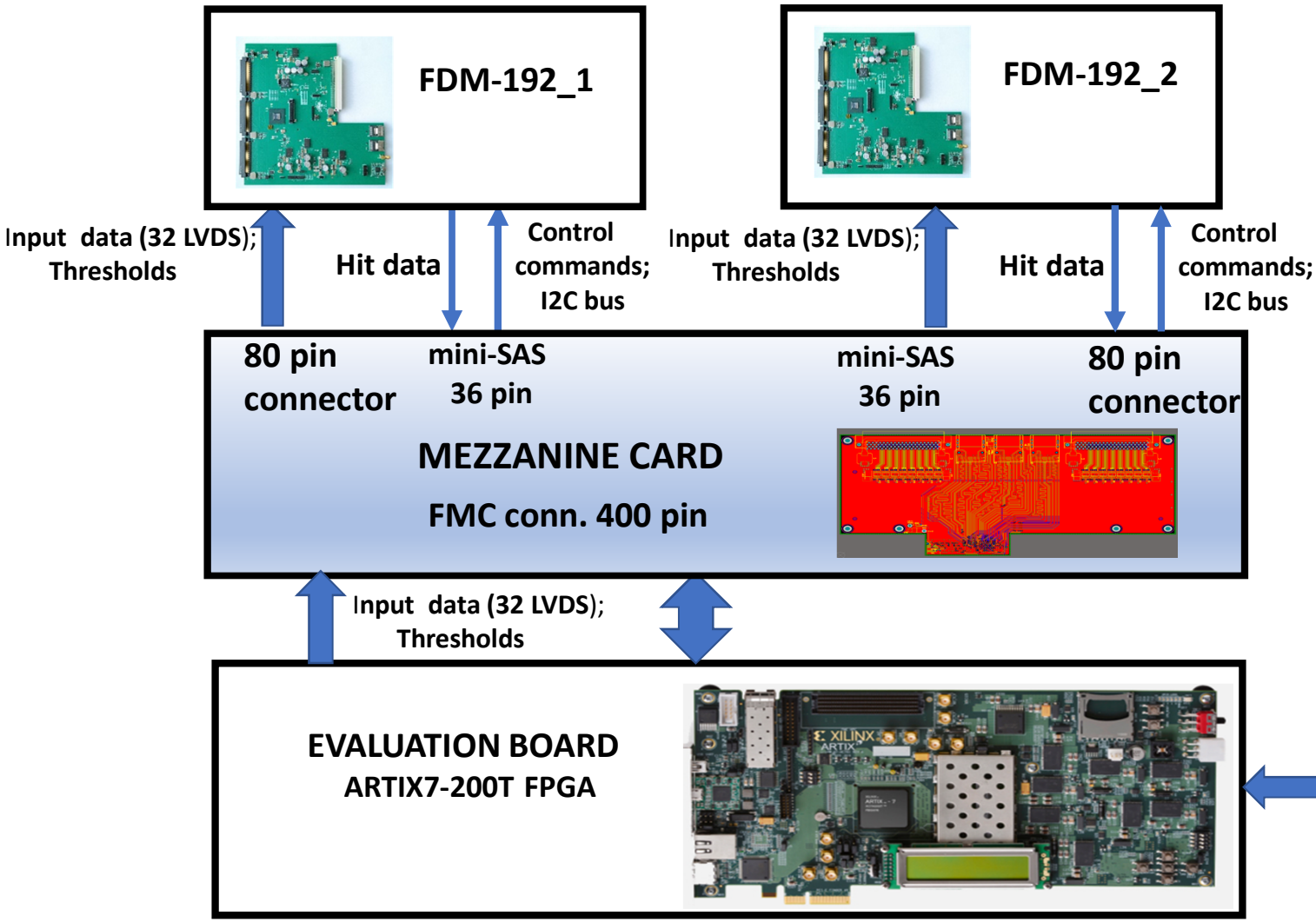
L1 concentrator prototype



Use own test bench

Containing FPGA that can work as L1 prototype

Test Bench structure for FDM-192



Main purpose of the stand:

-development and debugging of the data exchange protocol between FEE and L1 concentrator of the DAQ.
-test of FDM modules.

Thank you for attention!