Status of the L1, L2 concentrators design

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System requirements for the first phase of SPD

- Quantity of e-link (FEE) channels ~ 1100
- Quantity of L1 concentrators (8ch) ~ 140
- Quantity of L2 concentrators (8ch) ~ 20
- Data rate < 20GB/s

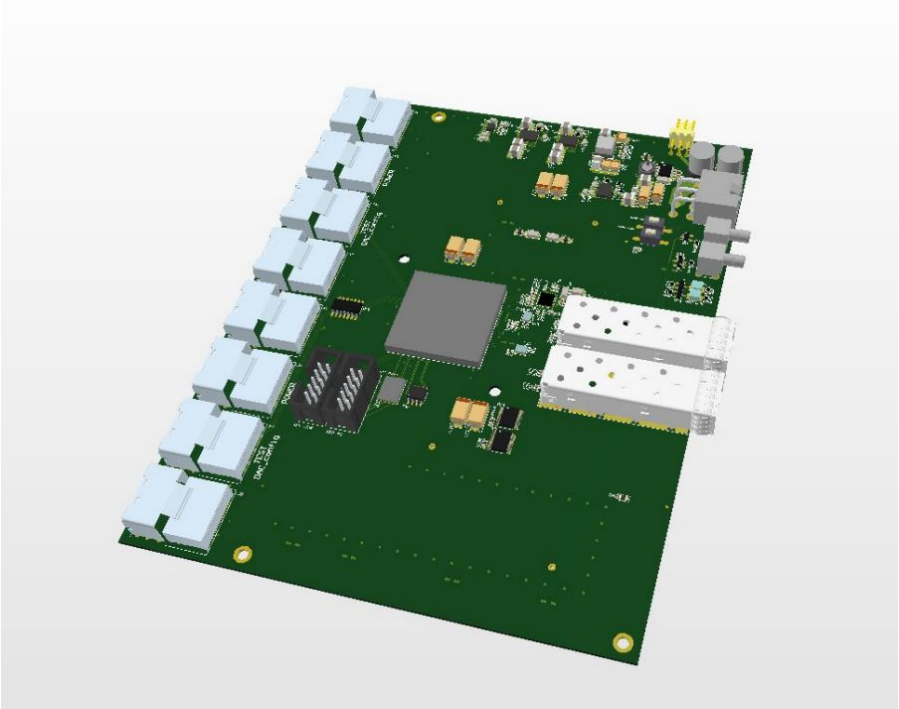
F.e. for RS we need 680 FEE, 85 L1, 10 L2 and up to 3GB/s data rate.

Status of the L1 concentrator board (version 0)

- Cyclone10GX 10CX220YF780I5G
- Quantity of miniSAS connectors - 8

  (64 diff. pairs)
- 1 SFP+ 10Gb data transceiver
- 1 SFP+ (White Rabbit)

Design of the PCB should be completed in May.
Production and test of the board will begin in July.



The possibilities of L2 concentrators' design (iWave version)

- SoC
  - Xilinx (AMD) Zynq UltraScale+ MPSoC
  - Quad Cortex A53@1.5GHz
- Memory:
  - 4GB DDR4 for PS with ECC
  - 8GB eMMC Flash
- On SOM Features
  - 10/100/1000 Ethernet
- Interfaces:
  - PL GTY Transceivers x 16 @ 32.7Gbps
  - PL GTY Transceivers x 32 @16.3Gbps
  - 48 LVDS/96 SE/32

Form Factor: 110mm x 75mm

iW-RainboW-G35M

Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM

Hardware User Guide

Stratix 10 (Intel) SoC FPGA SOM iW-RainboW-G45M®

- Intel’s Stratix 10 SoC & FPGA
- Memory:
  - 8GB DDR4 for HPS with ECC (64bit + 8bit) (Upgradable)
  - 2 x 8GB DDR4 for FPGA (64bit + 64bit) (Upgradable)
- Interfaces:
  - Upto 16 GXT Transceiver Channels up to 28.3Gbps
  - 32 GX Transceiver Channels up to 17.4Gbps
- Form Factor: 110mm x 75mm

Agilex 7 SoC FPGA SOM iW-RainboW-G43M®

- Quad ARM Cortex A53 Processor
- Memory:
  - 32GB eMMC (Expandable)
  - 8GB DDR4 with ECC for HPS (64bit + 8bit)
  - 2 x 8GB DDR4 with ECC for FPGA (64bit + 8bit)
- Interfaces:
  - 64 x FGT transceivers up to 58Gbps
  - 8 x FHT transceivers up to 116Gbps

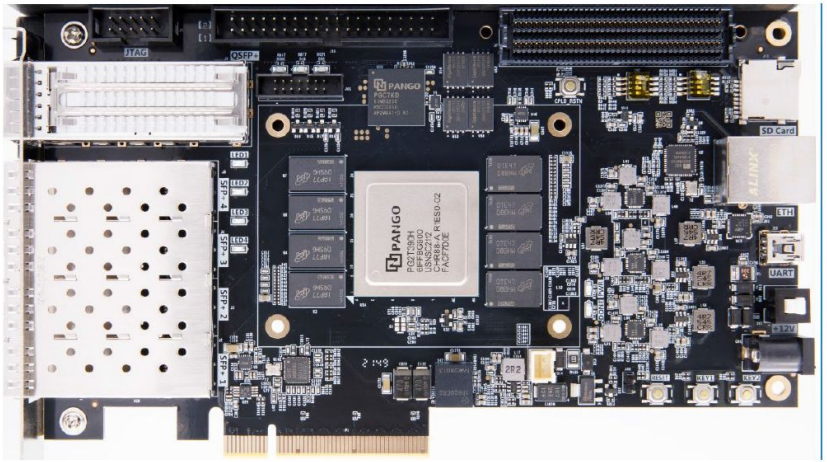
The possibilities of L1, L2 concentrators’ design (Chinese version)

Titan2 FPGA It adopts the second-generation new high-performance 28nm FPGA chip PG2T390HFFBG900 of the Titan family launched by Shenzhen Ziguang Tongchuang Electronics Co., Ltd. (PangoMicro)

Memory: DDR4 With 4 high-capacity 2GB (8GB total) high-speed DDR4 SDRAM.

Interfaces: 16 Transceivers HSST (Supports Data Rates up to 12.5Gbps), PCIe 2.0 x8

IP is free. Price for board - 1518 $



AXP390 Products

AXP100 FPGA development platform for L1 concentrators

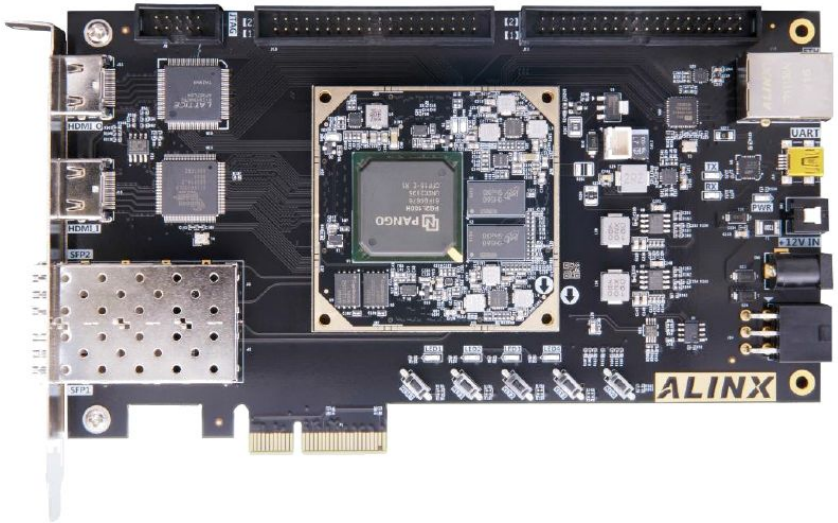
Logos2 FPGA core board PG2L100H

It consists of PG2L100H+8Gb DDR3+128Mb QSPI FLASH

Two-way SFP high-speed optical fiber interface up to 6.6Gb/s.

Max Diff IO (pair) - 240

A possible option for the L1 concentrator board



Thanks for your attention

Backup

SPD detectors' outputs (at the first stage)

Sub-detector	Information type	Number of channels	Channels per FE card	Number of e-links
Micromegas	T + A	~15000 (25600)	128	118 (200)
Straw tracker	T + A	30208	128	236
BBC (inner+outer)	T + (T + A)	256 + 500	32	8 + 12
Range System	T	130200	192	679
ZDC	T + A	1050	64	17
Total (max)		177214 (179598)		1070 (1152)

SPD readout chain