SPD COLLABORATION MEETING
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JINR, DUBNA

Development of an ASIC for Straw and MicroMegaS detectors of SPD NICA

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NICA-SPD Straw Tracker
Summary table of straw detector parameters

Detector type	barrel	end-cap
Detector tasks	dE/dx	xy coordinates, dE/dx
Working mode	triggerless	triggerless
Detector inner diameter, mm	540	
Detector outer diameter, mm	1700	
Number of layers	30 (double layer)	2x, 2y, 2u, 2v
Number of stations, sections	8 sections	12 stations
Number of channels	32288	8192
Tube diameter, mm	10	10
Maximum tube length, mm	2400	1700
Central core diameter, mm	0.03	0.03
Maximum detector capacitance, pF	26	18,5
Gas detector	70 Argon, 30 CO_2	70 Argon, 30 CO_2
Operating voltage, V	+1650	+1650
Multiplication factor, HV=1750	4.5E4	4.5E4
Charge from the first electron, fC	7.7	7.7
Electron drift velocity, μm/ns	65	65
Electron drift time, ns	120	120
Ion drift time, μs	100	100
Spectral resolution, μm	150	150
Maximum load, kHz per tube	150	

Micromegas central tracker (MCT)
Summary table of micromegas detector parameters

Detector tasks	xy coordinates method of weighted amplitude channel
Working mode	triggerless
Detector inner diameter, mm	54
Number of channels on the inner layer	728
Detector outer diameter, mm	188
The composition of the gas mixture (mobility of CO2+ ions 1.72	70 Argon, 30 CO2
Anode capacity, pF	20÷200
Gap between cathode and grid, drift area, mm	5
Gap between grid and anodes, multiplication area, um (n is the number of layers of the photoresistor, the optimal value is n=2)	n*64
Multiplication factor	10000
Time of the electronic component in the drift region, us	2
Time of the electronic component in the multiplication region,	1÷2
Time of the ion component of the signal, ns	30÷140
Loading per channel, kHz	10÷100
Anode width, um	150÷300
Anode length, cm	до 100
Electrode potentials, V: cathode/grid/anode (capacitive	-350/0/+550
Design features	Charge distribution between 3÷5 anodes

Parameter accommodation for both straw and micromegas detectors

Parameter	straw	micromegas	Notes
Optimal number of channels	32 Channels step: 10 мм	32 Channel steps: 400 μm On the inner radius up to 502 channels or 16 chips	
Minimum number of channels	8	32	
Fast channel shaping time, ns	6÷10	6÷10	Enough 8 bits
Slow channel shaping time, ns	150	150, 250, 400	
Time resolution, ns	1	<5	
Amplitude resolution, bit	8÷10	8÷10	
ADC, bit	8÷10	8÷10	
Gain, mV/fC	1÷4	4÷10	Straw has 3 times more multiplication

AST-SPD chip specification

Detector parameters		
Range of input charges, fC	+/-(0÷1000)	
Detector channel capacitance, pF	20÷100	
Loading per channel, kHz	150	
Working mode	triggerless	
Common chip parameters		
Technology	CMOS, 180 nm	
Number of channels	32	
Supply voltage, V	1.8	
Power dissipation, mW/ch	10	
Fast, time channel parameters		
Fast channel shaping time, ns	6÷10	
Time channel resolution, ns	1	
Discriminator threshold adjustment, fC	15	
ENC (r.m.s.), e Cd=60pF	<3000	
TAC time window, ns	500÷5000	
Parameters of the slow, amplitude channel		
Slow channel gain, mV/fC	straw	micromegas
	1/3	3/9
Slow channel shaping time, ns	straw	micromegas
	75/150	250/400
Base signal width, ns	300/600/	1000/1600
Shaper order	4	
ADC capacity, bit	10	
ENC (r.m.s.), e Cd=60pF	<3000	

Development stages of the AST-SPD chip

1) Circuit design and simulation of the AST-SPD Terms of work: from 01/09/2022 to 30/04/2023

2) AST-SPD topology development
Terms of work: from 01/05/2023 to 31/03/2024

3) Manufacturing of wafers with AST-SPD chips of the first iteration
Terms of work: 01/01/2024 to 12/20/2024

Wafer production is possible at semiconductor factories: X-FAB (Germany), Mikron (Russia)

AST-SPD chip development status

As part of the first stage, the following work was carried out:

1) the functional blocks of the chip are designed and modeled;

2) the structure of the channel of the chip is chosen;

3) functional modeling of the channel is performed.

Designed functional blocks

Analog blocks:
CSP - Charge Sensing Amplifier
FS - fast shaper
SS - slow shaper
PD – peak detector
S&H– sample and hold
MUX – analog multiplexer
IREF – Current Reference&StartUp
VREF – Voltage Reference

Analog-digital blocks:
Dis – discriminator
TAC - time-to-amplitude converter
SAR ADC - Serial ADC

Digital blocks:
MUX control block
sLVDS - low-voltage LVDS receiver and transmitter
Configuration register

Now we can proceed to the second stage of work, that is, to the development of the topology of functional blocks.

Optimized chip channel structure

<table>
<tr><td rowspan="2">CSP</td><td>FS</td><td>Dis</td><td>TAC</td><td rowspan="2">MUX
2:1</td><td rowspan="2">SAR ADC</td></tr>
<tr><td colspan="2">SS</td><td>PD</td></tr>
</table>

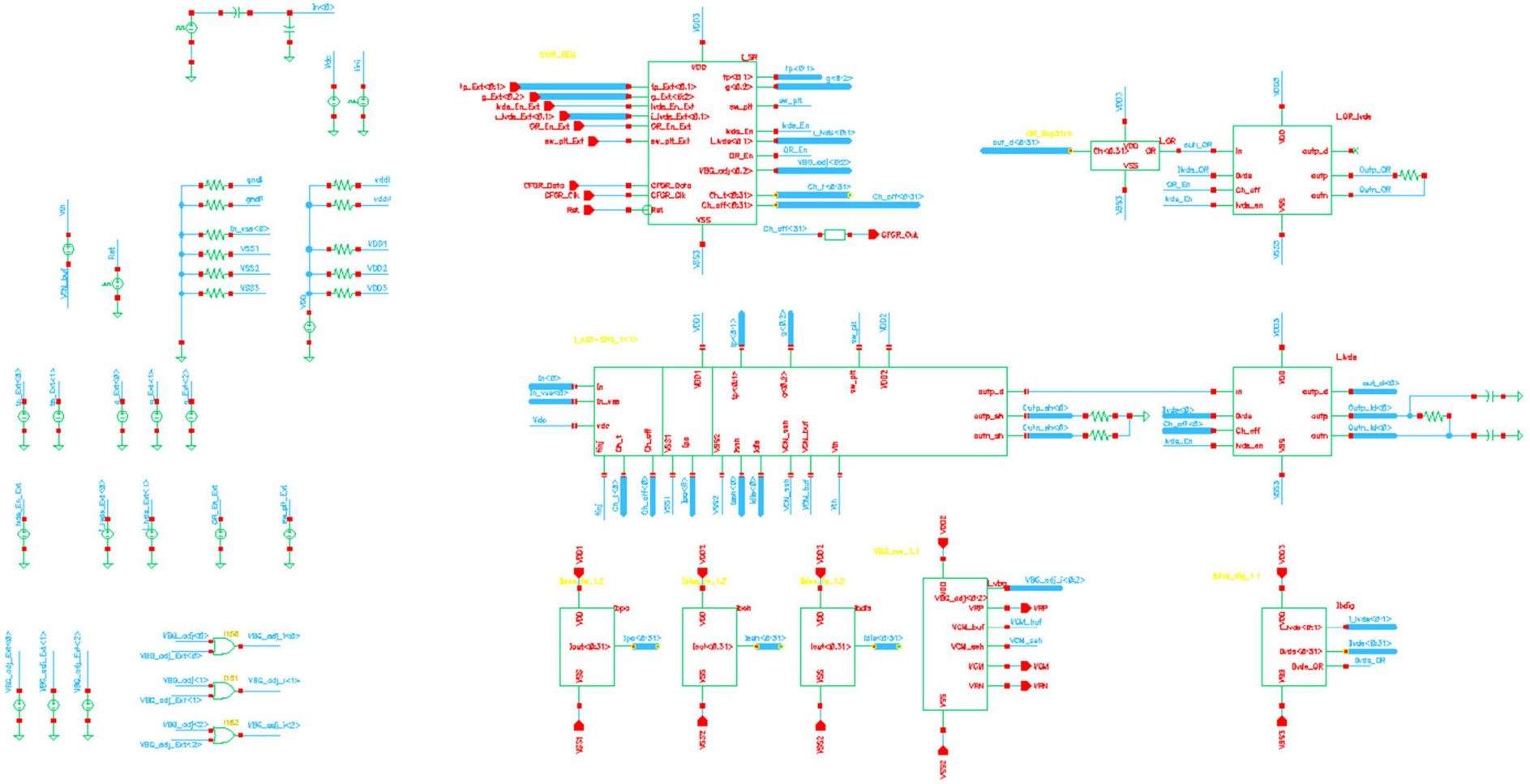
One SAR ADC per channel
Event digitization time up to 250 ns

Channel optimization criteria:
1) event rates
2) dead time
3) power dissipation
4) chip area

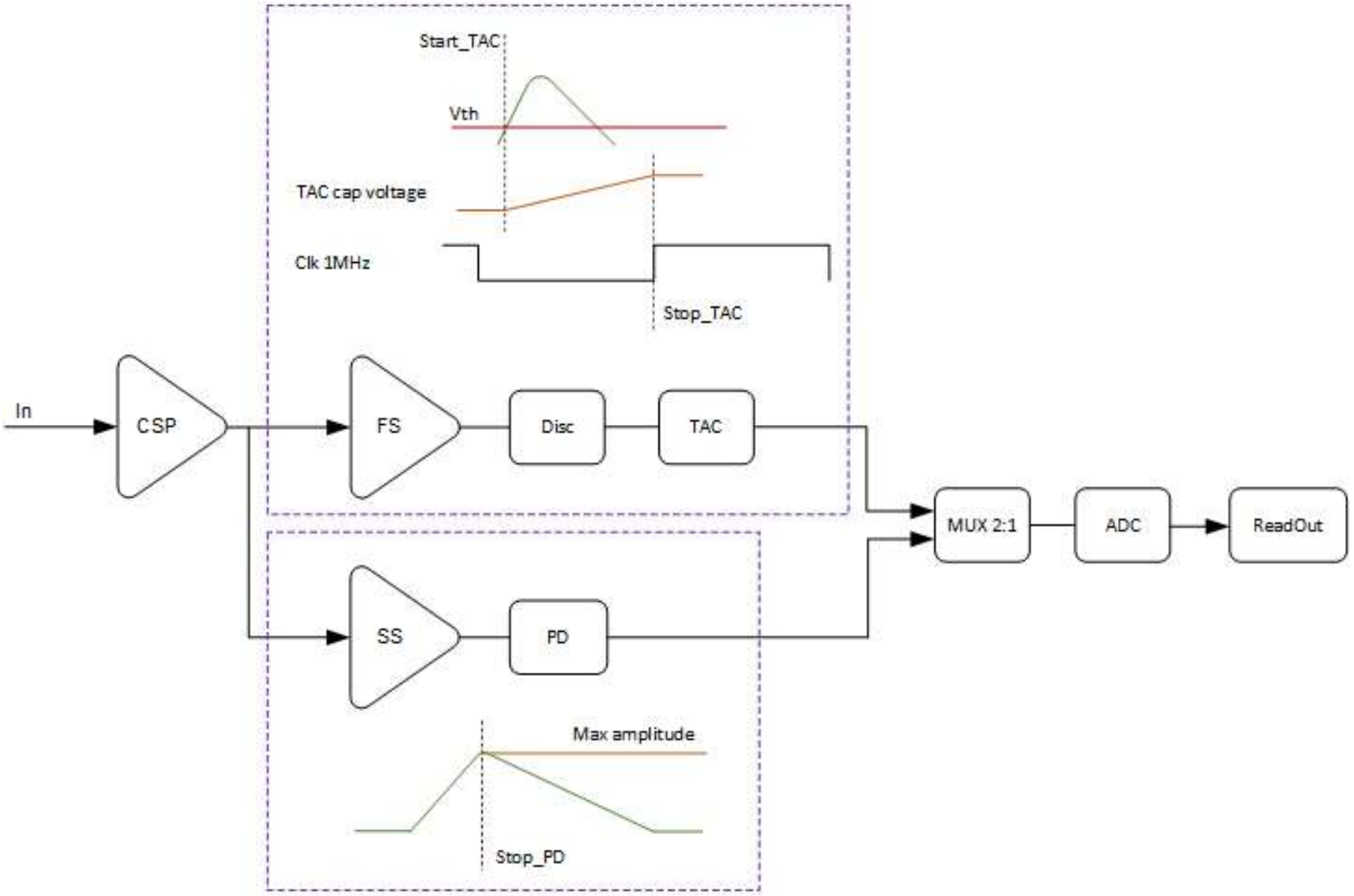
Block	CSA	FS+Dis	SS	PD	TAC	MUX	SAR ADC
Power dissipation, mW	1.5	1	1	1	0.25	0.5	3

Total: 8 mW/channel

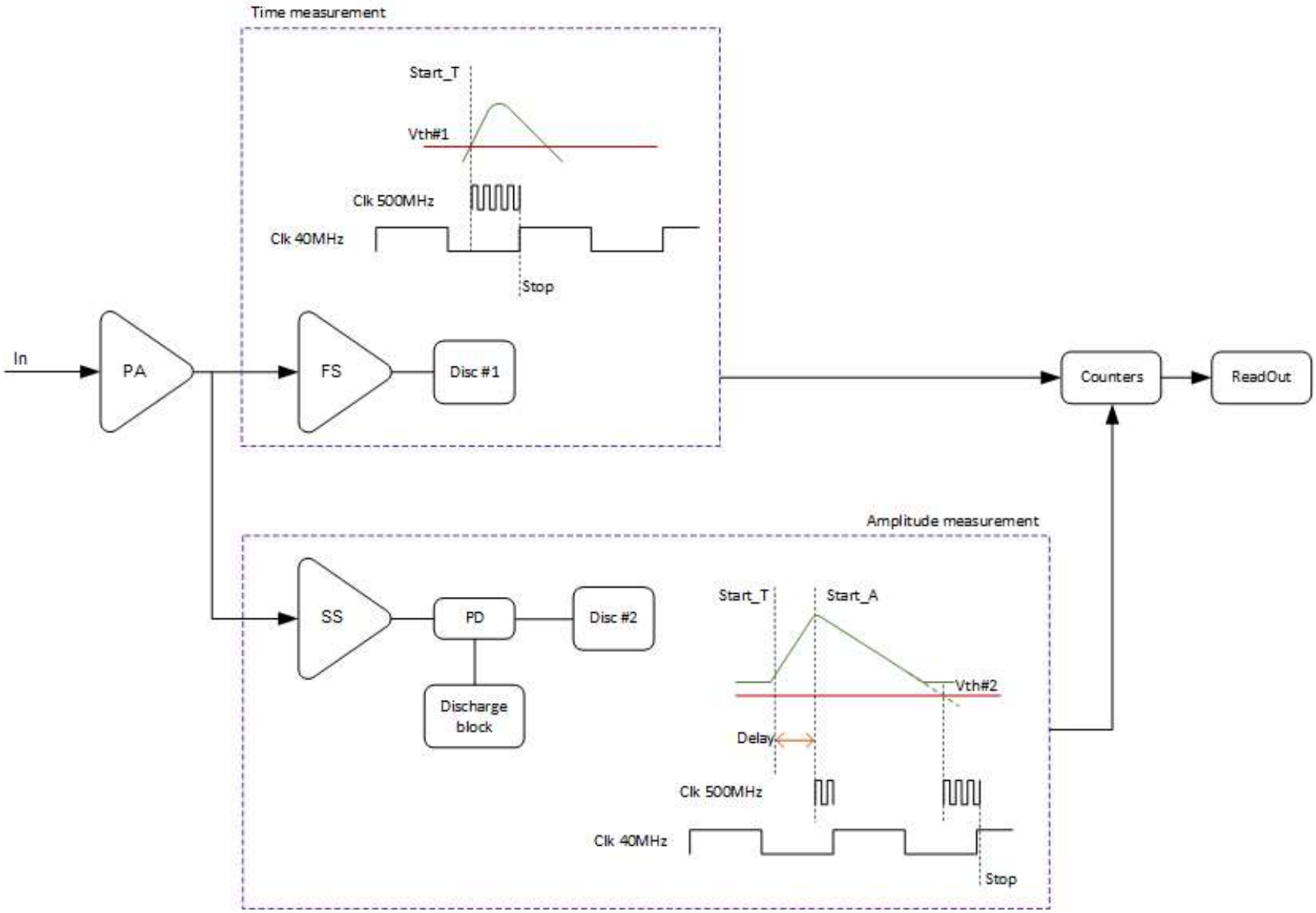
Test bench for modeling the AST-SPD channel



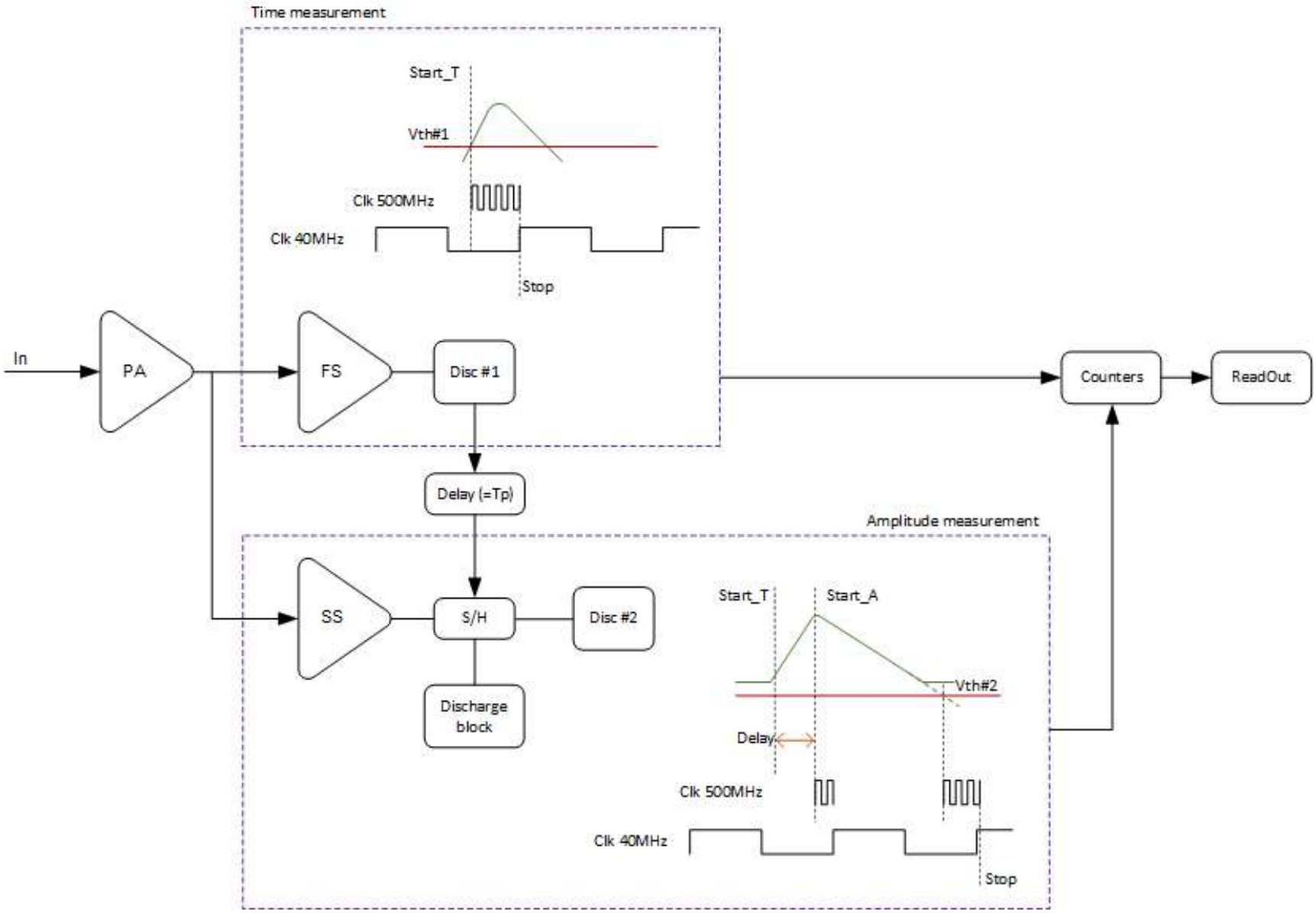
AST-SPD chip block diagram



Block diagram of the TDC version of the AST-SPD chip
with peak detector

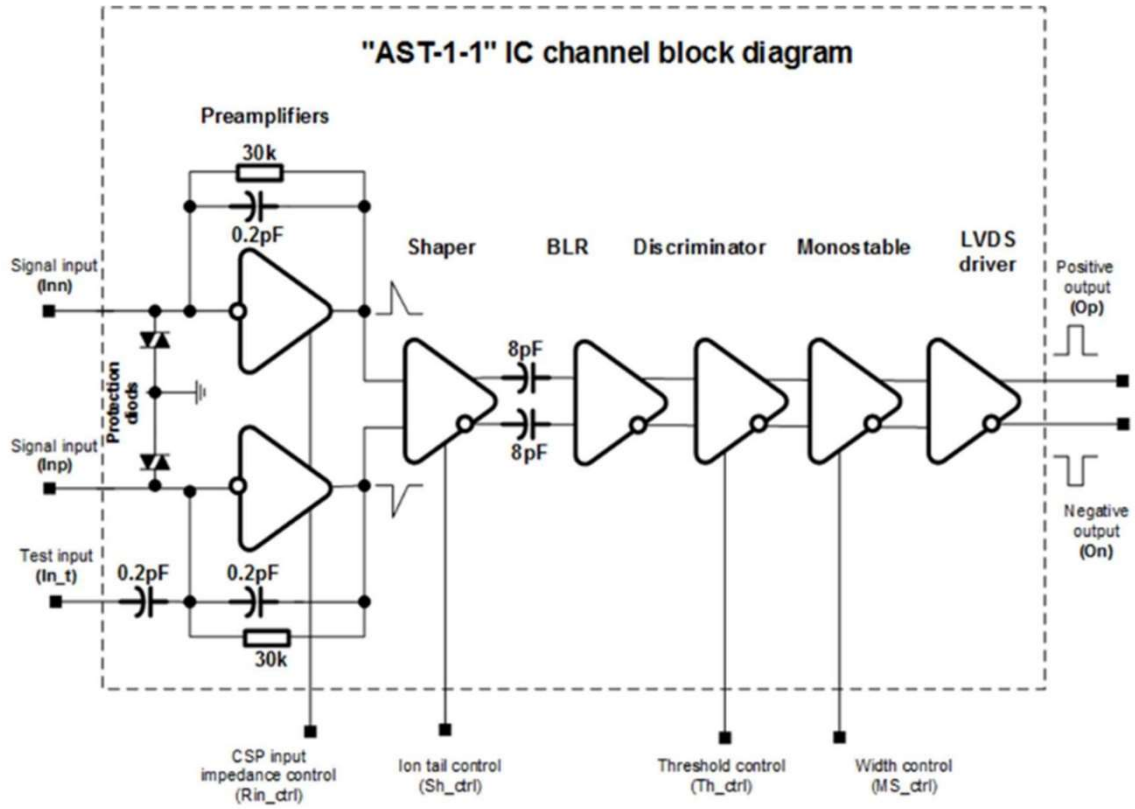


Block diagram of the TDC version of the AST-SPD chip
with sample and hold



Straw detector chip version based on AST-1-1 ASIC

A front-end called AST-1-1 ASIC was developed for the straw detectors of the CBM experiment. This chip is currently used in the straw detectors of the NA64 experiment and one of the silicon detectors of the BM@N experiment.



Upgrade option: add a slow shaper to the channel, analog signals from which are digitized with a cheap commercial eight-channel ADC