National Research Tomsk State University

L2 concentrator firmware. Current status

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On behalf of TSU electronics group

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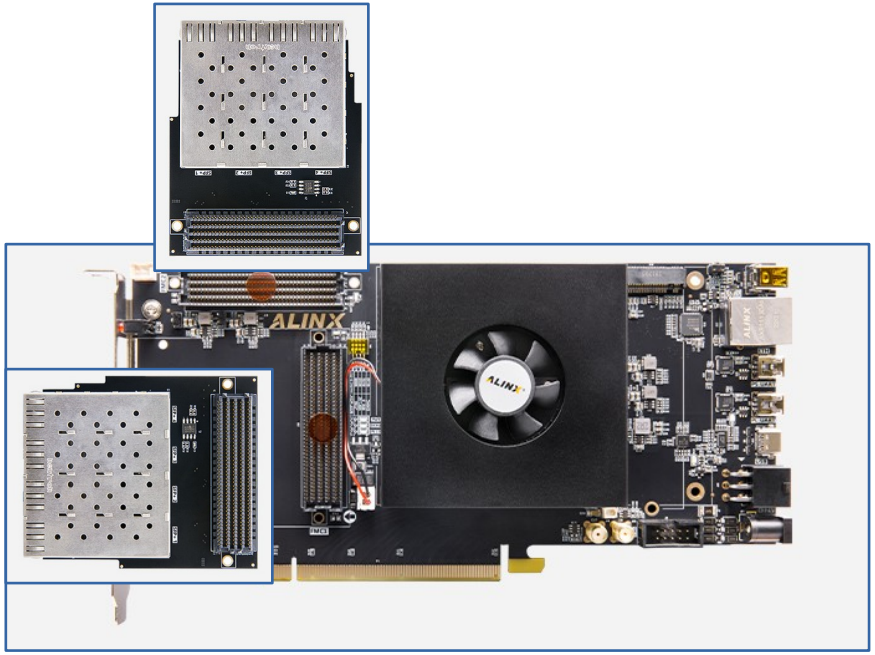
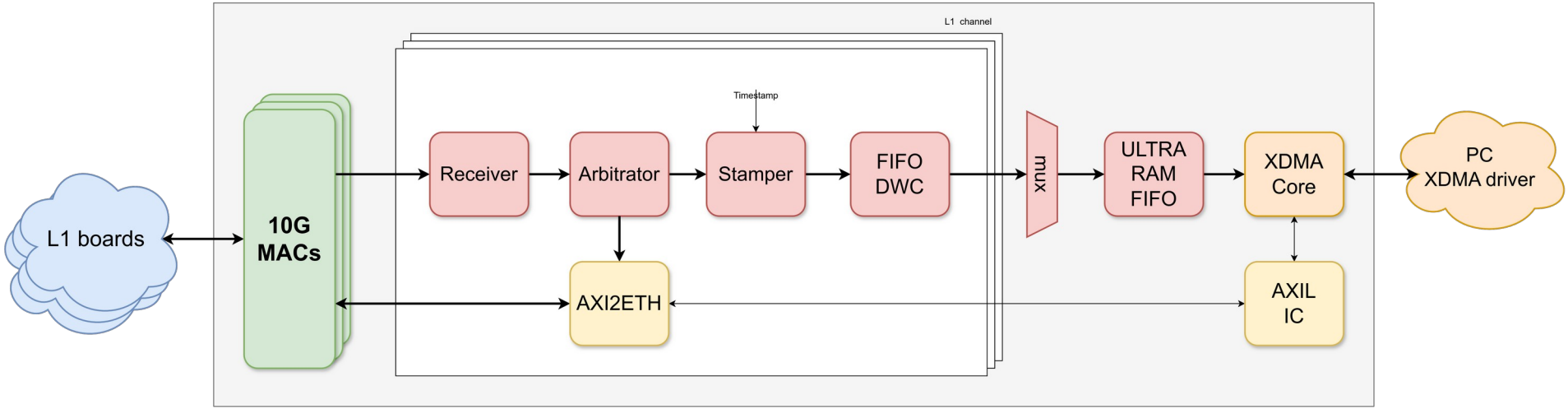
Platform



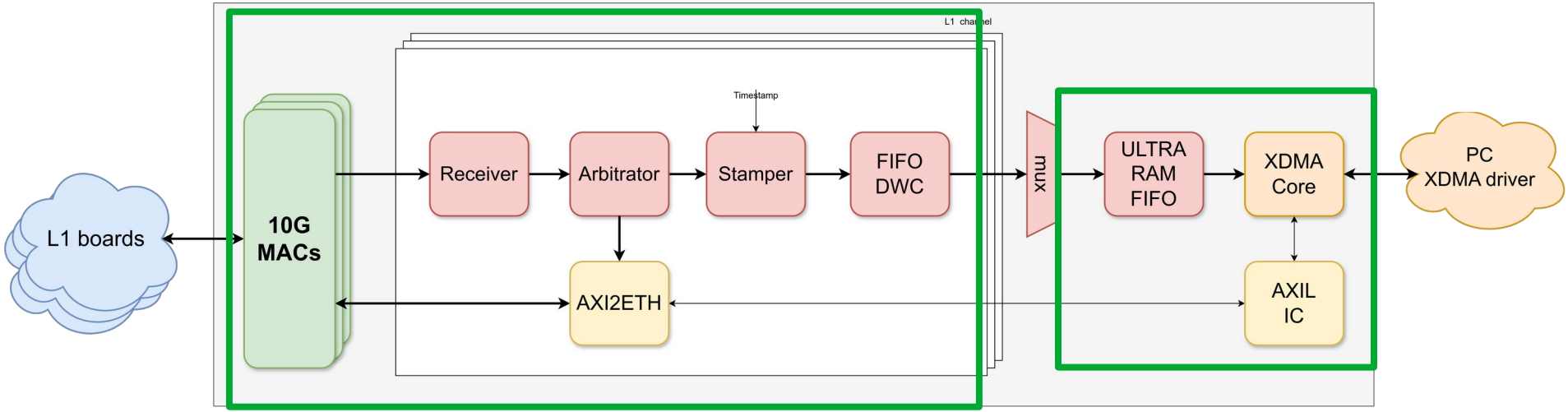
- Full setup based on Alinx Z19-P board
- Up to 8 10G SFP channels (L1 links/boards)
- PCIe Gen 3.0 x16
- MPSoC XCZU19EG chip

We expect delivery two of these board plus 4 mezzanines with 8 SFP modules each in December

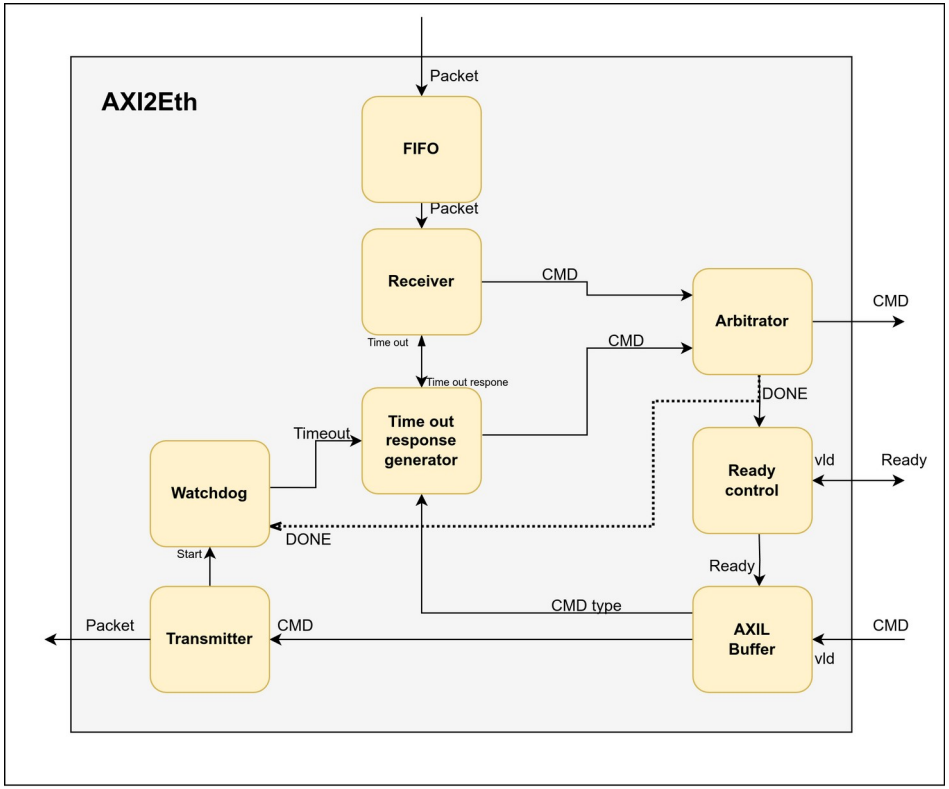
L2 FPGA architecture



L2 FPGA progress



AXI-Ethernet transport



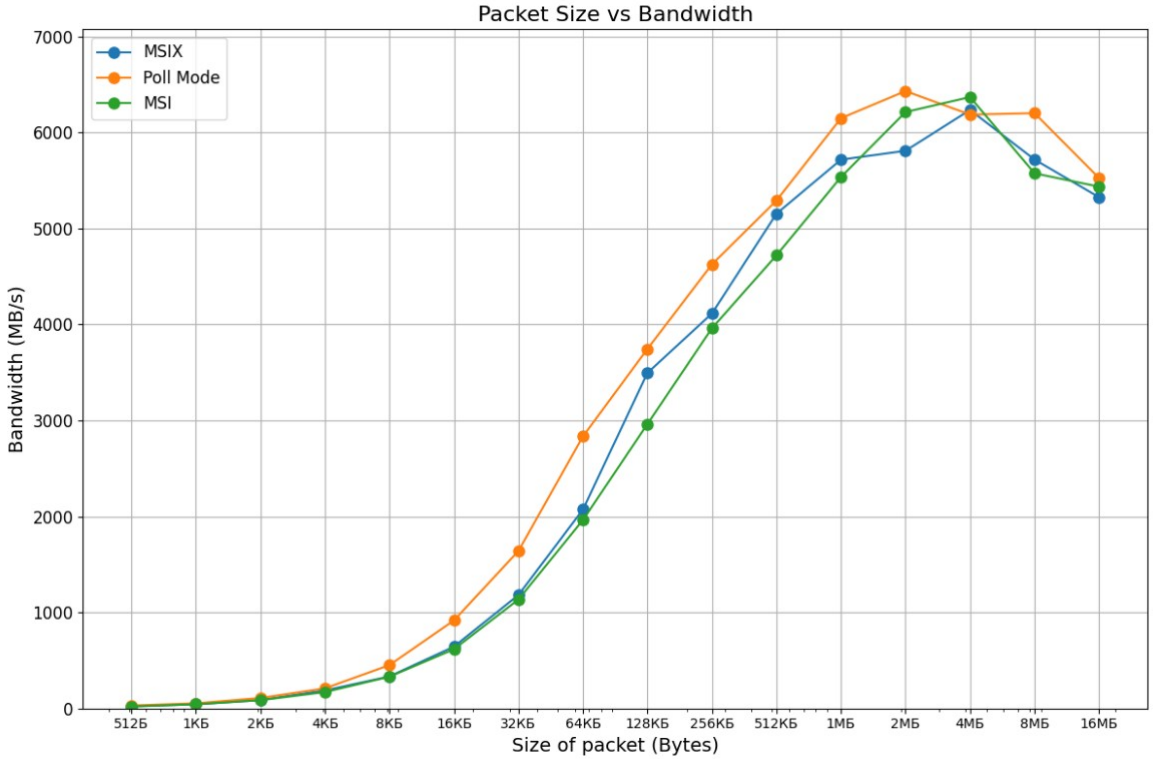
AXILite to Ethernet transport

Sent AXI Lite command to L1 and receive responses

It needs to be aligned with firmware of L1 (A. Boikov)

Simple kick-off design for ZU19-P board is prepared:
https://git.jinr.ru/spd/DAQ/l2-hub-alinx/-/tree/eth2axi

PCI C2H bandwidth



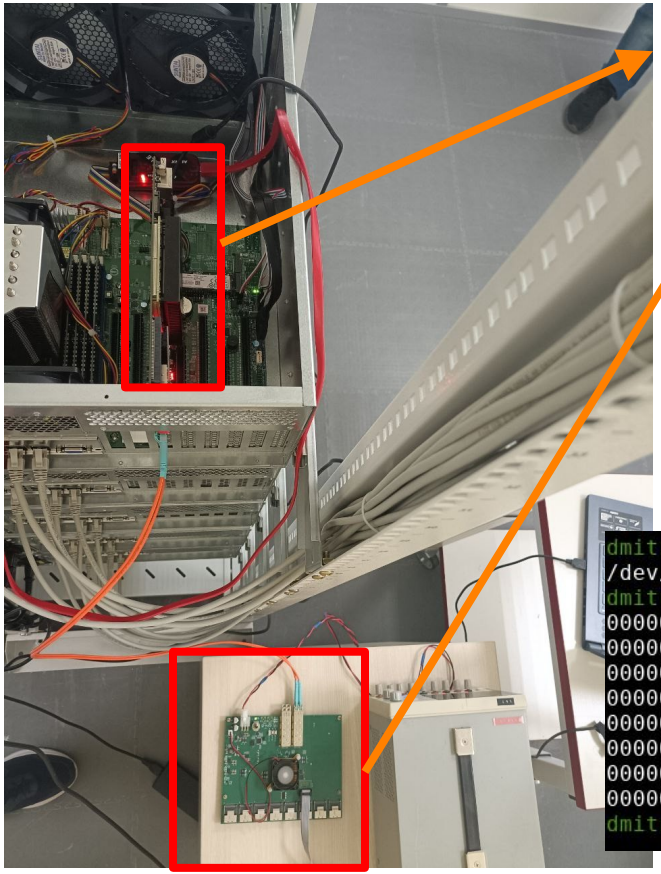
PCIe 3.0 x16 has maximum throughput up to 15.754 GB/s

We observe ~half of it.

The issue is under investigation…

… but it's still enough for 7-8 channels of L1

L2-L1 joint. Preliminarily results.



During visit to JINR Andrey and Dmitrii ran joint between L2 and single L1 board.

Packets are transmitted via full chain:
L1 → fiber → L2 → PCIe → Server

This is not real data stream, but a few test packets. But we lock the chain.

```
dmitrii@srv5:~/tools_git/tools$ sudo ./dma_from_device -s 122 -c 1 -f /test.hex
/dev/xdma0_c2h_0 ** Average BW = 122, 1.557871
dmitrii@srv5:~/tools_git/tools$ xxd /test.hex
00000000: 4500 0422 056a 0000 ff11 30f8 c0a8 0008  E.."j....0.....
00000010: c0a8 0010 6090 6090 040e 0000 0000 4441  ....`.`.......DA
00000020: 5441 eeee eeee ffff ffff eeee eeee ffff  TA..............
00000030: ffff eeee eeee ffff ffff eeee eeee ffff  ................
00000040: ffff eeee eeee ffff ffff eeee eeee ffff  ................
00000050: ffff eeee eeee ffff ffff eeee eeee ffff  ................
00000060: ffff eeee eeee ffff ffff eeee eeee ffff  ................
00000070: ffff 0000 000c baad dbba                 ..........
dmitrii@srv5:~/tools_git/tools$
```

Ongoing work

- Scale the firmware to 4/8 channels;
- Investigate issue with PCIe speed, I'd like to understand, what's wrong with it even if the speed is enough;
- Wait for new evaluation boards for test setups in Tomsk and/or Dubna;
- Primitive API for L2 concentrator for control registers and DAQ tasks;
- Integration of fw and sw with experiment: verify joint with L1 and DAQ software;
- We expect additional 3 FPGA students since next semester. All of them will pass through Digital Design School. And all of them will start their Master or Bachelor theses in HEP Electronics.

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Thanks for your attention

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