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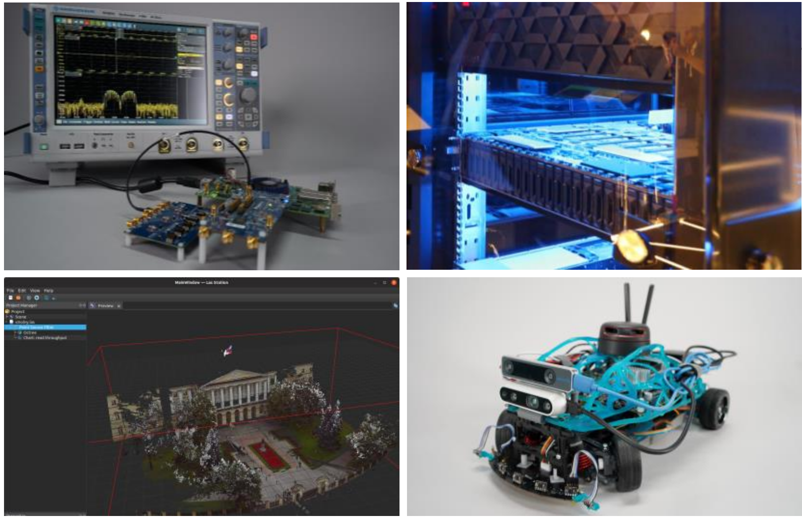

SPD-meeting

November 5th 2024

Current status of TSS development. White Rabbit precision and accuracy

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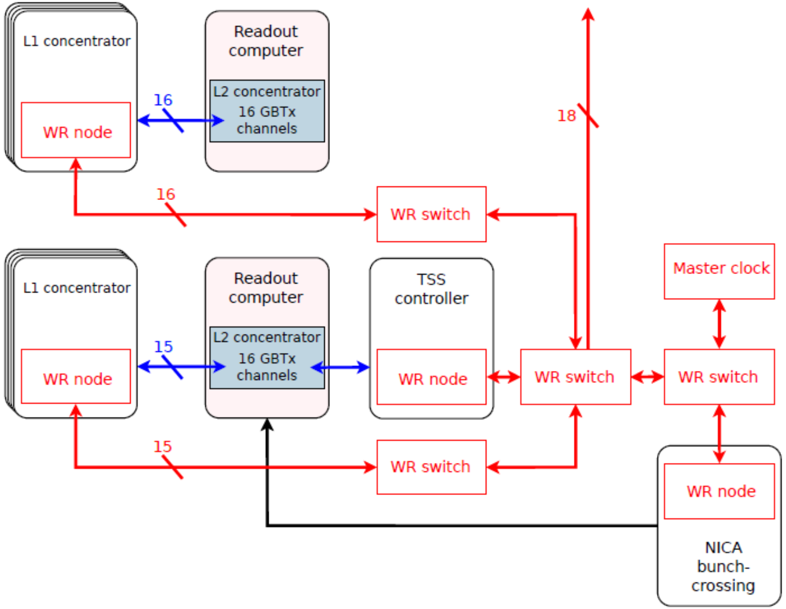
Industrial Systems for Streaming Data Processing Laboratory,
“Digital Engineering” Advanced Engineering School, SPbPU

Presentation brief

- Refresher on TSS subsystem, precision and accuracy requirements
- White Rabbit calibration primer + automation method
- White Rabbit precision and accuracy evaluation results
- Current development work and prospects

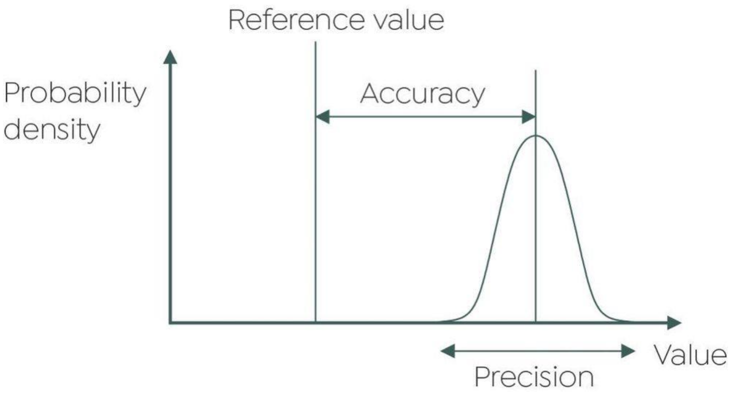
Time Synchronization Subsystem (TSS) with White Rabbit



1. **Provides the global clock and time** for the SPD DAQ
    - WhiteRabbit PTP (high accuracy profile of the IEEE1588-2019) – standard open protocol developed and maintained by CERN
    - Expected accuracy is better than 1 ns
2. **Generates and distributes synchronous commands** to mark data frames and slices
    - Run Control sends Start/Restart, Stop and Abort commands to TSS controller
    - The TSS controller generates a schedule
    - TSS nodes (at L1) receive this schedule and generate synchronous commands to front-end electronics

What is accuracy and precision

After initial synchronization WR node tracks the global clock and maintains the equal frequency of the local clock.



Accuracy as average clock skew:

$$\overline{\Delta t} = \frac{1}{M}\sum_{i=1}^{M}\left(t_{ref} - t\right)$$

Precision as relative rms jitter:

$$\sigma_N = \sqrt{\frac{1}{M-1}\sum_{i=1}^{M}\left(\Delta t_i - \overline{\Delta t}\right)^2}$$

SPD requires:

< 1 ns

< 50 ps

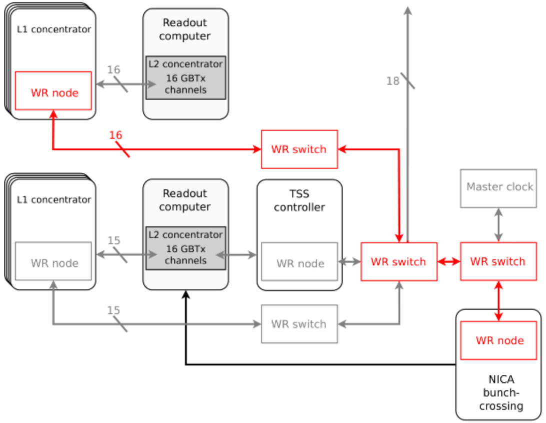
- Sub-nanosecond accuracy can be achieved after calibration.
- Jitter depends on the hardware and environment.

Calibration

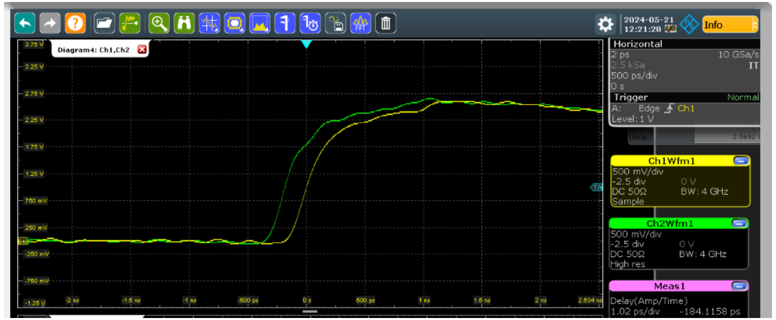
Calibration of WR devices significantly decreases relative skew between clock signals of calibrated devices.

Each different pair of devices’ ports
[and each cable type] should be calibrated

Measurements with Rohde & Schwarz RTO2044
- in room temperature conditions
- 20 GHz sample frequency



- Recalibrated SyncTechnology WR switches and nodes
- Reference clock: 10 MHz clock
  from top-level WR switch’s internal oscillator
- Topology represents TSS network structure



2024-05-21
12:21:28

Horizontal
2 ps 10 GSa/s
2.5 kSa IT
500 ps/div
0 s

Trigger Normal
A: Edge Ch1
Level: 1 V

Amp. 2.5692 V

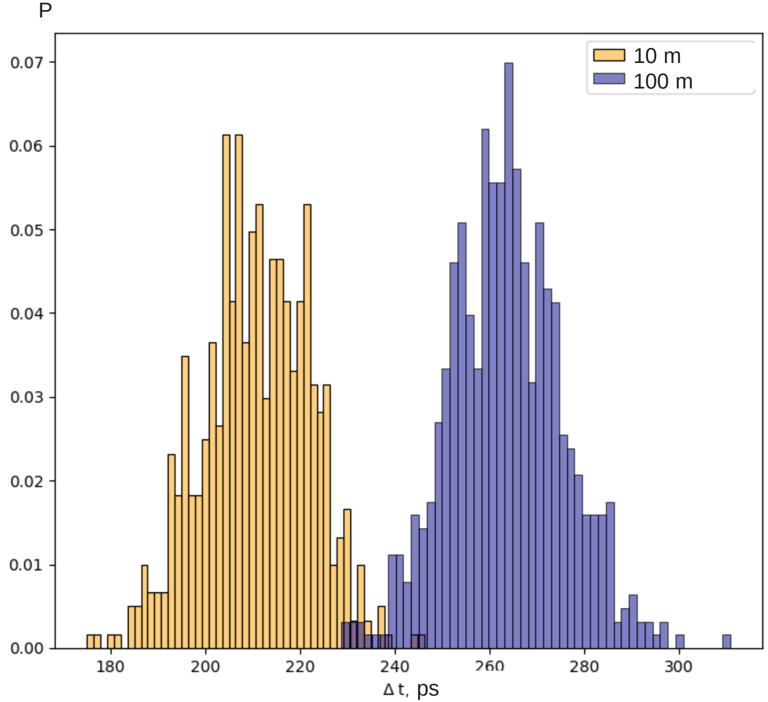
Ch1Wfm1
500 mV/div
-2.5 div 0 V
DC 50Ω BW: 4 GHz
Sample

Ch2Wfm1
500 mV/div
-2.5 div 0 V
DC 50Ω BW: 4 GHz
High res

Meas1
Delay(Amp/Time)
1.02 ps/div -184.1158 ps

Cable length effects
Can we omit optical cable calibration?

WR automatically tracks clk phase deviations
- Automatic compensation for different cable lengths
- Regular calibration includes fiber asymmetry (α) estimation



Our motivation:
- up to 200 WR-nodes
- long life-cycle of SPD experiment
- maximum cable length 100 m

Experimental results:
- for 9/125 simplex single mode 3.0mm optical cable
- no more than 50 ps/100 m clk skew change

We can significantly reduce TSS deployment time.

Calibration procedure automation

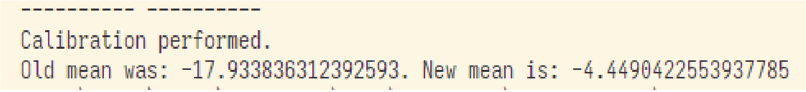
based on “White Rabbit. Good Practice Guide”
Motivation: calibration of one end point is a repetitive manual process, takes around 30 min

Method: automated RX and TX calibration presets refinement.
Requires:

- manual oscilloscope probes connection (RTO2044)
- remote LAN connection to oscilloscope
- remote LAN connection to end node

Python script performs:

- automated measurement of the current relative PPS skew
- repetitive PTP restart
- estimation of the required delay correction
- remote end node’s delays reconfiguration
- verification of calibration



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Calibration performed.
Old mean was: -17.933836312392593. New mean is: -4.4490422553937785
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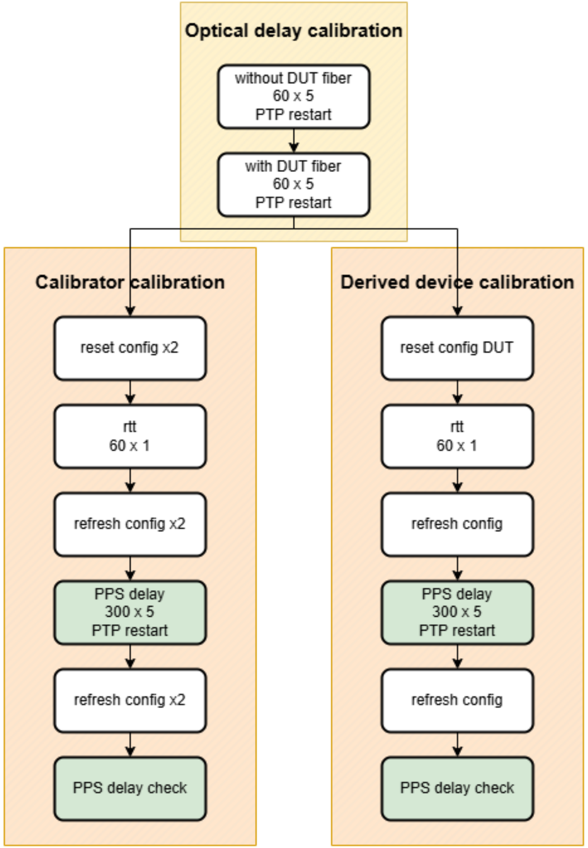
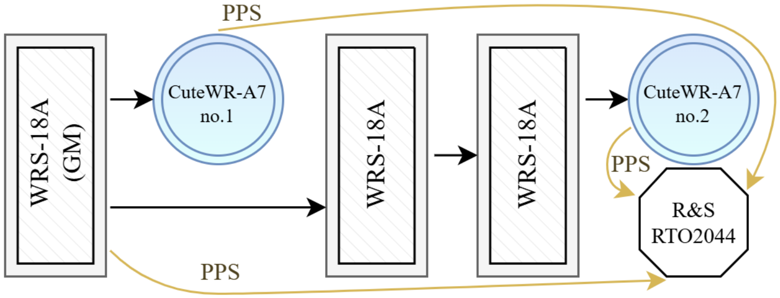


Measurement setup and expected clk characteristics

SyncTechnology devices
RTO2044 Delay measurement function
Sampling mode: 20 GHz, linear interpolation
Signals: PPS (50% levels)



Required jitter measurement correction: 0.3-0.2 ps

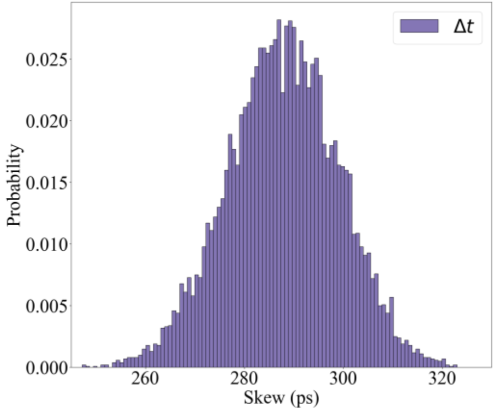
$$\sigma_{Ncor} = \sqrt{\sigma_N^2 - \sigma_{ITJ}^2 - \left(\frac{\sigma_{IF_{SW}}}{S_{SW}}\right)^2 - \left(\frac{\sigma_{IF_N}}{S_N}\right)^2}$$

WR clk jitter

- has complex nature
- strongly depends on WR device implementation

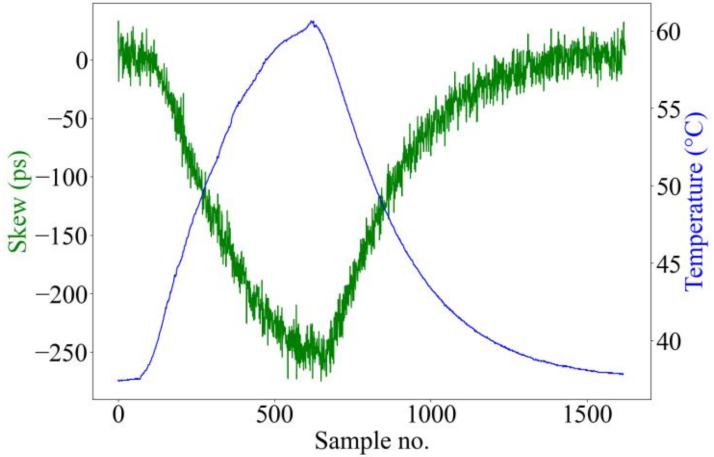
WR clk skew

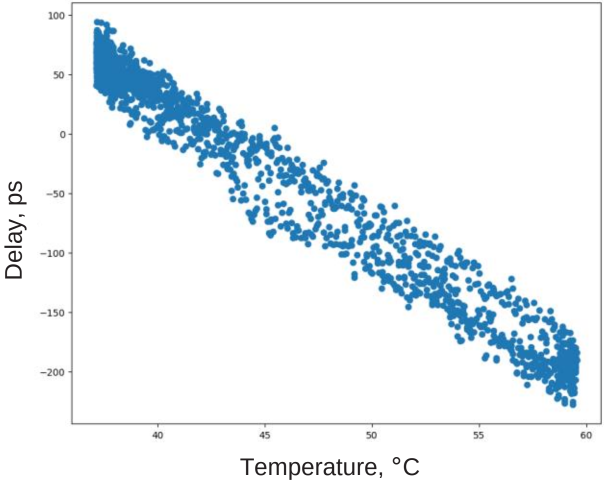
- has a linear correlation with WR device temperature
- depends on complexity of factors
- depends on WR device implementation



Temperature effects on clk skew
Slow temperature changes

WR devices will operate over the daily and seasonal temperature fluctuations.





Moderate slow temperature change (~30 min)
ΔT= (37-60°C), 260 ps Δt difference (11 ps/°C)

Pearson correlation coefficient
r = -0,98700

Temperature effects on clk skew (contd.) Rapid temperature changes (-50°C)

Device: switch WRS-18

- Grand-master mode
- Fixed room environment
- Aerosol Freezer Spray
- Metal device case

Results: No significant changes in PPS skew

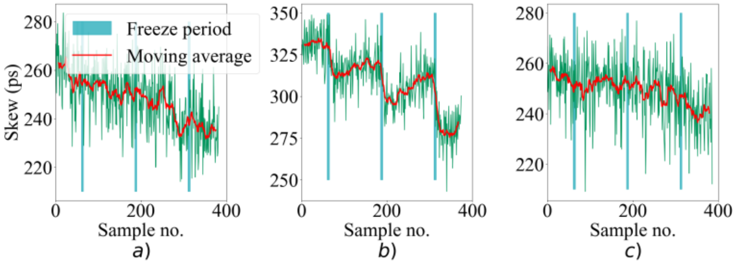
Conclusion: GM SW is protected from short-term weather effects

Device: node CuteWR-A7

- Fixed room environment
- Aerosol Freezer Spray
- Heat sink, plastic case, SFP

Results:

- rapid clk skew changes (~30 ps)
- long-term transient process



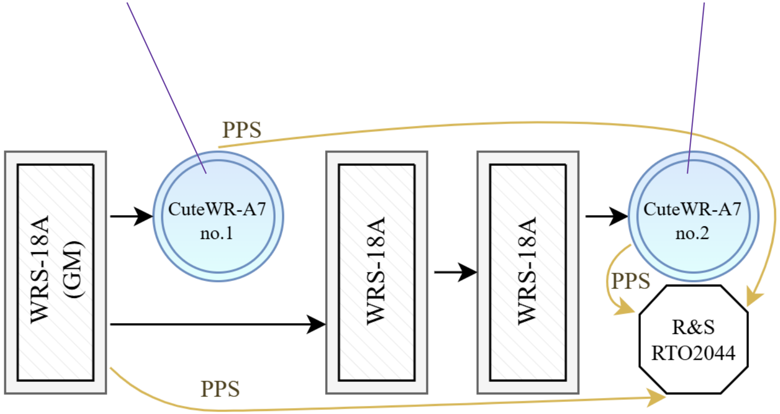
Conclusion: nodes are not protected from weather effects, but clk skew changes are tolerable

Temperature effects on clk skew (contd.)
Static temperature (20°C and 24°C)

- Eliminated long transient period

31 ps/°C skew error
<1 ps jitter difference

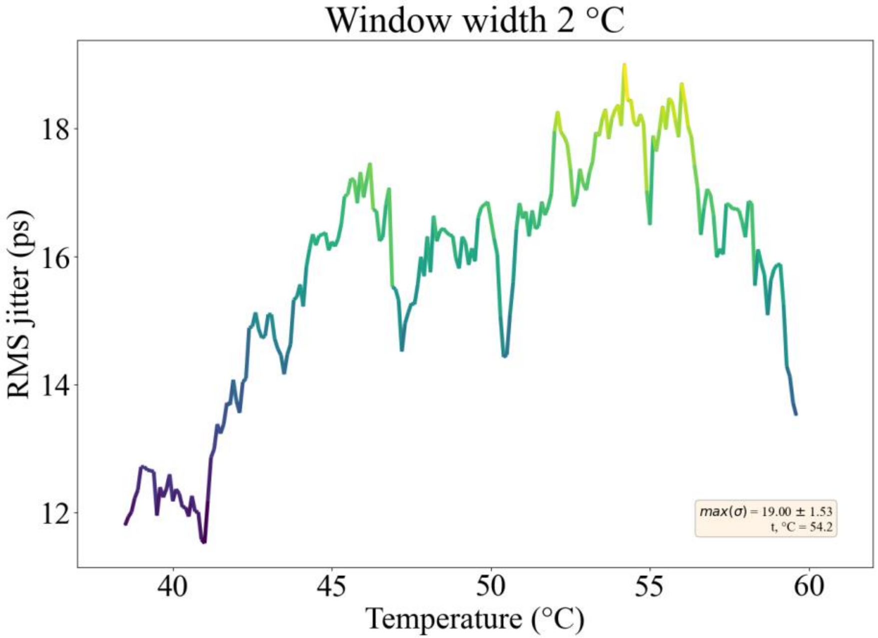
1 ps/°C skew error
<2 ps jitter difference



Conclusion:
- unpredictable system-effects in a particular setup
- still tolerable clk skew

Temperature effects on clk jitter

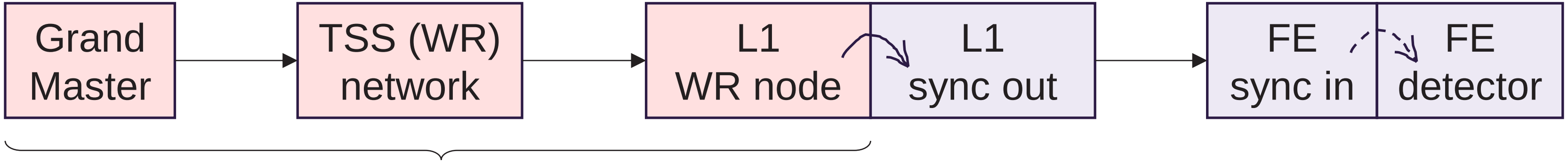
Very few reports on jitter and temperature correlation in the literature.



- **Device**: CuteWR-A7
- We have observed a jitter peak at 54.2°C
- The rise of the temperature leads to growth of the instability of the PPS signal

Conclusion: skew and jitter budget of a clock signal path

Different detectors may present more strict or more relaxed requirements.
Some detectors will be asynchronous to WR.



SyncTechnology’s WR provides acceptable baseline jitter and clock skew performance for SPD DAQ.

<300 ps PPS skew, <20 ps PPS jitter
Temperature effects:
30 ps/°C skew error, negligible jitter error

Future work for the TSS involves experiments and analytical estimates of accuracy and precision for the generated synchronous signals at the outputs of the SPD DAQ elements and their execution at the SPD detectors’ side.

Reports on calibration methodology, and accuracy and precision evaluation

This work got support from Russian Ministry of Education and Science, state assignment for fundamental research (code FSEG-2024-0033).

IP:

- “WR-NODE Calibration Refinement Program”

Conference publications:

- Д. Рябиков и др. «Использование технологии White Rabbit в эксперименте SPD», на SAEC-2024
- D. Kozyrev et al. “White RabbitTechnology Evaluation for the SPD Experiment”, at PIERE-2024 (IEEE)

Workshop presentation:

- Н. Макаревич «Задача измерения дисперсии Аллана в сети White Rabbit», на семинаре Разработка электронных систем обработки данных - 2024

TSS development roadmap

2024

- ✓ New! WR calibration tools
- ✓ New! Jitter evaluation
- ✓ Development of TSS protocol specification elements
- ~~Release of 2nd revision of WR evaluation board~~
- ~~Project porting for Cyclone 10~~
- New! Preliminary TSS testing

2025

- TSS controller prototype implementation
- Preliminary integration and testing with DAQ L1 elements
- New! Evaluation of WR implementation based on PangoMico FPGA

2026

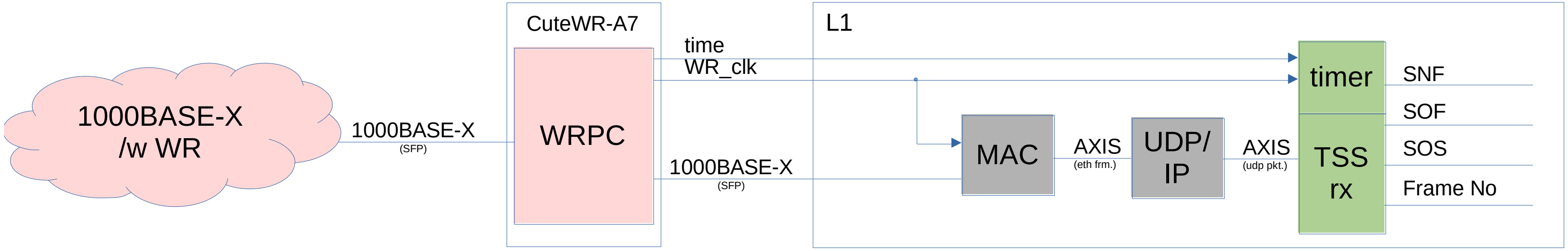
- WR network deployment and configuration for TSS network segments

2027

- Continuous support and refinement of TSS

Hardware platforms to test TSS-nodes (to be located at L1)

CuteWR-A7 in cascade mode as external WR-capable device



DK-DEV-10CX220-A

- Cyclone10 GX FPGA

iW-RainboW-G30D

- Zynq UltraScale+ FPGA