VIII SPD COLLABORATION MEETING
Nov 05-08, 2024
Dubna

ASIC chipset for the NICA-SPD Range (Muon) System

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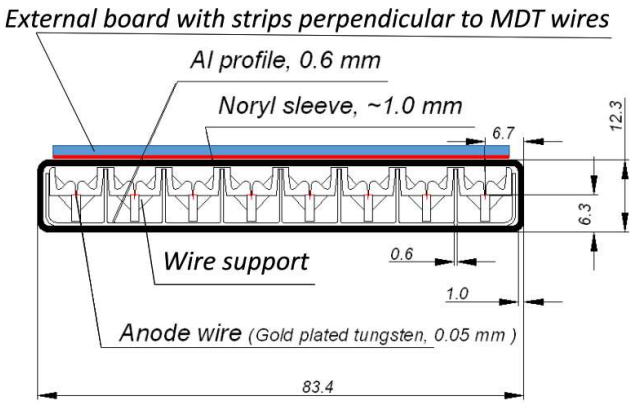
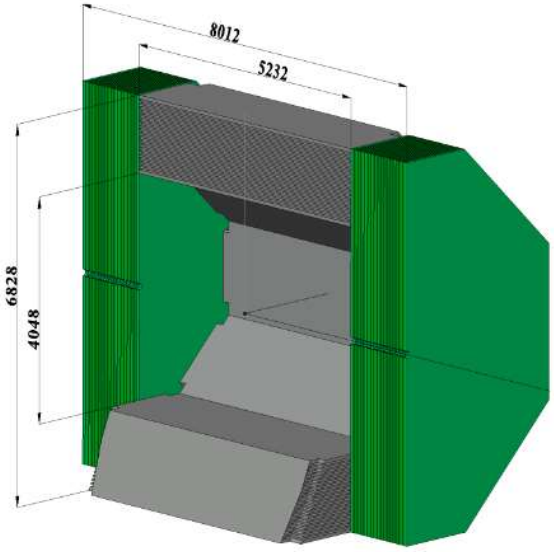
ASIC chipset for the two-coordinate MDT with open cathode geometry

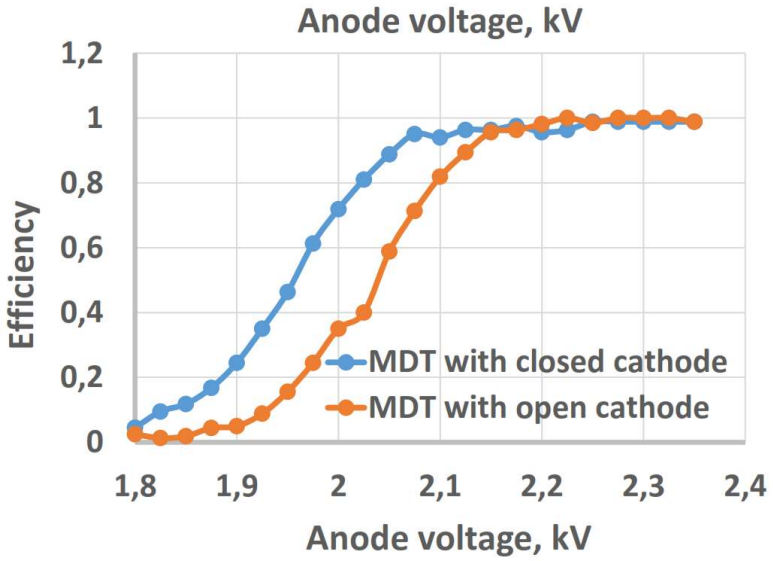
Parameters of the MDT with open cathode geometry

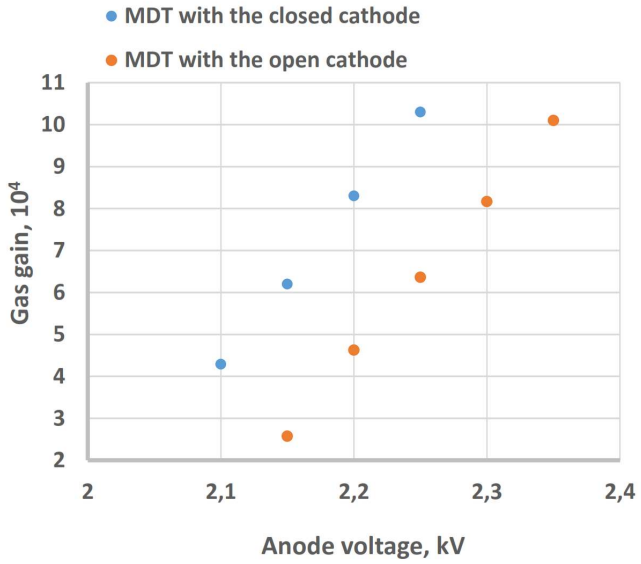
Anode section	
Wire diameter, microns	50
Wire pitch, mm	10
Length of tubes, mm	до 5232
Wire capacity, pF	50
High voltage, V	2300
Gas mixture	70% Ar + 30% CO2
Multiplication factor	8.1E4
Negative input charge, fC	13
Electron drift time, ns	(150÷200)
Cathode section	
Width of strips, mm	30
Strip length, mm	до 3414
Strip capacity, pF	1800
The induced positive charge, in % of the charge on the wire, i.e. (5-7) times less than the charge from the wire	(15÷20)

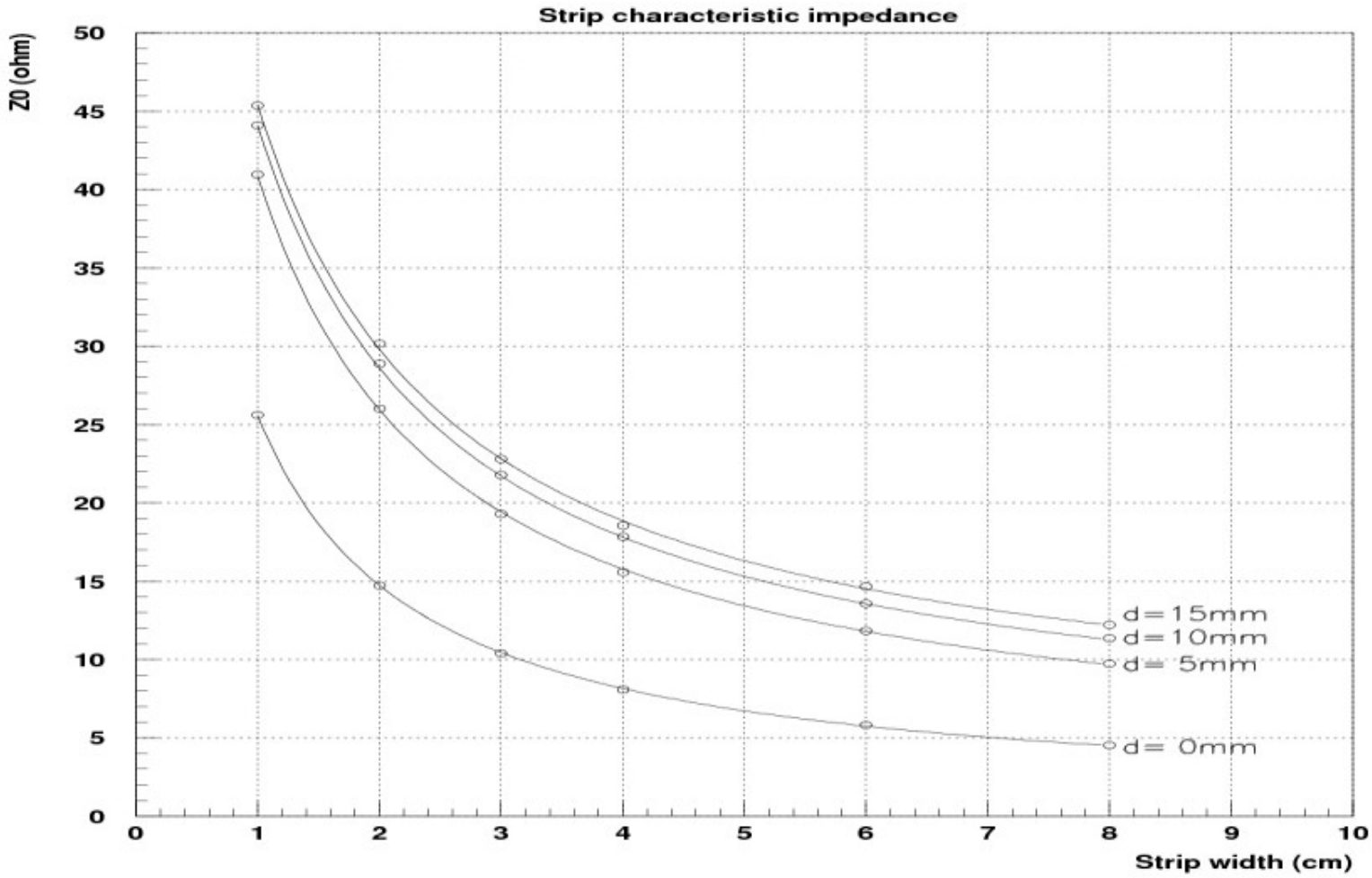
MDT with open cathode geometry and external pickup electrodes (strips) cross-section











The dependence of the wave resistance of the strips on the width of the strips and the distances between the strip plane and the absorber plate, d = 0÷15 mm

ASIC chipset for the MDT with open cathode geometry

Basic developments
Ampl-8.53 – 8-channel transimpedance amplifier
Disc-8.17 - 8-channel discriminator

Planned developments:
Ampl-8.11R-G5 - 8-channel Rush amplifier

Semiconductor factory and technology

Branch of the Scientific and Technical Center "Belmicrosystems" of JSC "Integral" (Minsk)
Microwave complementary bipolar technology (CBT), developed on the basis of pJFET-bipolar technology with design standards of 1.5 μm

Chip packages
Chips are assembled into metal-ceramic packages of the H16.48-2B type

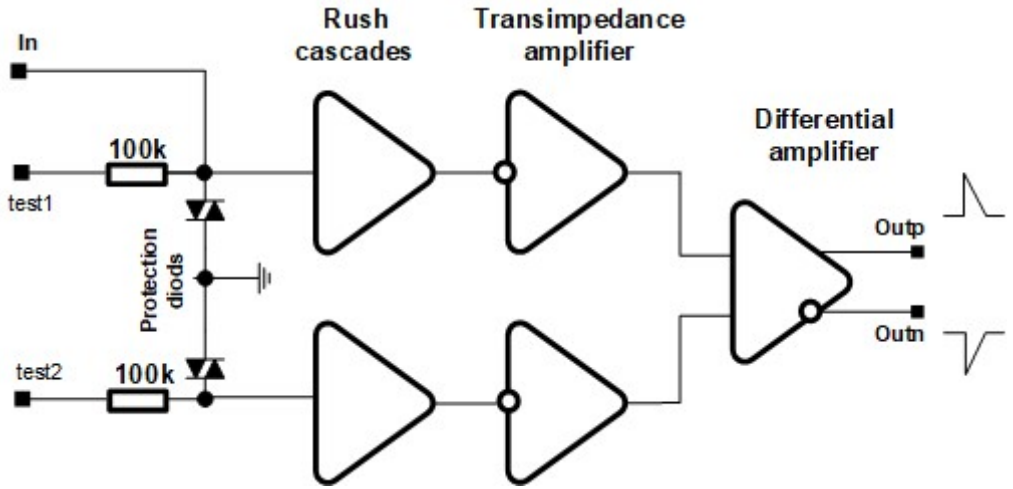
Supply voltages
Bipolar supply: +/-3 V

Ampl-8.53 – 8-channel transimpedance amplifier

Ampl-8.53 specification

Input impedance: 1 MHz, Ohms 10 MHz, Ohms 30 MHz, Ohms	 0.25 0.9÷2.2 3.32÷8.7
Input signal polarity	±
Protection against positive and negative discharges	yes
Differential output	yes
Differential conversion factor, mV/uA	100÷150
Offset voltage between outputs, V	≤1.0
Output load, ohms, not less	1000
Rise time, (0.1-0.9), ns	8÷12
Inoise at detector capacity: C_{det}= 0, r.m.s. nA C_{det}= 40 pF, r.m.s. nA C_{det}= 1800 pF	 63÷110 96 315
Dynamic range at C_{det} = 0, dB	48
Cross-talk, dB	<-40
Supply voltage, V	±3
Power dissipation, mW	510
The number of channels	8

Ampl-8.53 channel block diagram



Ampl-8.53 vs Ampl-8.3

Parameter	Ampl-8.3	Ampl-8.53
Input resistance, Ohm	50	<10
Supply voltage, V	+/-5	+/-3
Technology	pJFET-bipolar	CBT

Development and manufacture stages of Ampl-8.53

ASIC	Status	Result
Ampl-8.51	Prototype: **manufactured and tested**	The parameters meet the specification
Ampl-8.53	Pre-production run: **in production** Circuit design similar to Ampl-8.51 Editing topology: separate wide power supply buses for the Rush stage and the output stage	

Disc-8.17 - 8-channel discriminator

Disc-8.17 specification

Input current, uA	≤5
Input current difference, uA	≤0,5
Signal propagation delay (when exceeding the threshold of 200 mV), ns	≤10,0
Rise/fall of the output pulse, ns	≤2,5
Minimum output signal width, ns	20
Output load, ohms	110
Output stage	open collectors
Output current, mA	3.5
Supply voltage, V	±3.0
Power consumption, mW	≤500

Disc-8.17 vs Disc-8.3

Parameter	Disc-8.3	Disc-8.17
Supply voltage, V	+/-5	+/-3
Technology	pJFET-bipolar	CBT

Development and manufacture stages of Disc-8.17 u Disc-8.15

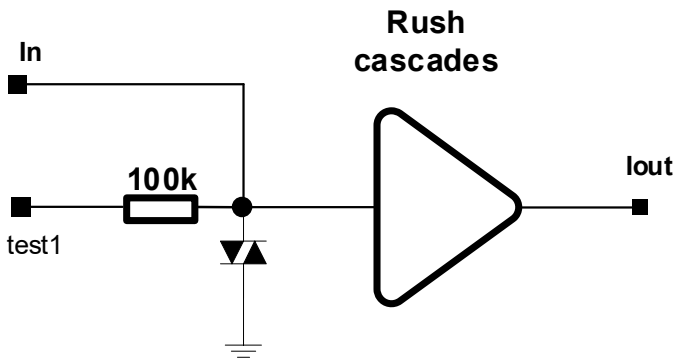
ASIC	Status	Result
Disc-8.15	Prototype: **manufactured and tested**	The parameters meet the specification
Disc-8.17	Pre-production run: **contract preparation** Schematics: added 20 ns time hysteresis	

Ampl-8.11R-G5 - 8-channel Rush amplifier

Ampl-8.11R-G5 specification

Параметр	Значение
Input impedance: 1 MHz, Ohms 10 MHz, Ohms 30 MHz, Ohms	 3.5 3.5÷4 4.25÷6.1
Input signal polarity	±
Protection against positive and negative discharges	yes
Output load, ohms, no more	50
Current gain	5÷7
Rise time, (0.1-0.9), ns	3÷4
Supply voltage, V	±3
Power dissipation when powered □3V, MW	192
Number of channels	8

Ampl-8.11R-G5 channel block diagram



Ampl-8.11R vs Ampl-8.11R-G5

Parameter	Ampl-8.11R	Ampl-8.11R-G5
Current gain	3	5÷7

Development and manufacture stages of Ampl-8.11R u Ampl-8.11R-G5

ASIC	Status	Result
Ampl-8.11R	Prototype: **manufactured and tested**	The parameters meet the specification
Ampl-8.11R-G5	Выполнена разработка схемотехники и топологии **Production is planned**	

Reading analog signals from the MDT with open cathode geometry

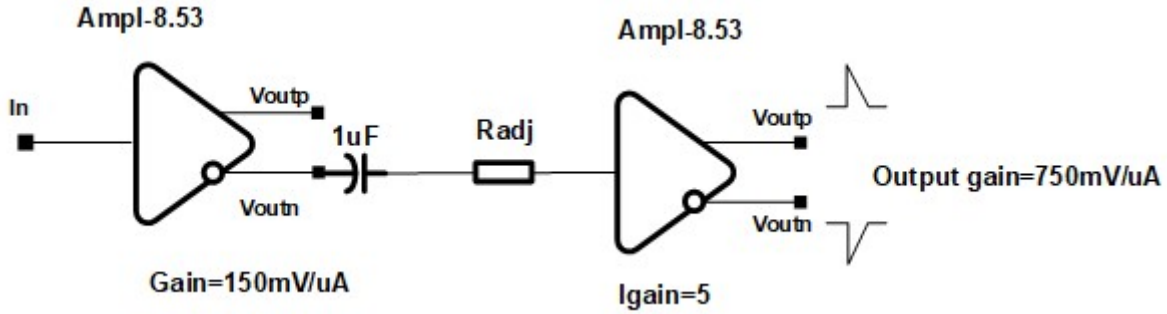
Reading signals from anode wires: Ampl-8.53+Disc-8.17

Reading signals from strips:

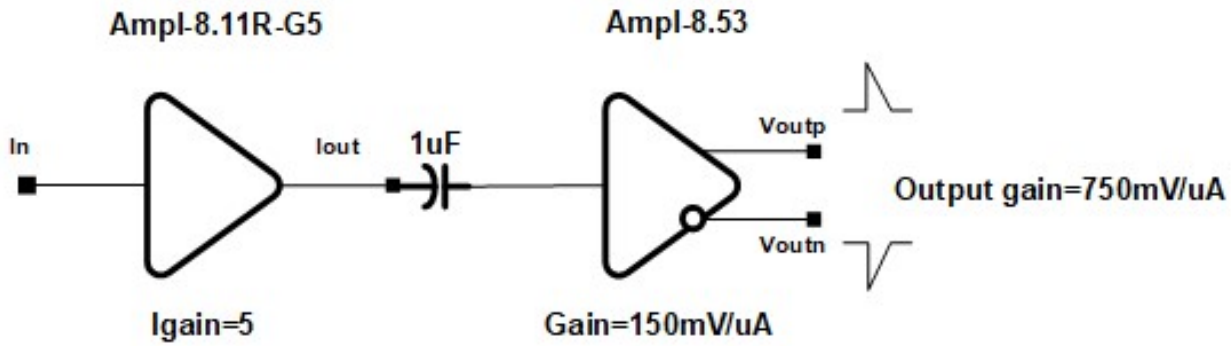
1) Ampl-8.53+Ampl-8.53+Disc-8.17
2) Ampl-8.11-G5+Ampl-8.53+Disc-8.17

Connecting channels:

1) Ampl-8.53+Ampl-8.53



2) Ampl-8.11-G5+Ampl-8.53



Development of an ASIC for straw and micromegas detectors of the NICA-SPD

Work status: conclusion of a contract for the manufacture of an 8-channel prototype IC **AST-SPD-8_v1rev01**

Production:31.08.2025

AST-SPD-8_v1rev01 specification

<table>
<tr><th colspan="2">Detector parameters</th></tr>
<tr><td>Negative input charge, fC</td><td>2000</td></tr>
<tr><td>Detector channel capacitance, pF</td><td>20÷100</td></tr>
<tr><td>Detector occupancy, kHz</td><td>up to 200</td></tr>
<tr><td>Working mode</td><td>triggerless</td></tr>
<tr><th colspan="2">Common chip parameters</th></tr>
<tr><td>Technology</td><td>CMOS, 180 nm</td></tr>
<tr><td>Number of channels</td><td>8</td></tr>
<tr><td>Supply voltage, V</td><td>1.8</td></tr>
<tr><td>Power dissipation, mW/ch</td><td>10</td></tr>
<tr><td>Channel optimization criteria:
1) Maximum occupancy
2) Minimum dead time
3) Power dissipation
4) Chip area</td><td><table><tr><td rowspan="2">CSP</td><td>FS</td><td>Dis</td><td>TDC</td></tr><tr><td colspan="2">SS</td><td>SAR ADC</td></tr></table>
TDC per time channel
SAR ADC per amplitude channel</td></tr>
<tr><td>Additional functions</td><td>OR output
Individual channels testing
Noisy channels masking</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Data output</td><td>4 parallel channels,120 MHz</td></tr>
</table>

Digital signals	sLVDS
Control	Configuration register
Test channel	Shape and gain control of analog signals: differential outputs of fast and slow shapers Discriminator test: differential outputs
Fast shaper, time channel	
Shaping time, ns	6÷10
Time resolution, ns	1
ENC (r.m.s.), e @ Cd=60pF	<1000
Slow shaper, amplitude channel	
Shaping time, ns	75/150/250
Shaper order	4
Gain, mV/fC	1/3/6/9
ENC (r.m.s.), e @ Cd=60pF	<1000
ADC, bit	10
Time conversion, ns	100