Status of SVD description in SPDroot source code

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MAPS/DSSD options in SPDroot source code

Are there any other tests?

My code was merged with the current development branch:
https://git.jinr.ru/avasyukov/spdroot/-/tree/SVD_Vasyukov

Visualization of geometry:

- spdroot/macro/geom/ConstructDssd.C
- spdroot/macro/geom/ConstructMaps.C

Launch: root -l Construct<Det>.C

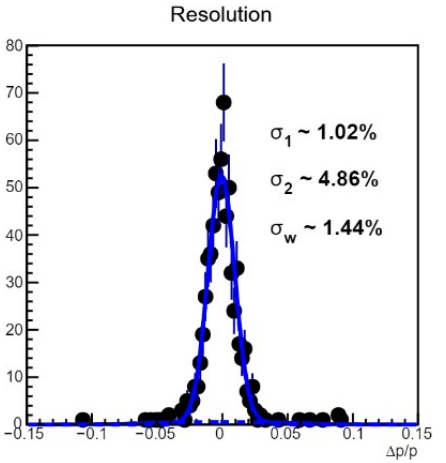
Performance tests:

- spdroot/macro/performance-tests/track-fitting/dssd-straw_noIts/
- spdroot/macro/performance-tests/track-fitting/maps-straw_noIts/

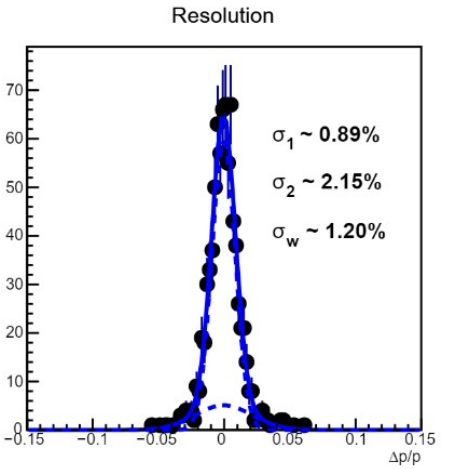
Launch: bash run.sh

Previous reports:
https://indico.jinr.ru/event/4598/#1-status-of-separating-maps-an
https://indico.jinr.ru/event/4702/#2-status-of-svd-description-in
https://indico.jinr.ru/event/4753/#1-status-of-mapsdssd-separatio

Dssd



Maps



End-cap for MAPS

Role model: Muon Forward Tracker (ALICE experiment)
TDR: https://cds.cern.ch/record/1981898
Detector web page: https://alice-collaboration.web.cern.ch/menu_proj_items/MFT

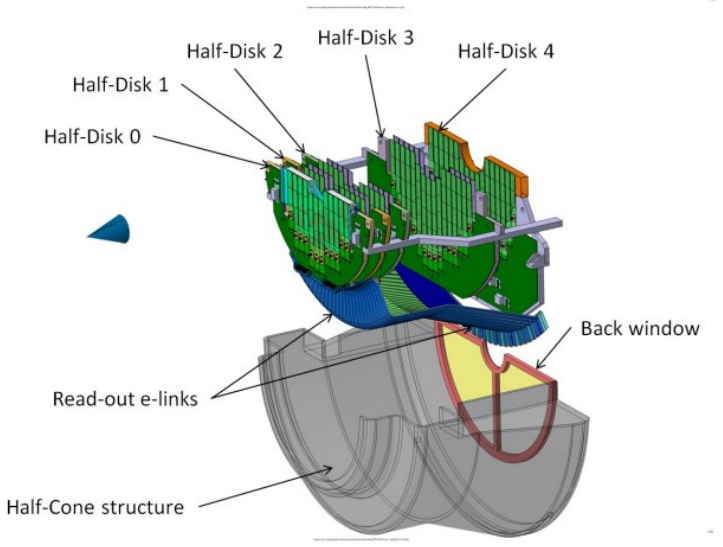
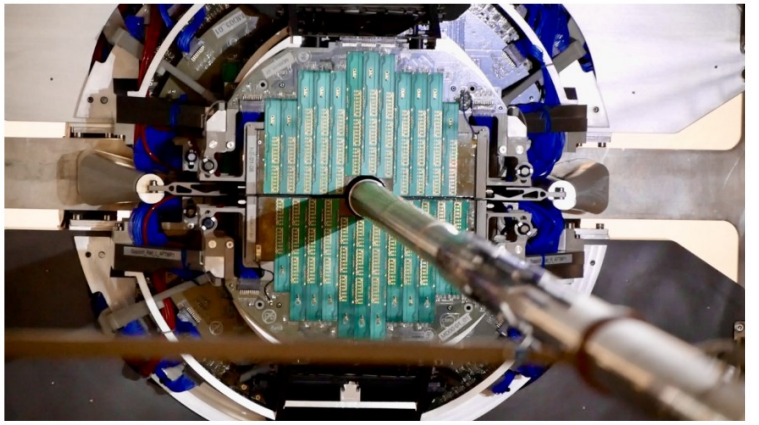


Figure 4.3: General layout of the MFT Half-Cone.



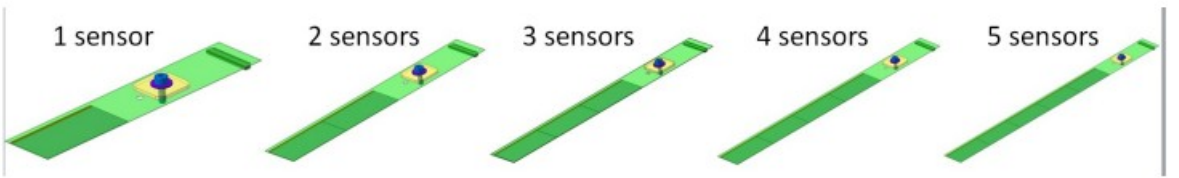
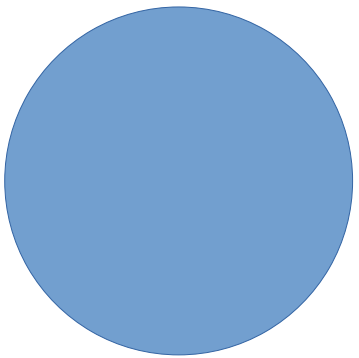


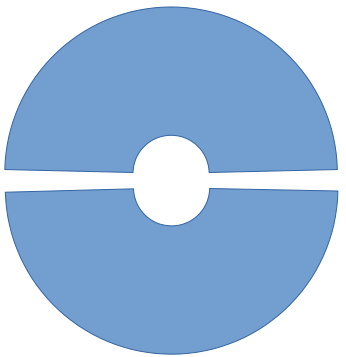
Figure 3.1: The 5 types of MFT ladders

End-cap Geometry Volumes

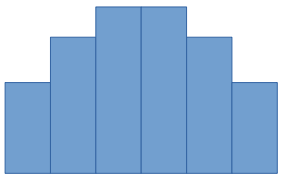
/spdgeometry/its/SpdItsVolPars.h



L1 Layer
Med: air
TGeoTube



L2 Segment
Med: air
TGeoTubeSeg



SpdItsLadder

L3 Ladder
silicon

SpdItsChip

L4 Chip
silicon

Further plans

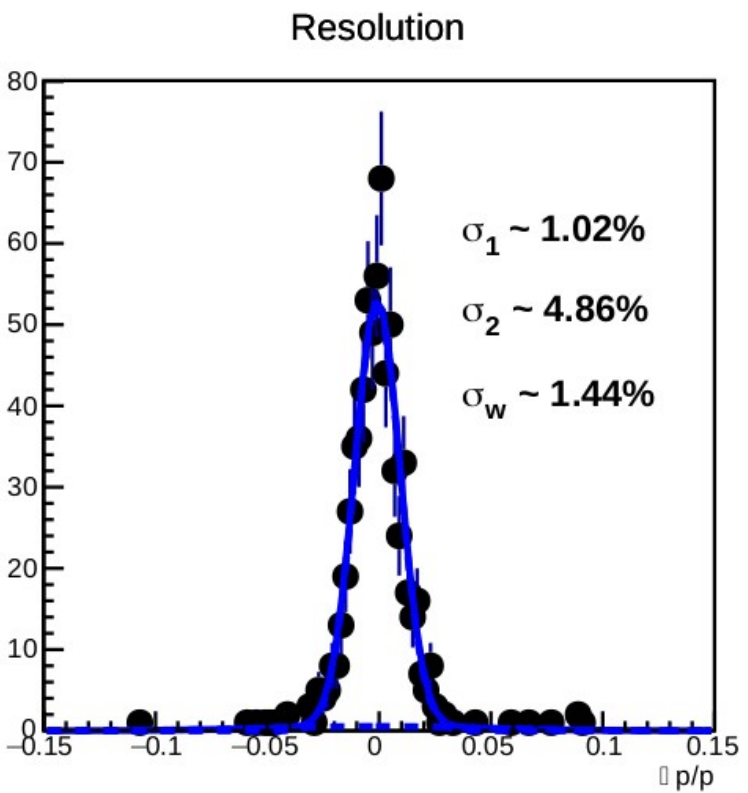
- If recommended, conduct additional testing of the code;
- Push development branch to nica/spdroot repository;
- Adding End-Caps for MAPS ongoing;

Thank you for your attention!

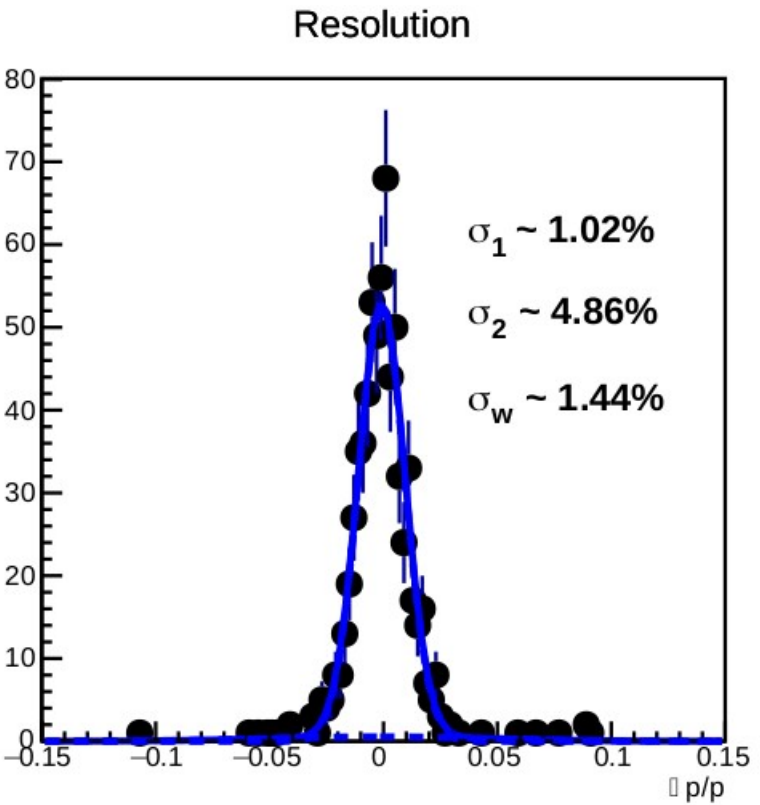
Appendix

Ap1 Performance tests DSSD

<SpdRoot dir>/macro/performance-tests/track-fitting/dssd-straw
. run.sh

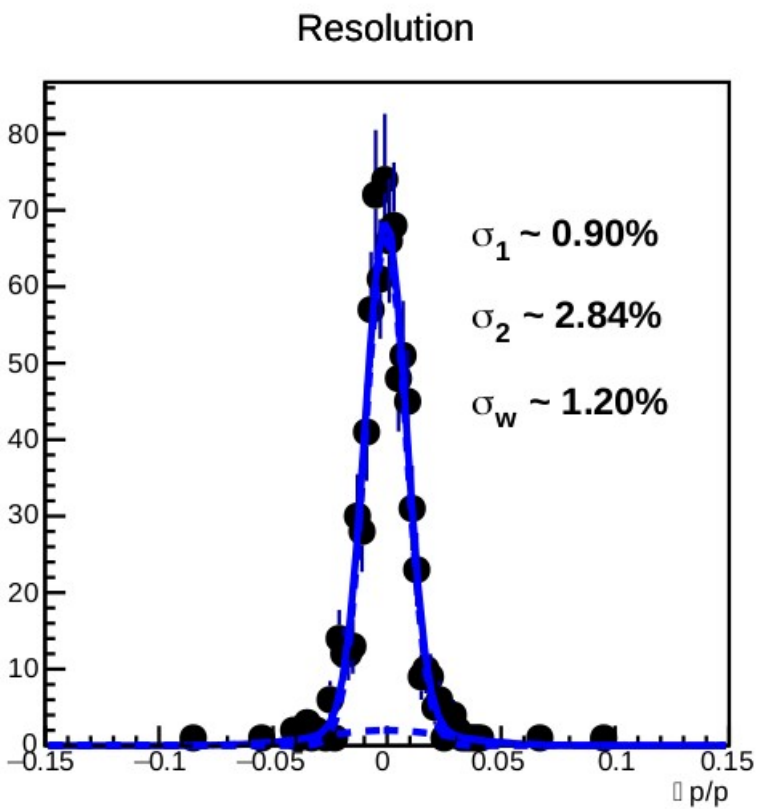


<SpdRoot dir>/macro/performance-tests/track-fitting/dssd-straw_noIts
. run.sh

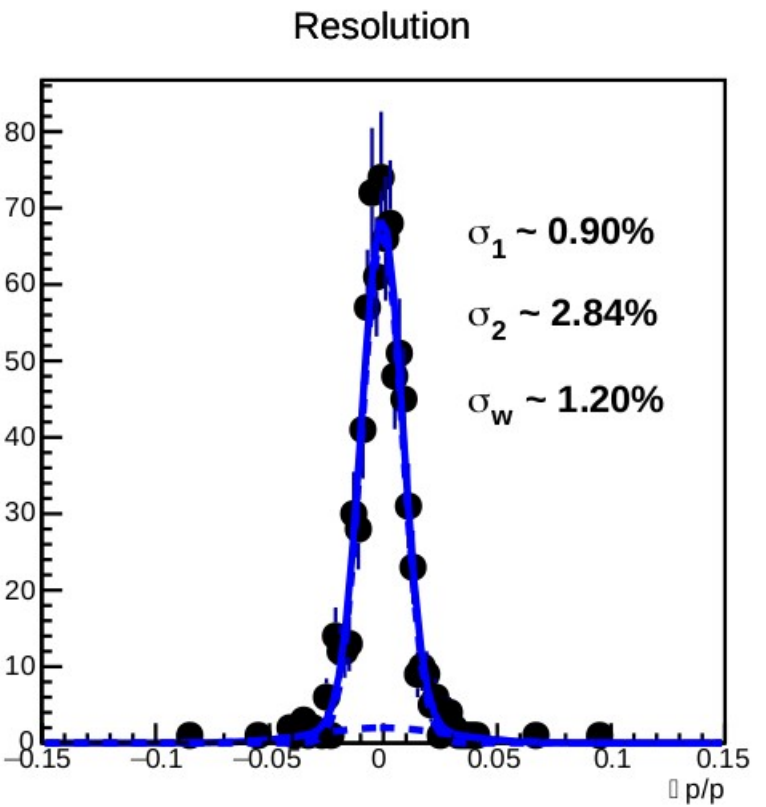


Ap2 Performance tests MAPS

<SpdRoot dir>/macro/performance-tests/track-fitting/maps-straw
. run.sh



<SpdRoot dir>/macro/performance-tests/track-fitting/maps-straw_noIts
. run.sh



Ap3 SVD parameters

These parameters must be set for each layer:

Layers/ladders parameters:

1. the distance from z axis to ladder center (LAYER radius)
2. ladder size along z axis
3. ladder size along phi axis
4. radial size of ladder
5. local rotation angle for ladder
6. global rotation angle for LAYER
7. number of ladders inside the LAYER

Chip paremeters:

1. chip size along z-axis
2. chip phi-size
3. gap size between chips along z-axis
4. gap size between chips along phi-axis
5. number of chip cells (channels) along z-axis
6. number of chip cells (channels) along phi-axis
7. chip type (0: NO INNER STRUCTURE, 1: MAPS, 2: DSSD, >2: USER DEFINED)