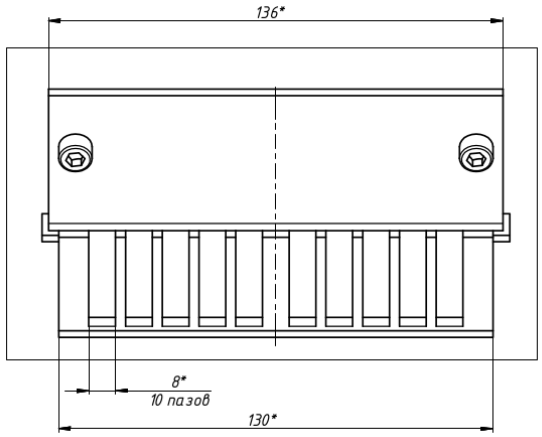
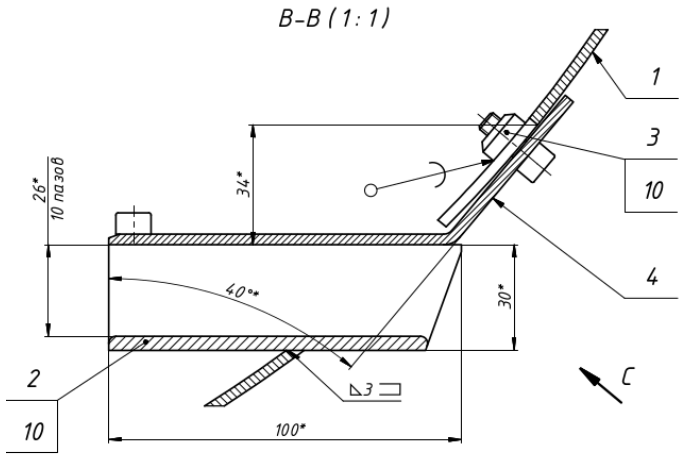
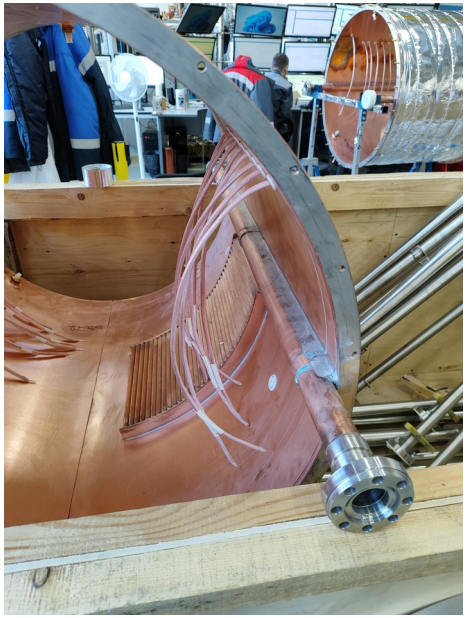
Zero Degree Calorimeter (ZDC) for SPD

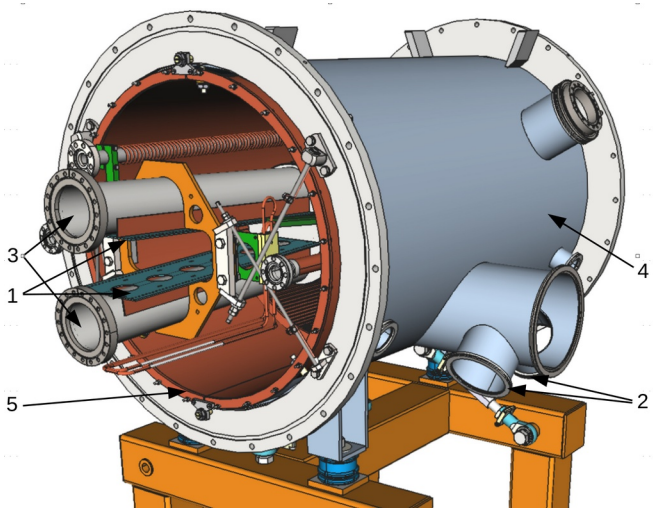
Progress report (previous report was on March, 14)

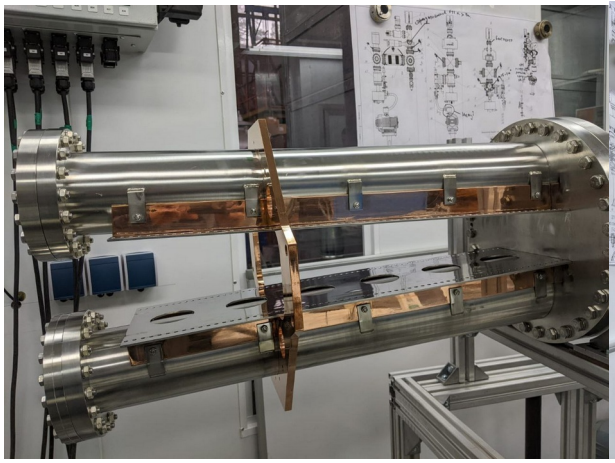
Pass through LqN_2 screen developed and hopefully cryostat sections are already modified. Cables go on one side of the screen only.
Space for wires ~ 20 cm^2

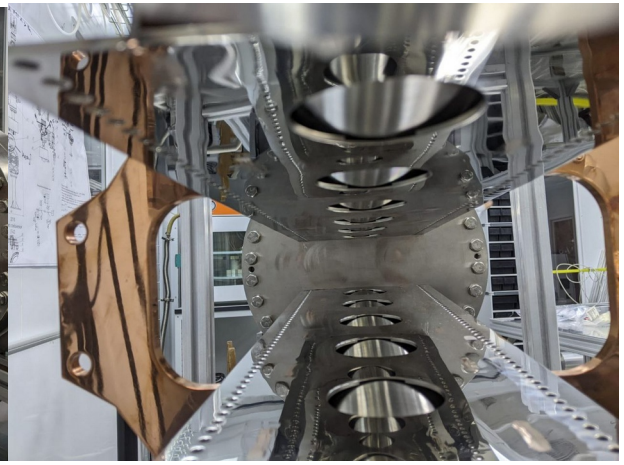




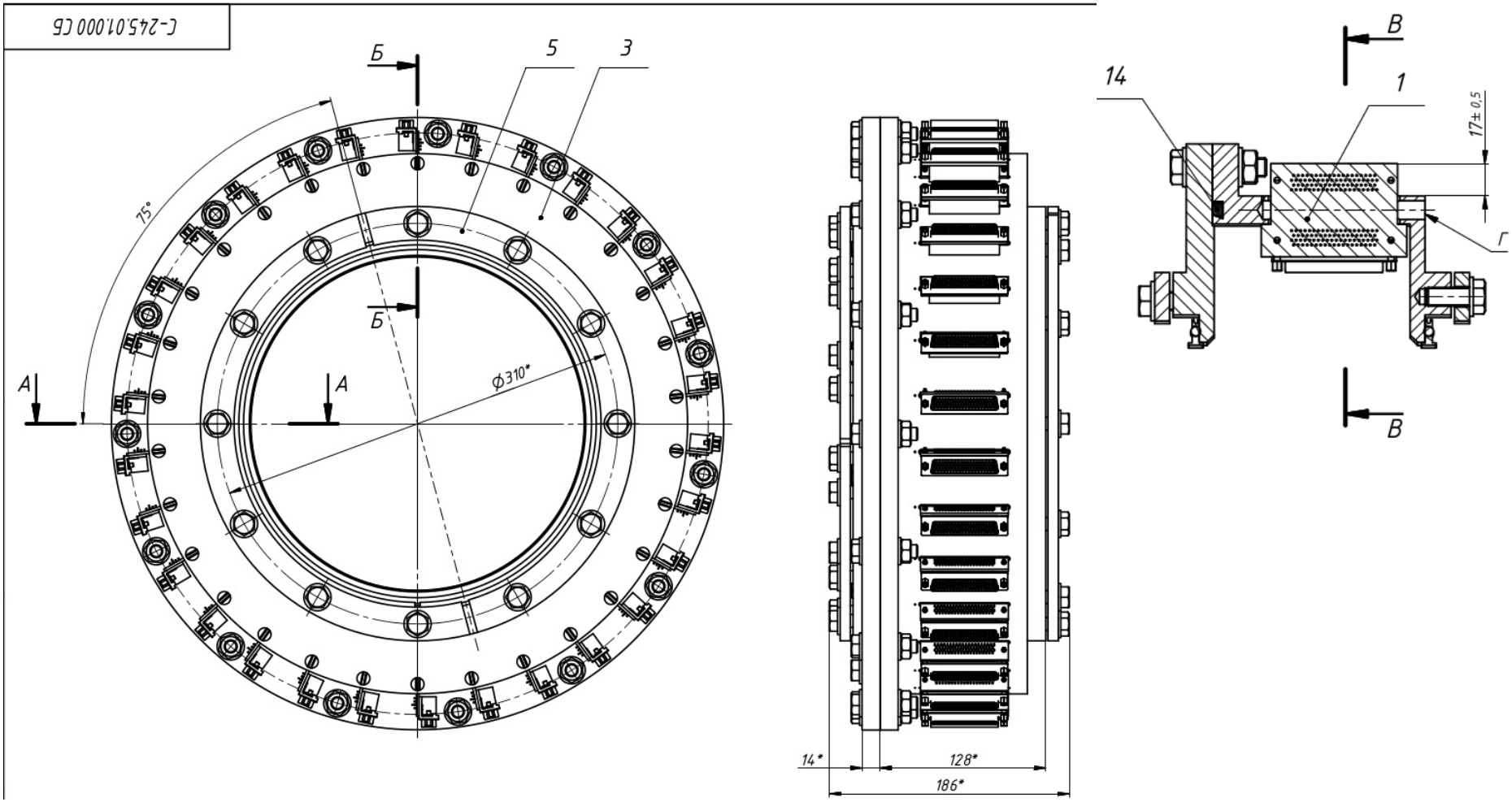




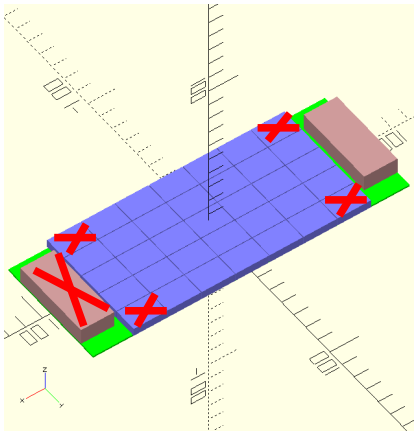




Pass from vacuum

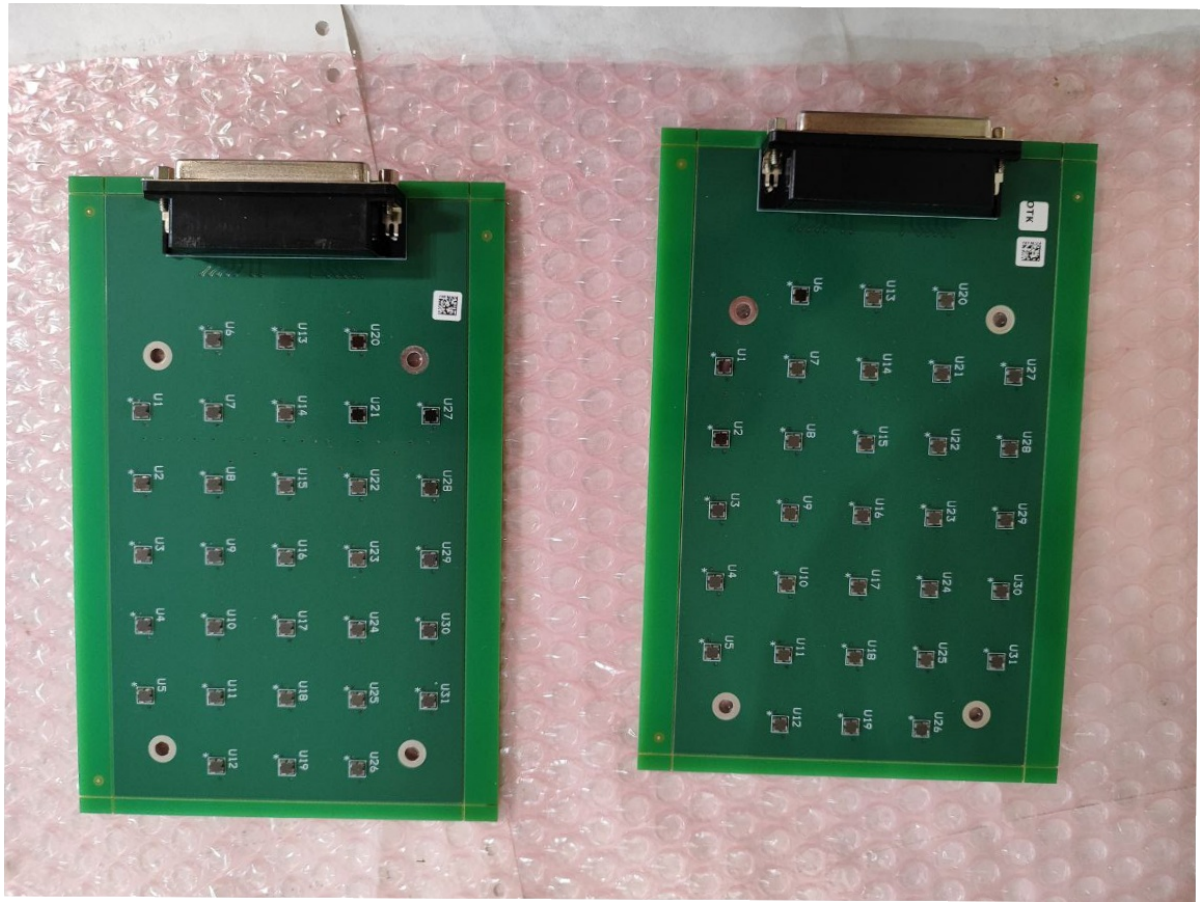


A barrel with 30 pcb boards with 78-pin connectors DHR-78F (DS1038-78F) will be installed on one side of the cryostat at large side flanges. The boards are already under production by REZONIT and should be ready by October 10.



Test SiPM boards

2 test SiPM boards with 31 SiPM each manufactured.
2 sets of square 20x20 mm^2 scintillator tiles with 3 and 5 mm thicknesses produced and connected to boards. The tiles are wrapped in high reflecting film and have polished pit in the place where SiPM is attached. Sensitive area 140x100 mm^2 correspond some middle part of ZDC.



Tunnel installation around December - March?

Original plan for the first stage of ZDC was – 6 planes with trapezoid geometry and 320 mm thick copper radiator. It was supposed to be prepared for installation by summer 2025.

What could be done by December-March:

A compact version with the same as in test board SiPM boards. 2-3 layers with a copper or stainless steel radiator about 9 cm total thickness (close to shower maximum for a few GeV).

What we need to do before the cryostat will be closed:

1. Manufacture and install vacuum feed through barrels.
2. Solder and install MGTF twisted pair cables with DHS-78M (DS1035-78M) on both sides. We need at least 3 cables at each side of IP.
3. Manufacture 4-6 more SiPM boards of the same size and design.
4. Produce 124-186 SiPM tiles 20x20x5 mm^3.
5. Make radiator planes.
6. Design an installation into the rails.
7. Assemble and install the modules.
8. A simple test with multimeter before we lose an access inside the cryostat.

Thank you for your attention

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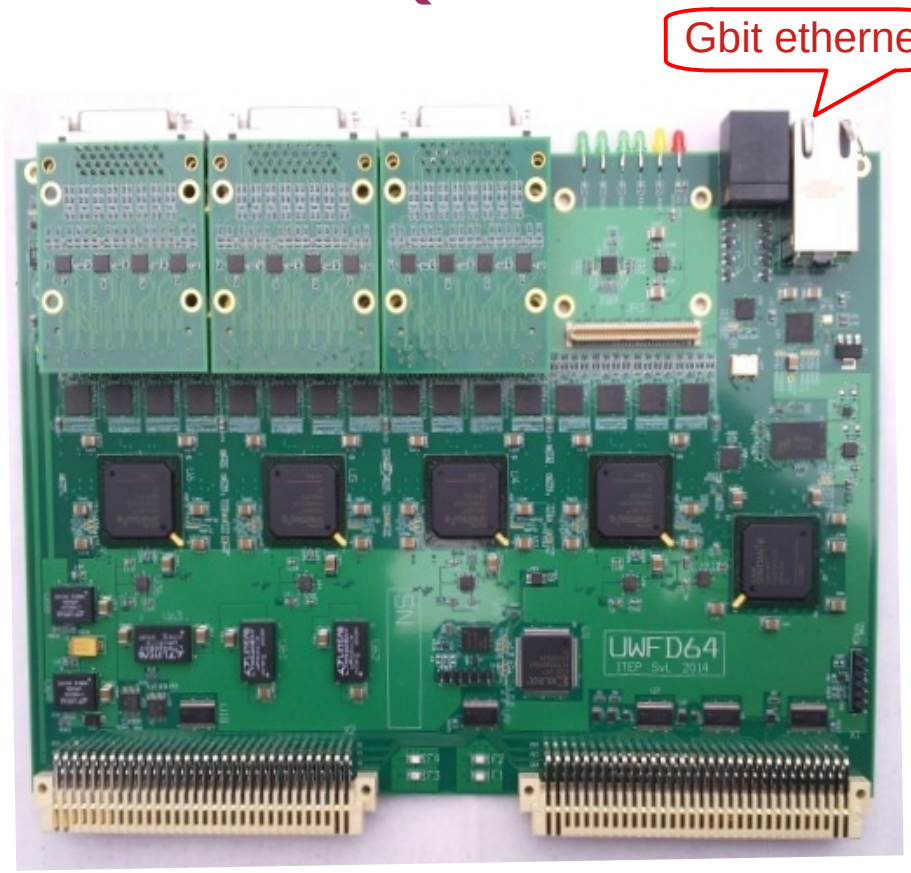
DAQ and front-end



DAQ:

- 64 channels
- 12 bits
- 125 MSPS
- 512 Mbyte DDR3 RAM
- Capable 64 bits DDR VME block transfer

Front-end:

- 32-channel
- ADA4940-2 based
- Need to be designed

SiPM power:

- 32-channel
- AD5674 based
- Is developed now for DANSS upgrade

Price estimate:
8 UWFD modules ~ 5 M rouble
15 front-end boards ~ 0.5 M rouble
15 power boards ~ 0.5 M rouble