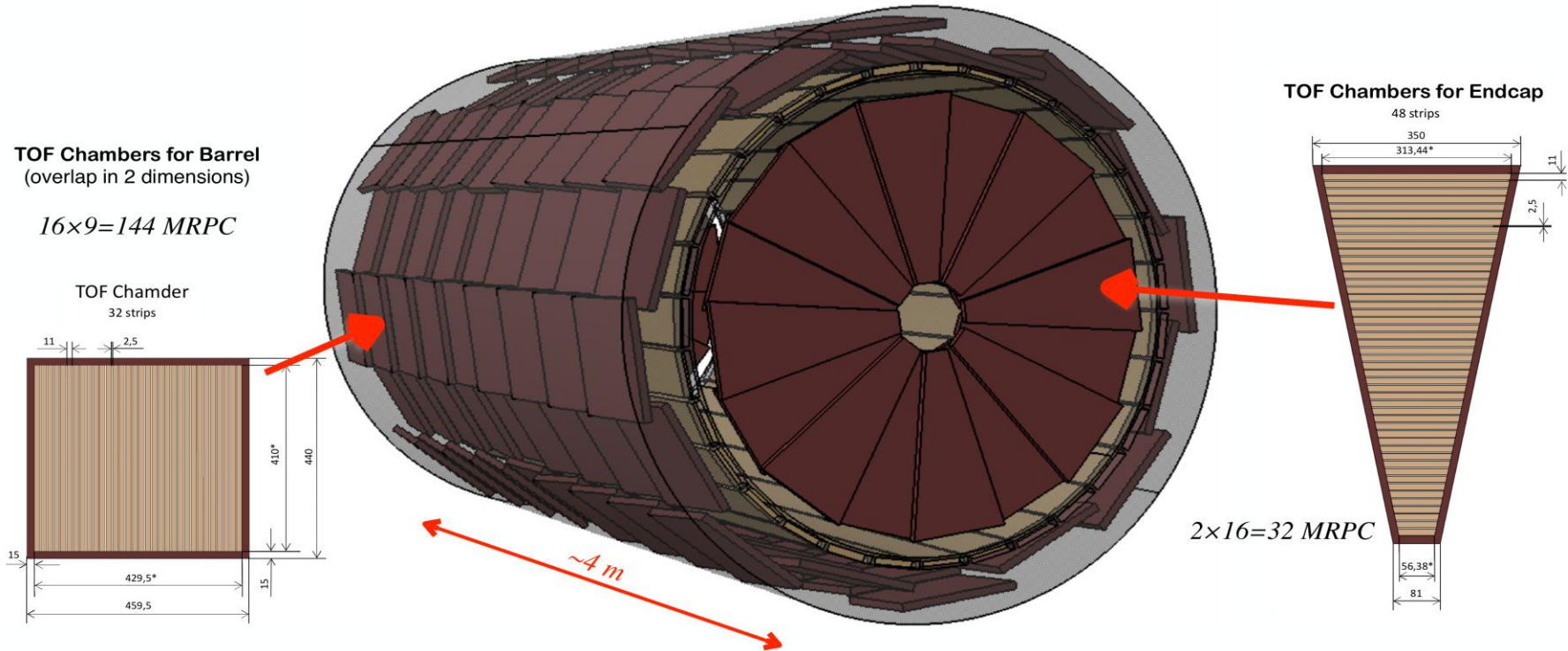


# Time of Flight Detector Status Report

**Valery Chmill**



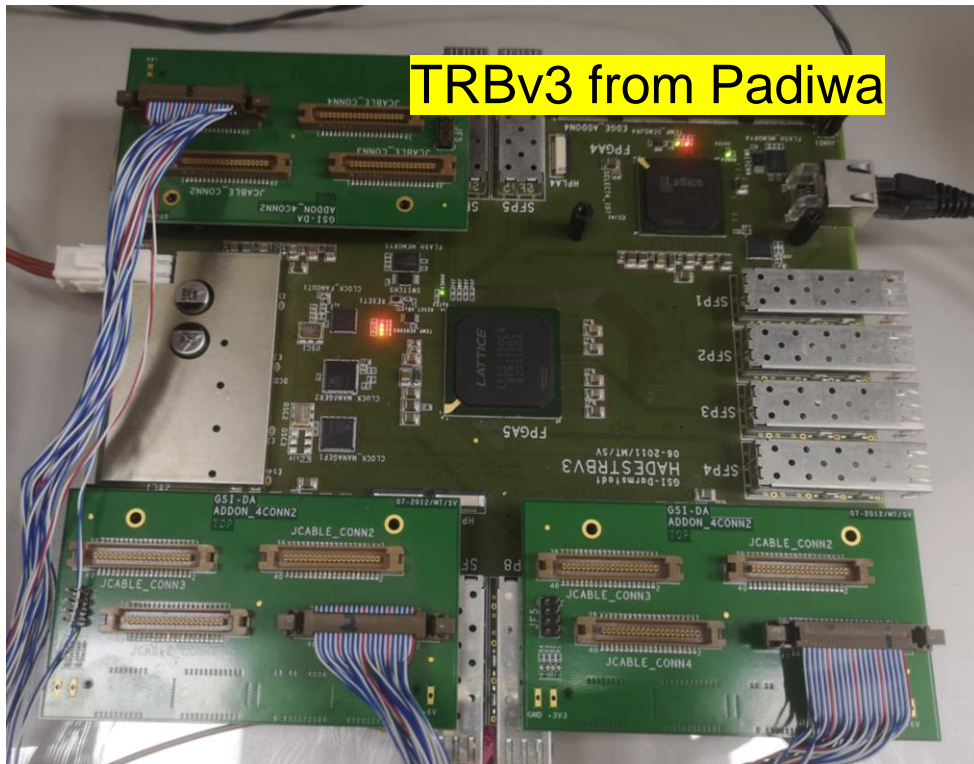
# Time of Flight (TOF) detector proposal



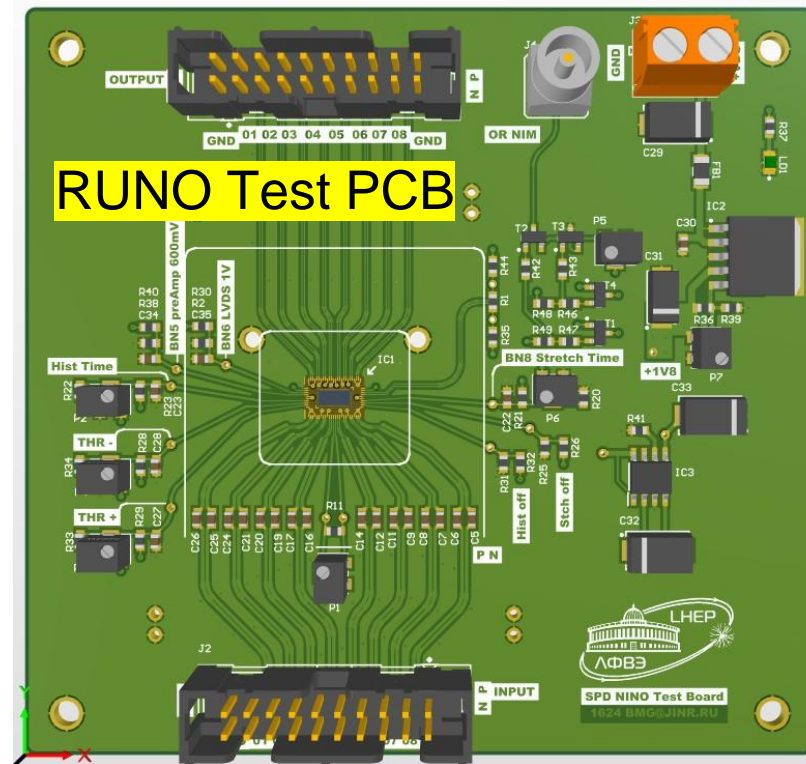
- $\pi/K/p$  discrimination for momenta  $\lesssim 2$  GeV
- Determination of  $t_0$
- Time resolution requirement  $< 60$  ps.
- Sealed (MRPC) are the base option. B.Wang et al, JINST 15 (2020) 08, C08022

- Number of readout for Barrel is  $144 \times 2 \times 32 = 9216$  channels.
- Number of readout for Endcap is  $32 \times 2 \times 48 = 3072$  channels.
- Total amount is 12288 channels

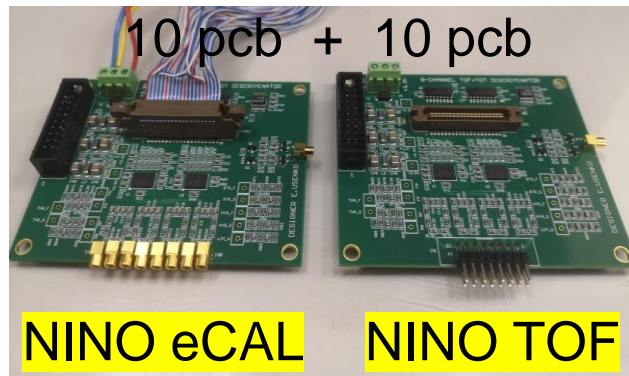
# DAQ (TRBv3) preparation and FEE news



TRBv3 from Padiwa



RUNO Test PCB



10 pcb + 10 pcb

NINO eCAL

NINO TOF








RUNO



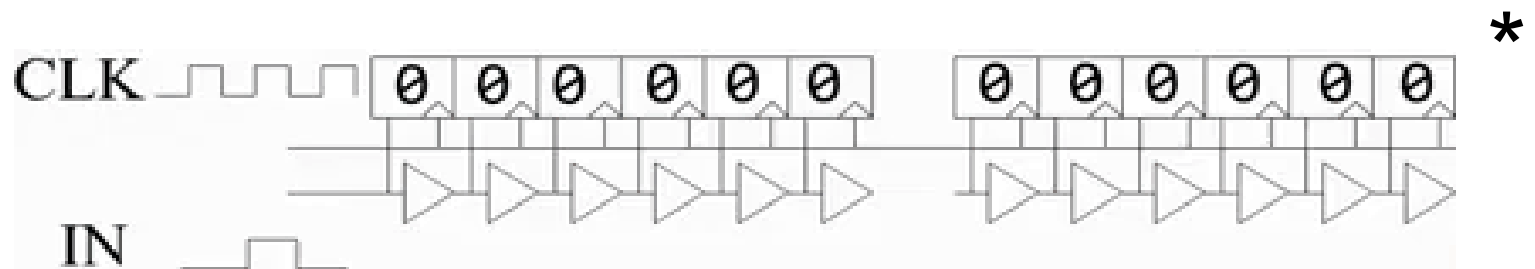
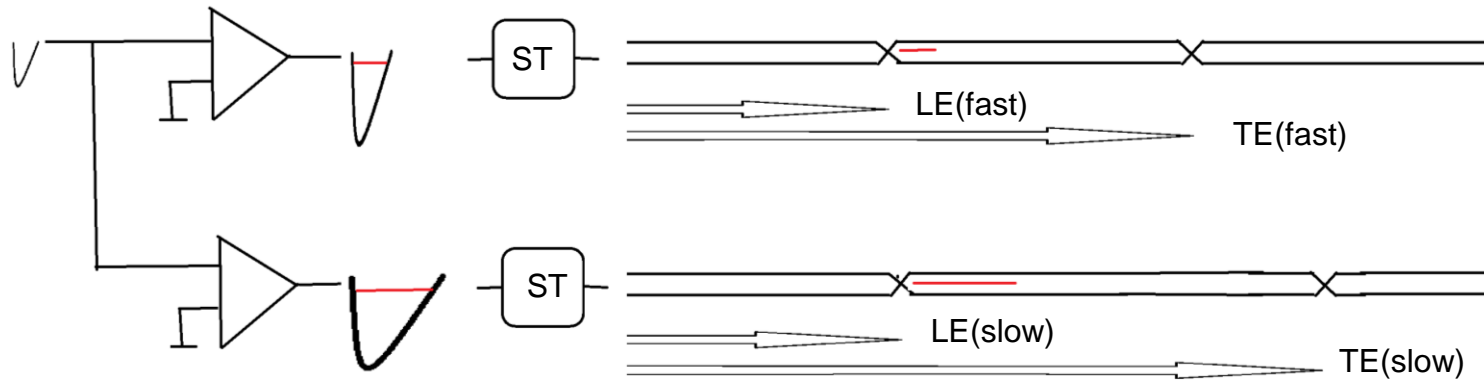
Получили безкорпусные

# TDC-Readout-Board, Triggered/Triggerless-Readout-Board

Item		Value
Supply Voltage		48 V (40-50V), galvanically isolated on board
Power Supply Current		0.5A minimum without AddOns
GbE-connectivity		max. 95 MBytes/s transfer per link
GbE-slow-control		up to 400 registers/transfer, speed depends on GbE latency
Connectivity		Max. 8 SFPs, each 2Gbit/s on board. With hub-addon: max. 32 SFP
		4 AddOns on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate		about 300 kHz (depending on configuration and network size)
Max Hit Rate		50 MHz (burst of 63 hits)
TDC Channels		260 (Single edge detection)
Time Precision		<20 ps
Minimum pulse width		<500 ps

## TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

# TDC on FPGA, TRB3 FEE from PADIWA



\* Jinyuan Wu, Z. Shi и I. Wang CERN2000

# WEB GUI



### Configuration

Board:

Filter:

# of Channels:

Update Interval (ms):

Split Table:  Differences:

Input Status:  Enable:

Hit Rate Status:

Reg	Channel	0310			
		3	2	1	0
	Channel group	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c000	0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c001	1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c002	2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c003	3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c004	4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c005	5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c006	6	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c007	7	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c008	8	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c009	9	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00a	10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00b	11	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00c	12	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00d	13	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00e	14	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c00f	15	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c010	16	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c011	17	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c012	18	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c013	19	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c014	20	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c015	21	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c016	22	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c017	23	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c018	24	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c019	25	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01a	26	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01b	27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01c	28	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01d	29	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01e	30	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c01f	31	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
c020	32	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Reg	Content	0310
	tdc version	2.1.5
	channels	32
c100	ref input	polarity correct
c104	valid trg	14844561
c105	valid tmrg trg	14844561
c106	valid notmg	0
c107	invalid trg	0
c108	multi trg	0
c109	spurious trg	0
c10a	wrong rdo	0
c10b	spikes	0
c10c	idle time	7274799
c10d	wait time	14227882
c10f	releases	14844561
c110	rdo time	412354
c111	timeout number	0
c112	data finished number	14844561

Reg	Content	0310
c800	Logic Anal. Debug Mode	0
	Calib. Prescaler	0
c801	window en.	Disabled <input type="checkbox"/>
	window bef.	<input type="text" value="0"/> ns
	window aft.	<input type="text" value="0"/> ns
c802	act chan 1	0xc000c000
c803	act chan 2	0x0
c804	data limit	<input type="text" value="8"/>
c805	inv chan 1	0x0
c806	inv chan 2	0x0

Threshold settings x TDC Registers

localhost

### Threshold Settings

#### Configuration

Board:

DAC-Chain:

Channel:

Board Type:

Update Interval (ms):

Reference (mV):

DiRich2 Flash:

Last read:

Last set:

Coarse (0-65535)

Fine (0-255)

#### Shortcuts

- c/v: Increase/Decrease channel number
- d/f: Increase/Decrease chain number
- Up/Down: Increase/Decrease by 1
- Shift + Up/Down: Increase/Decrease by 16
- PageUp/PageDown: Increase/Decrease by 256
- Shift + PageUp/PageDown: Increase/Decrease by 2048
- a/A: Increase / Decrease board address
- B/U/R: Select input field
- r: Refresh values, read-back values from Padiwa

# WEB CTS



## Central Trigger System

### - Status overview

Counter	Counts	Rate
Trigger asserted	34969050 clks.	30.00 Kcnt/s
Trigger rising edges	34969050 edges	30.00 KHz
Trigger accepted	34969050 events	30.00 KHz

Last Idle Time	30860 ns	
Last Dead Time	2470 ns	404.86 KHz
Total Dead Time	74100242 ns	7.4%

Plot will be available in a few moments

Throttle  Limit Trigger Rate to  KHz  
 Full Stop  Ignore all events

Click on the image to switch between short and long plotting intervals

Export CTS Configuration [as TrbCmd script](#) [as shell script](#)

### - Trigger Channels

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	<input type="checkbox"/>	R. Edge	Periodical Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
1	<input type="checkbox"/>	R. Edge	Periodical Pulser 1	0x1_physics_trigger	25.00 Mcnt/s	25.00 MHz
2	<input type="checkbox"/>	R. Edge	Random Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
3	<input type="checkbox"/>	R. Edge	Input Multiplexer 0	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
4	<input type="checkbox"/>	R. Edge	Input Multiplexer 1	0x1_physics_trigger	2365.45 cnt/s	2365.45 Hz
5	<input type="checkbox"/>	R. Edge	Input Multiplexer 2	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
6	<input checked="" type="checkbox"/>	R. Edge	Input Multiplexer 3	0x1_physics_trigger	6.40 Mcnt/s	30.00 KHz
7	<input type="checkbox"/>	R. Edge	Input Multiplexer 4	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
8	<input type="checkbox"/>	R. Edge	Input Multiplexer 5	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
9	<input type="checkbox"/>	R. Edge	Periph. FPGA Inputs 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
10	<input type="checkbox"/>	R. Edge	Periph. FPGA Inputs 1	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
11	<input type="checkbox"/>	R. Edge	Coincidence Module 0	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
12	<input type="checkbox"/>	R. Edge	Coincidence Module 1	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
13	<input type="checkbox"/>	R. Edge	Coincidence Module 2	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
14	<input type="checkbox"/>	R. Edge	Coincidence Module 3	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz

### - Trigger Inputs

#	Source	Inp. Rate	Invert	Delay	Spike Rej.	Override	Downscale
0	extclk[0]	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	
1	extclk[1]	2365.45 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	
2	trgext[2]	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	
3	trgext[3]	30.00 KHz	<input checked="" type="checkbox"/>	0 ns	0 ns	bypass	
4	jeclin[0]	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	
5	jeclin[1]	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	

### - Peripheral Trigger Inputs

#	from FPGA 1				from FPGA 2				from FPGA 3				from FPGA 4			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

### - Pulsers and Coincidence Detectors

Periodical Pulsers	Coincidence Detectors
--------------------	-----------------------

## ZOO on SUSE Tumbleweed:

- **VHDL** is a hardware description language that can model the behavior and structure of digital system at multiple levels of abstraction.
- **Perl** Practical Extraction and Report Language.
- **XML** ExtensibleMarkupLanguage for storing, transmitting, and reconstructing arbitrary data.
- **C++** (ROOT etc.)

# GO4 for data visualization and analysis



Windows taskbar: 2 s, All items, scatter, No Errors, Cartesian, X: Lin, Y: Lin, Z: Lin, 100% zoom.

Browser: Panel1: [TDC\_0310\_Ch00\_RisingCalibr]

Name	Info
HLD	UserFolder
TRB_8000	UserFolder
TDC_0310	UserFolder
Ch00	UserFolder
TDC_0310_Ch00_RisingFine	TDC_0310 Ch00 Rising fine counter
TDC_0310_Ch00_RisingMult	TDC_0310 Ch00 Rising event multiplicity
TDC_0310_Ch00_RisingCalibr	TDC_0310 Ch00 Rising calibration function
TDC_0310_Channels	TDC_0310 Messages per TDC channels
TDC_0310_Errors	TDC_0310 Errors in TDC channels
TDC_0310_UndetectedHits	TDC_0310 Undetected hits in TDC chann...
TDC_0310_CorrectedHits	TDC_0310 Corrected hits in TDC channels
TDC_0310_MsgKind	TDC_0310 kind of messages
TDC_0310_FineTm	TDC_0310 fine counter value
TDC_0310_RaisingFineTmCalibr	TDC_0310 raising calibrated fine counter ...
TDC_0310_CoarseTm	TDC_0310 coarse counter value
TDC_0310_TotVsChannel	TDC_0310 ToT
TDC_0310_TotMoreCounter	TDC_0310 ToT > 20 ns counter in TDC c...
TDC_0310_TotMinusCounter	TDC_0310 ToT < 0 ns counter in TDC ch...
TDC_0310_RisingCalibr	TDC_0310 rising edge calibration
TDC_0310_ToTSigmaVsChannel	TDC_0310 SigmaToT
TDC_0310_RisingChannelsDiff	TDC_0310 Rising dt to reference channel...
TDC_0312	UserFolder
TRB_8000_MsgPerTDC	TRB_8000 Number of messages per TDC
TRB_8000_ErrPerTDC	TRB_8000 Number of errors per TDC
TRB_8000_HitsPerTDC	TRB_8000 Number of data hits per TDC
TRB_8000_CalHitsPerTDC	TRB_8000 Number of calibration data hit...
TRB_8000_ToTPerTDC	TRB_8000 Calibrated delay value of fallin...
ToT_ch1	UserFolder
ToT_ch11	UserFolder
ToT_ch12	UserFolder
ToT_ch13	UserFolder
ToT_ch14	UserFolder
ToT_ch15	UserFolder
ToT_ch16	UserFolder
ToT_ch17	UserFolder
ToT_ch18	UserFolder
ToT_ch2	UserFolder
ToT_ch3	UserFolder
ToT_ch4	UserFolder
ToT_ch5	UserFolder

Panel 1: TDC\_0310\_Ch00\_RisingCalibr

TDC\_0310 Ch00 Rising calibration function 12:48:43 2024-04-26 Analysis/Histograms/TRB\_8000/TDC\_0310/Ch00/TDC\_0310\_Ch00\_RisingCalibr

TDC_0310_Ch00_RisingCalibr	
Entries	600
Mean	396.3
Std Dev	132.9
Underflow	0
Overflow	0
Integral	1.868e+06
Skewness	-0.4529

Panel 2: ToT\_ch8 Width of slow channel 12:51:51 2024-04-26 Analysis/Histograms/ToT\_ch8/ToT\_ch8\_Slow

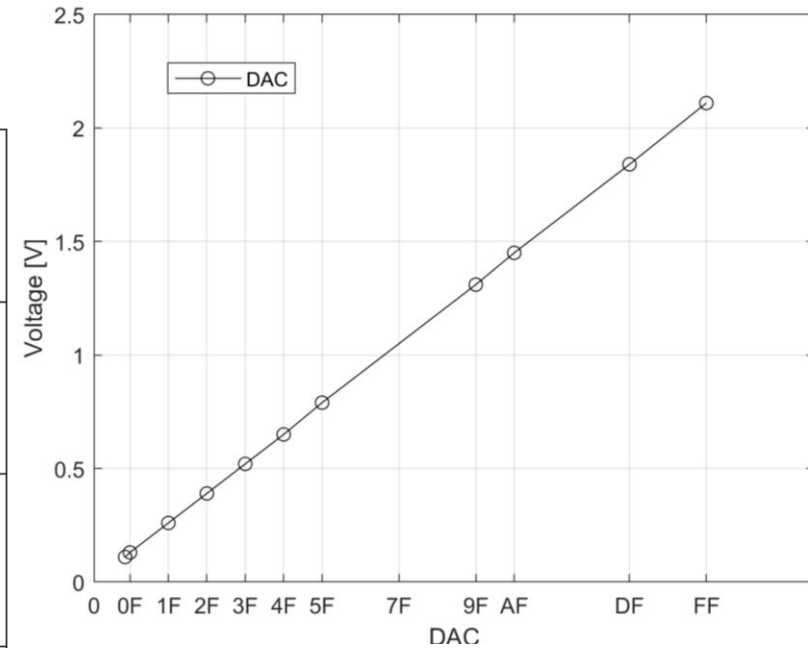
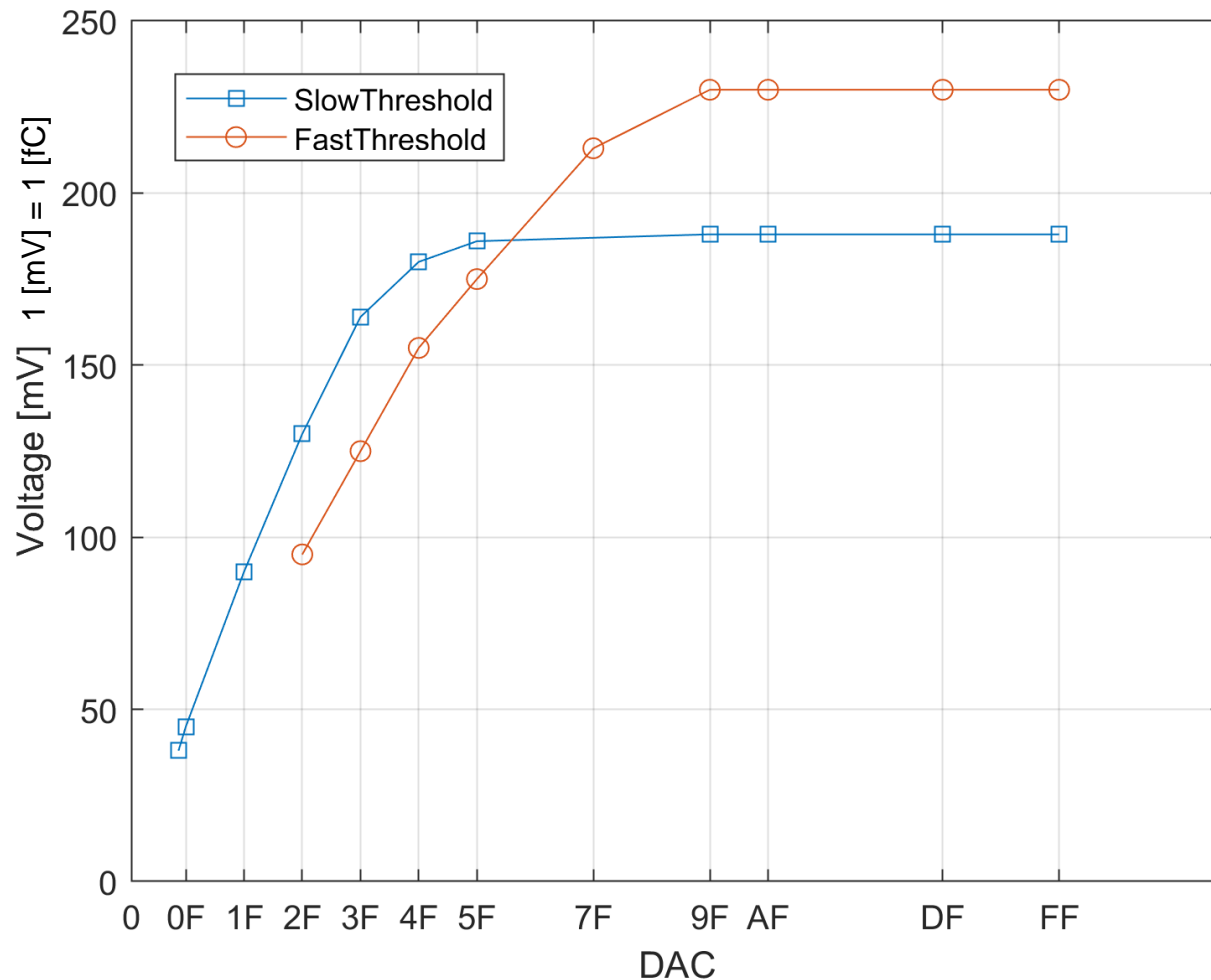
ToT_ch8_Slow	
Entries	6637933
Mean	68.81
Std Dev	0.8824
Underflow	0
Overflow	0
Integral	6.638e+06
Skewness	-0.2796

Windows taskbar: localhost:6543, 30508 Current Ev/s, 30033 Average Ev/s, 390 s, 11714591 Events, 2024-04-26 12:54:40

Windows taskbar: 12:54 PM 4/26/24

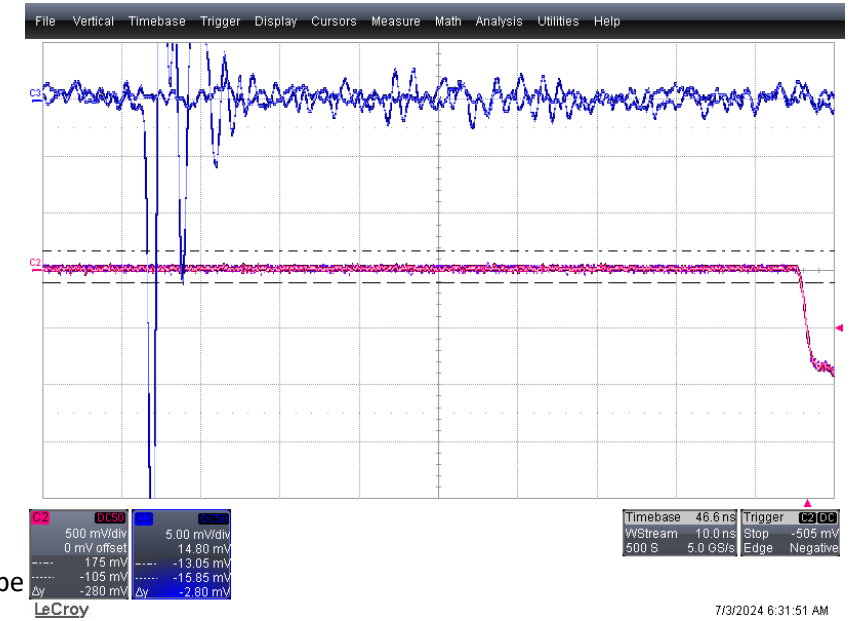
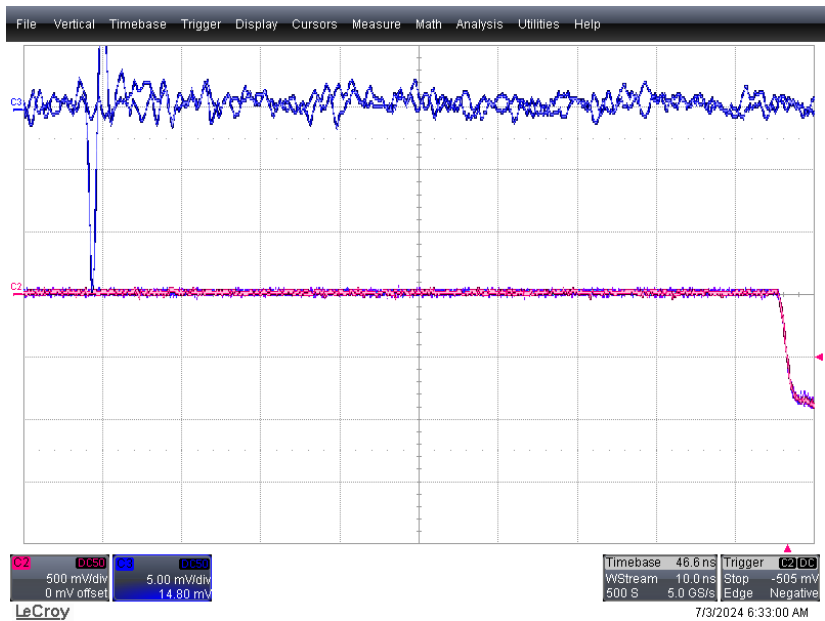
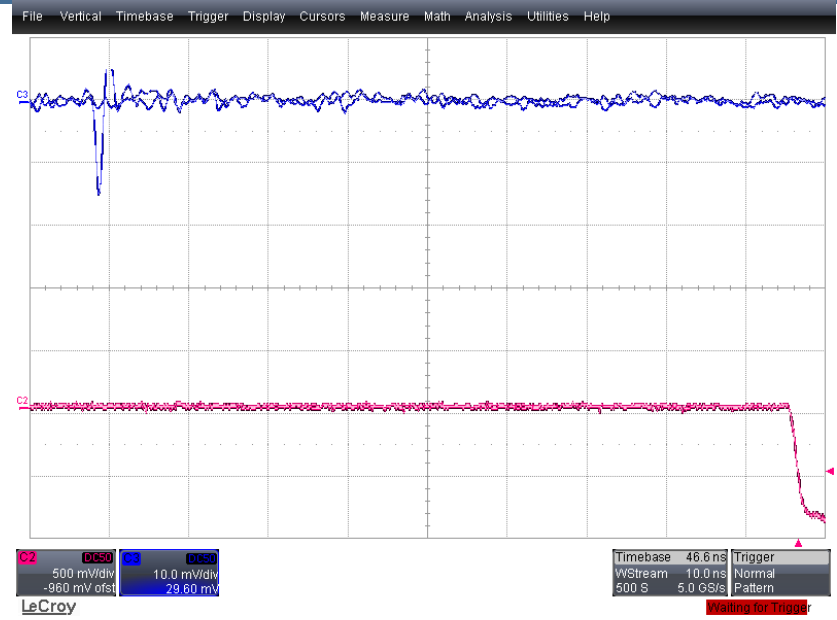
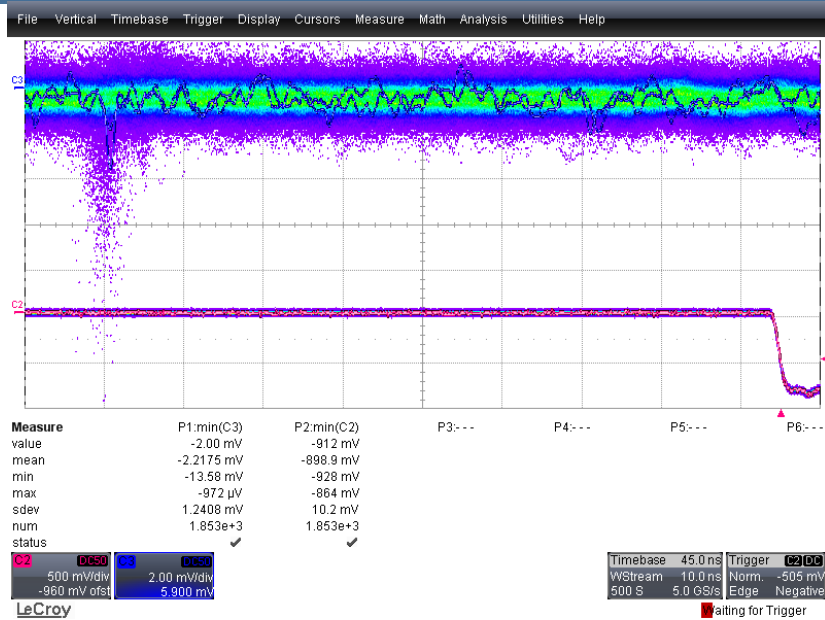


# Threshold for Fast and Slow FEE output

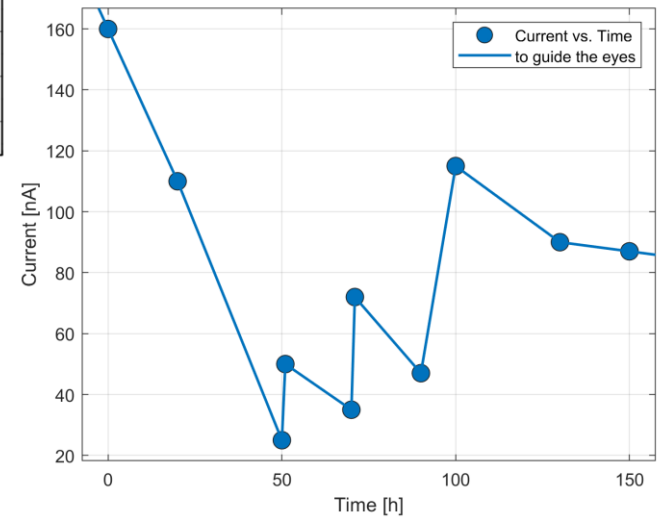
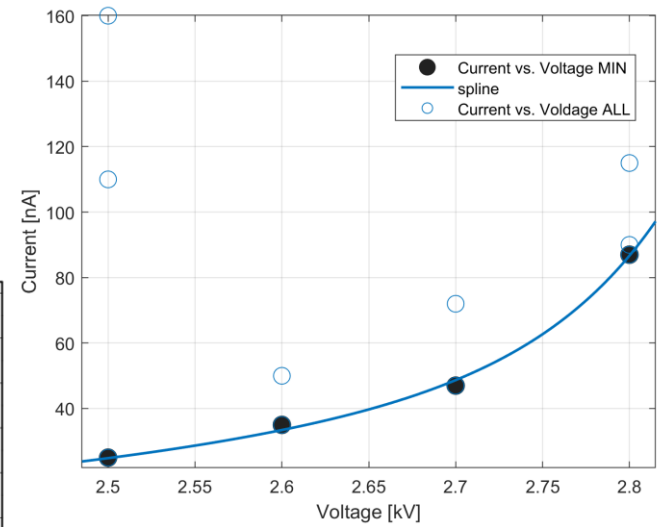
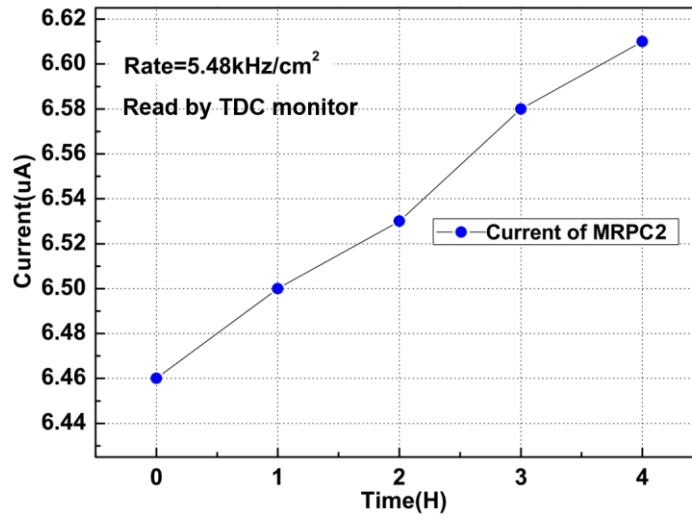
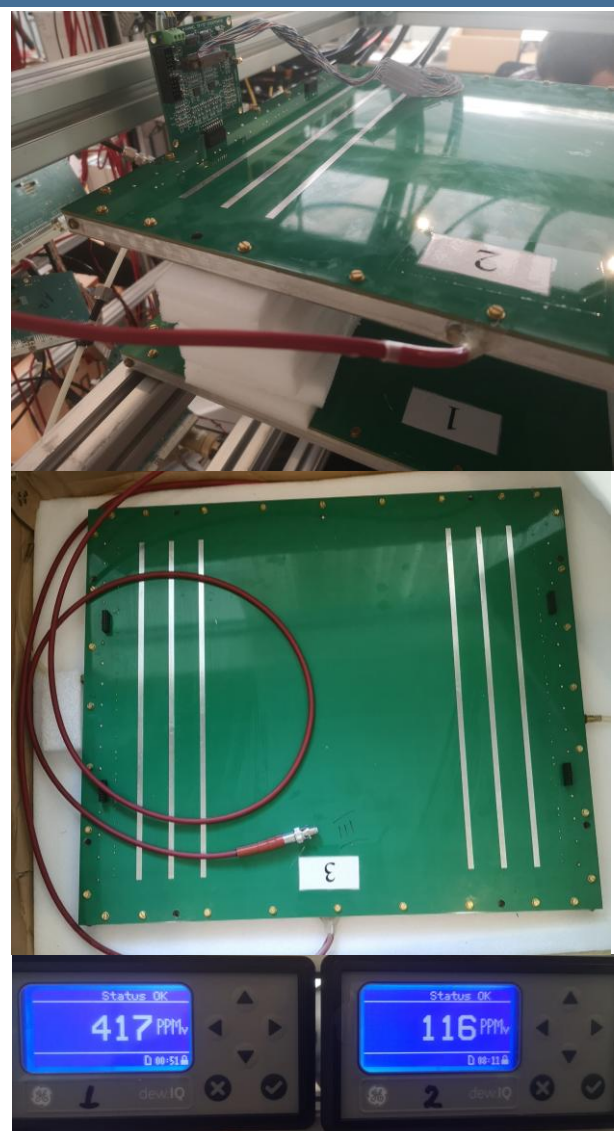


Counts on Fast and after for Slow channels becomes equal to triggers number (Threshold)

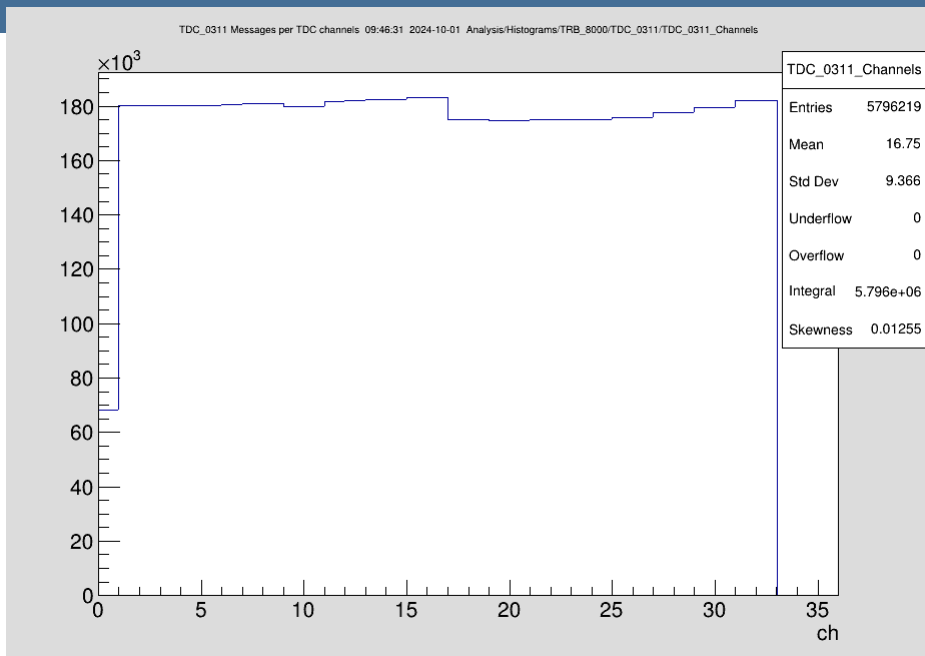
# Signals from MRPC



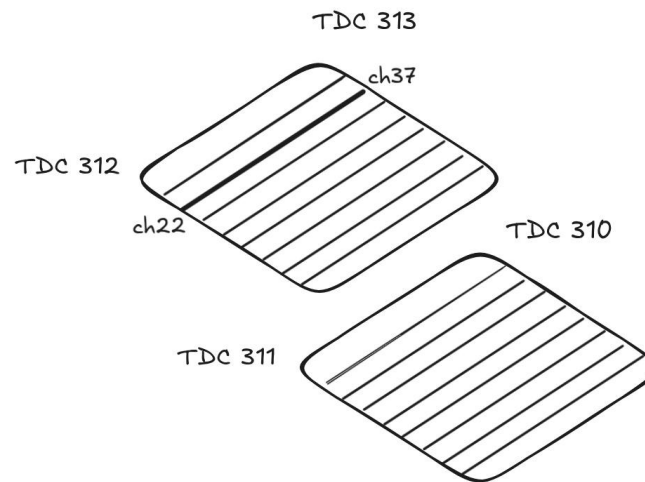
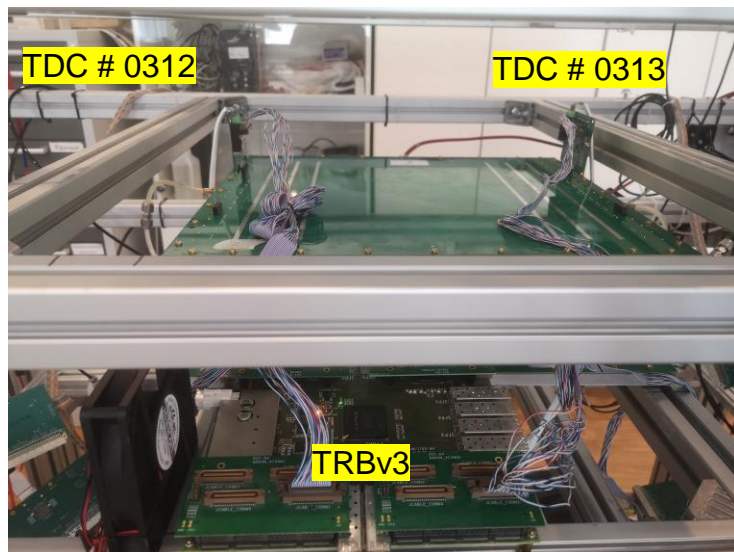
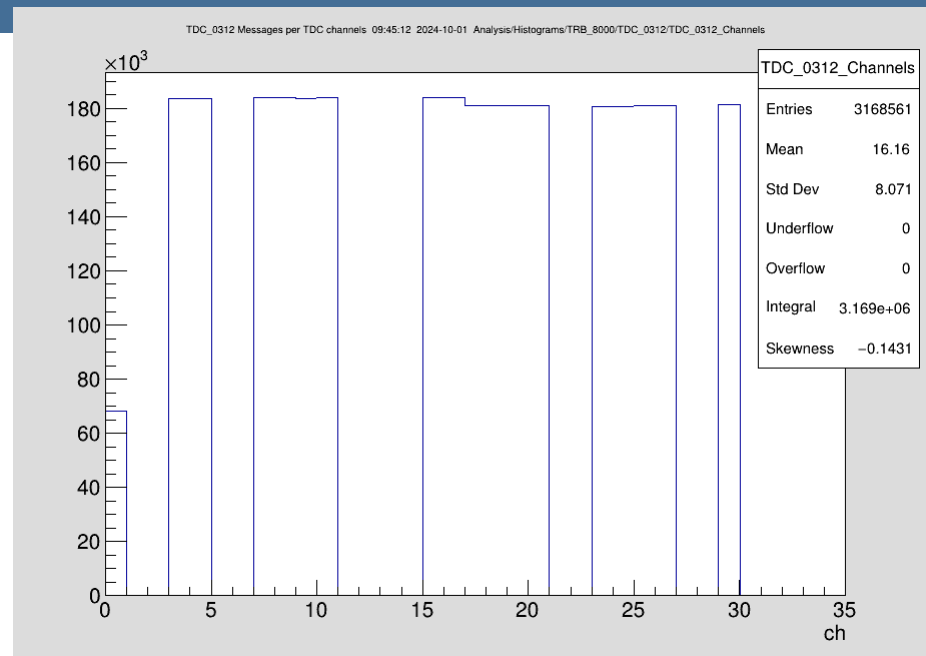
# IV of MRPC#2 from Protvino vs. Sealed (Yi Wang)



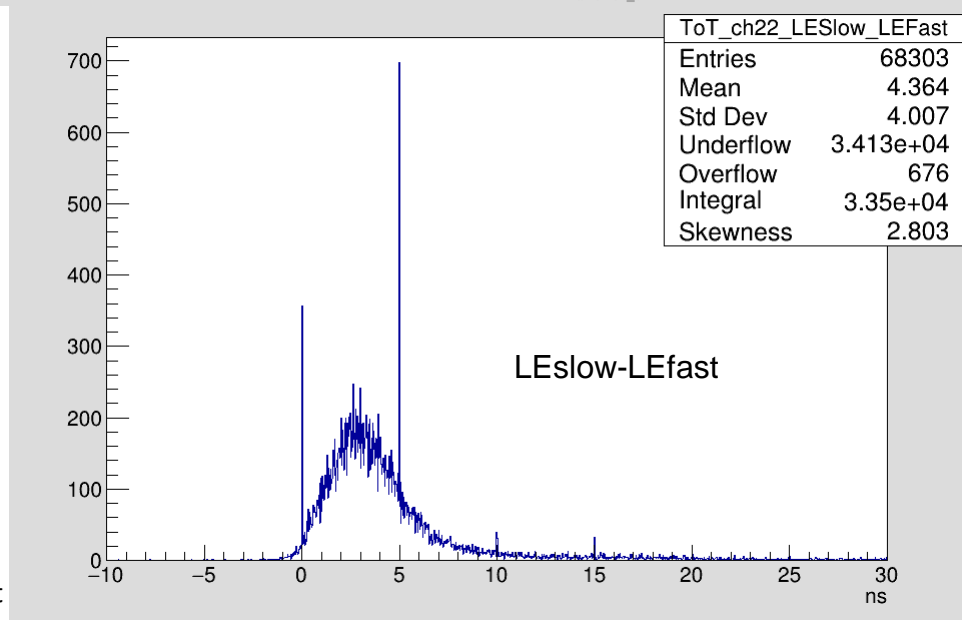
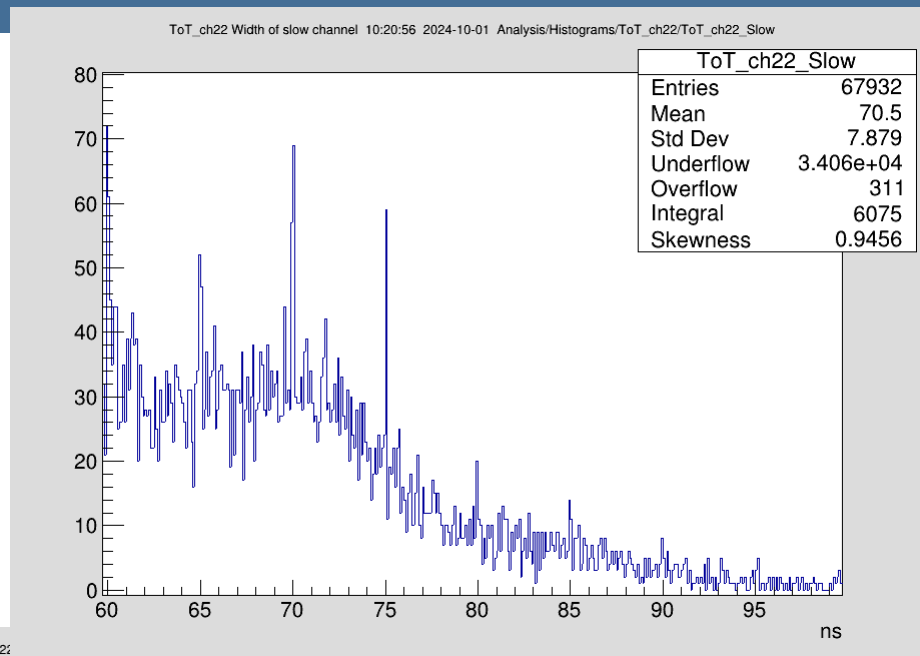
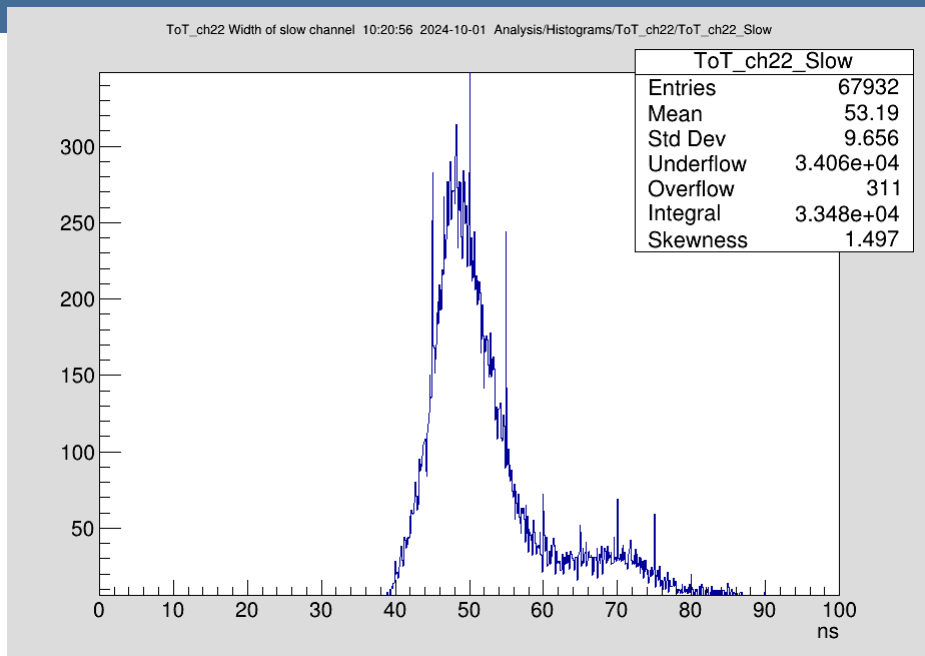
# TDC#0311



# TDC#0312



# CH#22 slow from TDC#0312



# Possible FEE and Digitization



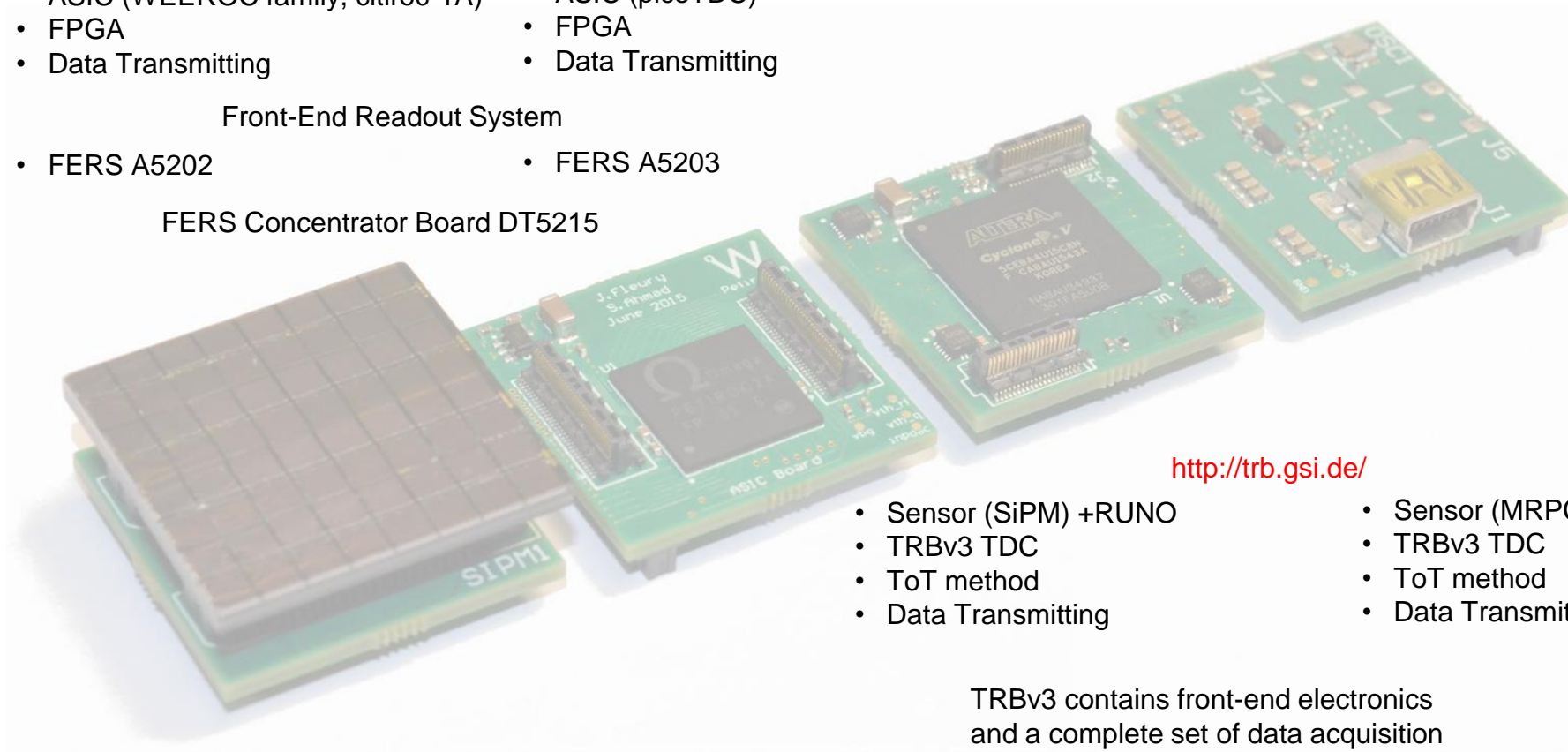
<https://www.caen.it/subfamilies/fers-5200/>

- |                                    |                        |
|------------------------------------|------------------------|
| • Sensor (SiPM)                    | • Sensor (MRPC) + NINO |
| • ASIC (WEEROC family, citiroc-1A) | • ASIC (picoTDC)       |
| • FPGA                             | • FPGA                 |
| • Data Transmitting                | • Data Transmitting    |

Front-End Readout System

- |              |              |
|--------------|--------------|
| • FERS A5202 | • FERS A5203 |
|--------------|--------------|

FERS Concentrator Board DT5215



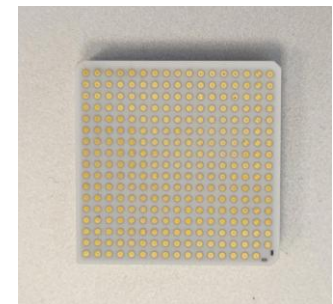
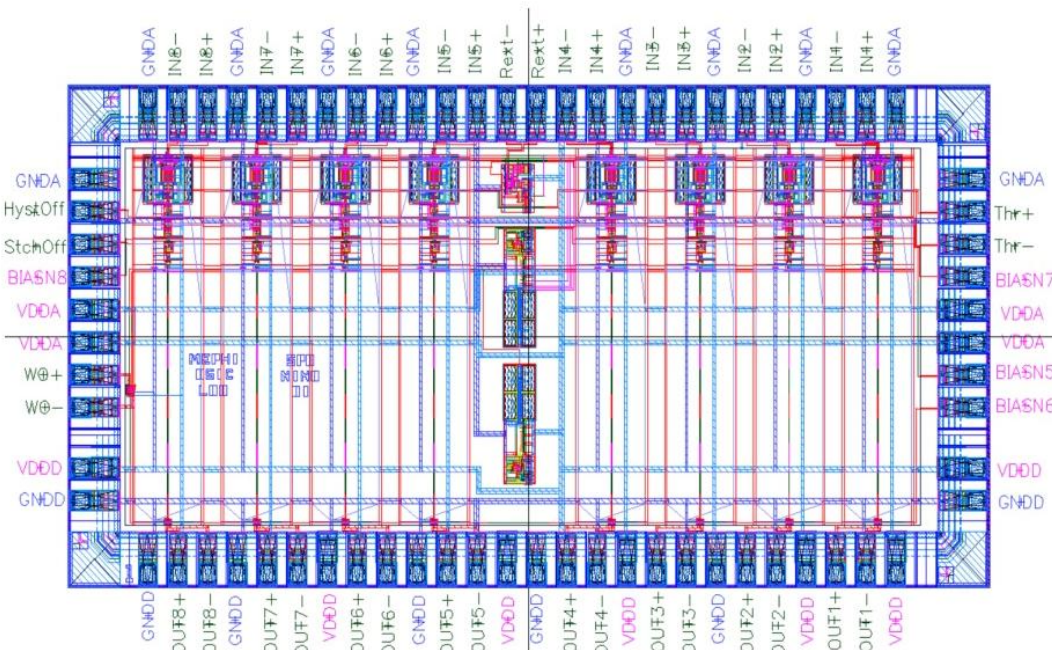
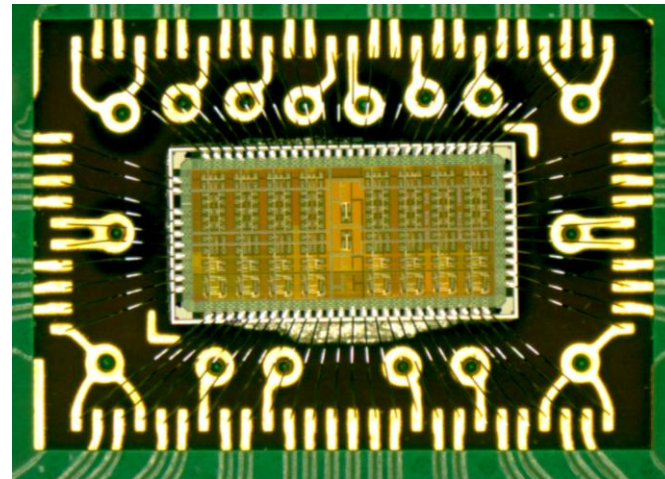
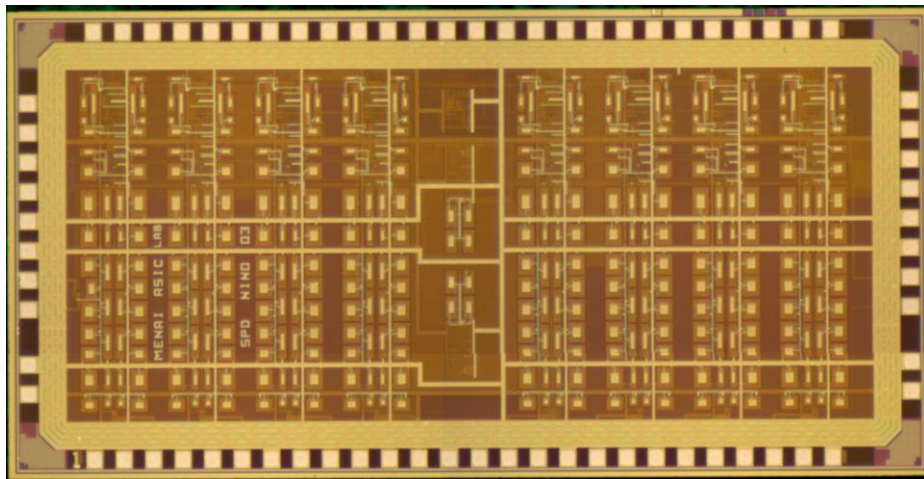
<http://trb.gsi.de/>

- |                       |                        |
|-----------------------|------------------------|
| • Sensor (SiPM) +RUNO | • Sensor (MRPC) + RUNO |
| • TRBv3 TDC           | • TRBv3 TDC            |
| • ToT method          | • ToT method           |
| • Data Transmitting   | • Data Transmitting    |

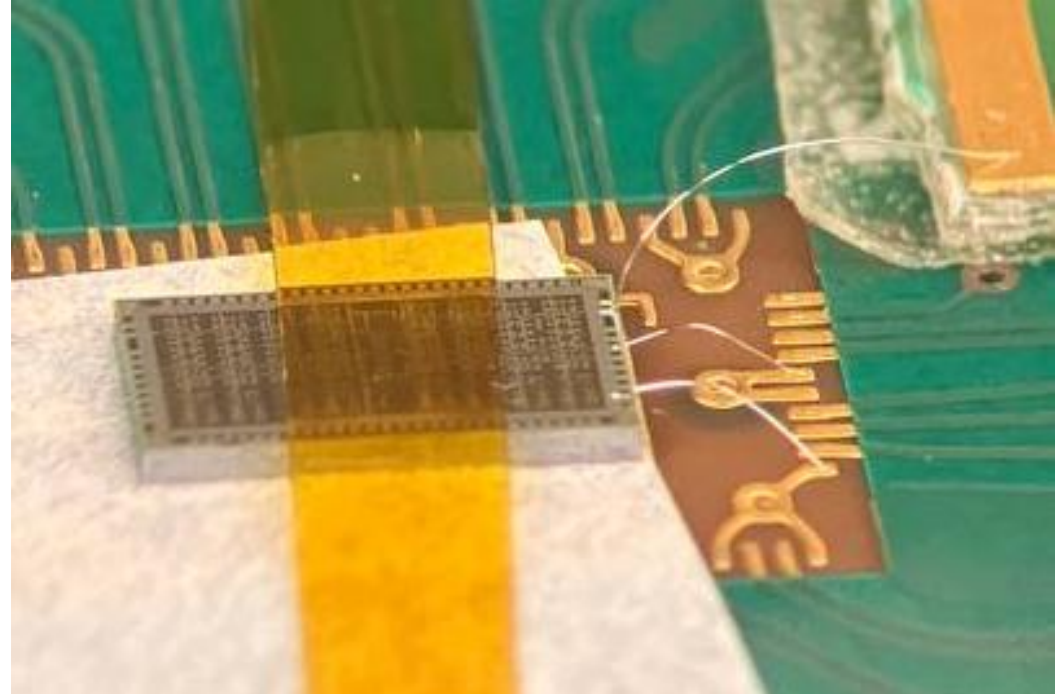
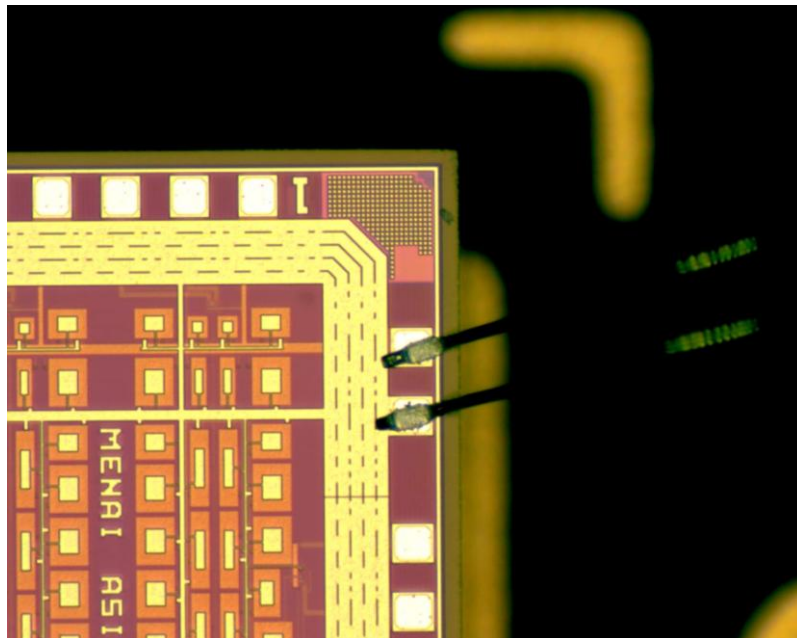
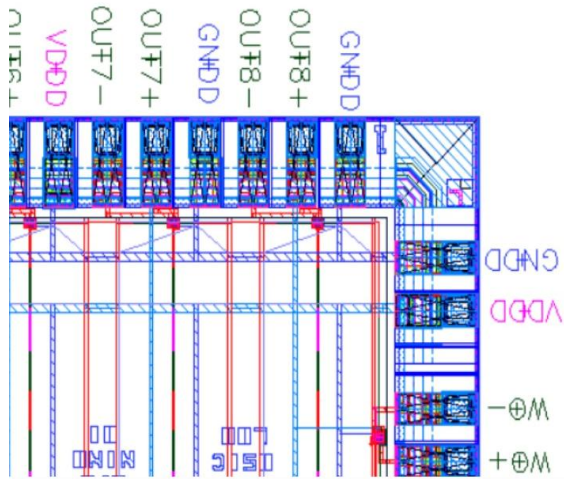
TRBv3 contains front-end electronics and a complete set of data acquisition and control software.

## FERS FERS+NINO vs. TRBv3 FPGA-TDC+RUNO

# RUNO



# RUNO



- RUNO has very low impedance on power line
- VddA and VddD are short-circuited
- GND D and GNDA as well
- We need some time to relax and enjoy the life



# F. Garzetti et al.: TDC IP-Core for FPGA at State of the Art

**TABLE 1. Most significant implementations of TDL-TDCs in Xilinx FPGA devices, sorted by resolution (LSB).**

Reference	FPGA device	Tech. Node	LSB	$\sigma_{CH}$	FSR	DNL	INL	Ch. Rate
[23]	Virtex-6	40-nm	10.0 ps	19.6 ps r.m.s.	N.A.	15.0 ps	22.5 ps	N.A.
[24]	Virtex-5	65-nm	16.3 ps	N.A.	N.A.	48.9 ps	81.5 ps	N.A.
[25]	Virtex-6	40-nm	1.70 ps	4.2 ps r.m.s.	N.A.	1.36 ps	1.70 ps	N.A.
[26]	Kintex-7	28-nm	17.6 ps	12.7 ps r.m.s.	N.A.	17.6 ps	15.3 ps	N.A.
[27]	Virtex-6	40-nm	10.0 ps	10.0 ps r.m.s.	N.A.	19.1 ps	22.0 ps	N.A.
[28]	Kintex-7	28-nm	10.6 ps	8.13 ps r.m.s.	N.A.	10.6 ps	45.6 ps	N.A.
[28]	Virtex-6	40-nm	10.1 ps	9.82 ps r.m.s.	N.A.	11.9 ps	33.3 ps	N.A.
[28]	Spartan-6	40-nm	16.7 ps	12.8 ps r.m.s.	N.A.	20.4 ps	42.4 ps	N.A.
[29]	UltraScale	20-nm	2.25 ps	3.90 ps r.m.s.	N.A.	N.A.	N.A.	N.A.
[30]	Virtex-5	65-nm	7.40 ps	6.80 ps r.m.s.	N.A.	5.48 ps	11.6 ps	N.A.
[31]	Virtex-7	28-nm	1.15 ps	3.50 ps r.m.s.	N.A.	4.03 ps	6.79 ps	N.A.
[12]	Virtex-7	28-nm	10.5 ps	14.6 ps r.m.s.	N.A.	0.84 ps	1.16 ps	N.A.
[12]	UltraScale	20-nm	5.02 ps	7.80 ps r.m.s.	N.A.	0.60 ps	2.31 ps	N.A.
[32]	Virtex-5	65-nm	18.0 ps	25.0 ps r.m.s.	10.7 s	N.A.	N.A.	5 MHz
[33]	Artix-7	28-nm	10.0 ps	15 ps r.m.s.	10.7 s	N.A.	N.A.	10 MHz
[34]	Artix-7	28-nm	250 fs	12 ps r.m.s.	10.3 s	N.A.	4.2 ps	20 MHz
[35]	Artix-7	28-nm	250 fs	12 ps r.m.s.	10.3 s	33 fs	4.6 ps	45 MHz
[36], [37]	Zynq-7000	28-nm	2 ps	12 ps r.m.s.	10.7 s	N.A.	N.A.	45 MHz
[38]	UltraScale	20-nm	305 fs	8.5 ps r.m.s.	10.2 $\mu$ s	N.A.	N.A.	50 MHz
[39]	Spartan-6	40-nm	7.70 ps	8.90 ps r.m.s.	N.A.	22.3 ps	67.8 ps	40 MHz
[40]	Virtex-7	28-nm	6.00 ps	7.00 ps r.m.s.	2.1 s	N.A.	N.A.	125 MHz

**TABLE 14. Implementation results and measurements. In particular, Artix-7 column refers to the device selected for testing the IP-Core.**

Performance	Artix-7	Virtex-5	Spartan-6	Kintex-7	Zynq-7000	Kintex UltraScale
Resolution	366 fs	18 ps	25 ps	250 fs	2 ps	305 fs
Precision	8.0 ps r.m.s.	25.0 ps r.m.s.	17 ps r.m.s.	8.0 ps r.m.s.	12 ps r.m.s.	8.5 ps r.m.s.
Full Scale Range	10.3 s	10.7 s	640 ns	10.3 s	10.7 s	10.2 $\mu$ s
DNL	250 fs	N.A.	N.A.	200 fs	1.4 ps	N.A.
INL	2.5 ps	N.A.	N.A.	2.2 ps	5 ps	N.A.
Number of Channels	16	16	4	16	8	24
Channel Rate	150 MHz	5 MHz	N.A.	150 MHz	45 MHz	50 MHz
Dead-Time	5 ns	N.A.	N.A.	5 ns	20 ns	N.A.
Temperature Sensitivity	286 fs/ $^{\circ}$ C	N.A.	N.A.	N.A.	N.A.	N.A.

# Master of Science Thesis in Electrical Engineering

## A 1.8 ps Time-to-Digital Converter (TDC) Implemented in a 20 nm Field-Programmable Gate Array (FPGA) Using a Ones-Counter Encoding Scheme with Embedded Bin-Width Calibrations and Temperature Correction:

Sven Engström  
LiTH-ISY-EX--20/5343--SE

### 5.1 Resolution

The best resolution of 1.8 ps was achieved using external calibration in combination with the pulsed edge mode. This result is better than previously published FPGA-based TDCs [6]. A small comparison to previous works can be seen in table 5.1.

Ref.-Year	Device	Method	Precision	Resources
[11]-14	Spartan-6	Wave union across multiple TDLS	6 ps	144 SLICES
[10]-15	Virtex-6	Average multiple TDCs	4.2 ps	–
[9]-17	Virtex-7	Average multiple TDCs	3.5 ps	12758 LUTs
[2]-16	Kintex-7	Average multiple TDCs, wave union	3.1 ps	–
[13]-17	Kintex-7	Multiple TDLS, ones-counter	3.9 ps	2433 LUTs
[5]-16	Kintex UltraScale	Dual sampling	3.9 ps	–
This work	Kintex UltraScale	Internal calibration, dual sampling, ones-counter	2.5 ps	1972 LUTs
		Wave union, dual sampling, ones-counter	1.8 ps	

**Table 5.1:** Comparison of recent, high resolution, FPGA-based TDCs

The only way to do great work is to love what you do. © S.J.



- Artem Semak, Evgeni Ladygin



- Sergei Morozov, Evgeni Usenko



- Artem Ivanov

- Vladimir Ladygin, Aleksey Tishevsky

- Vadim Babkin, Mikhail Buryakov, Oleg Tarasov



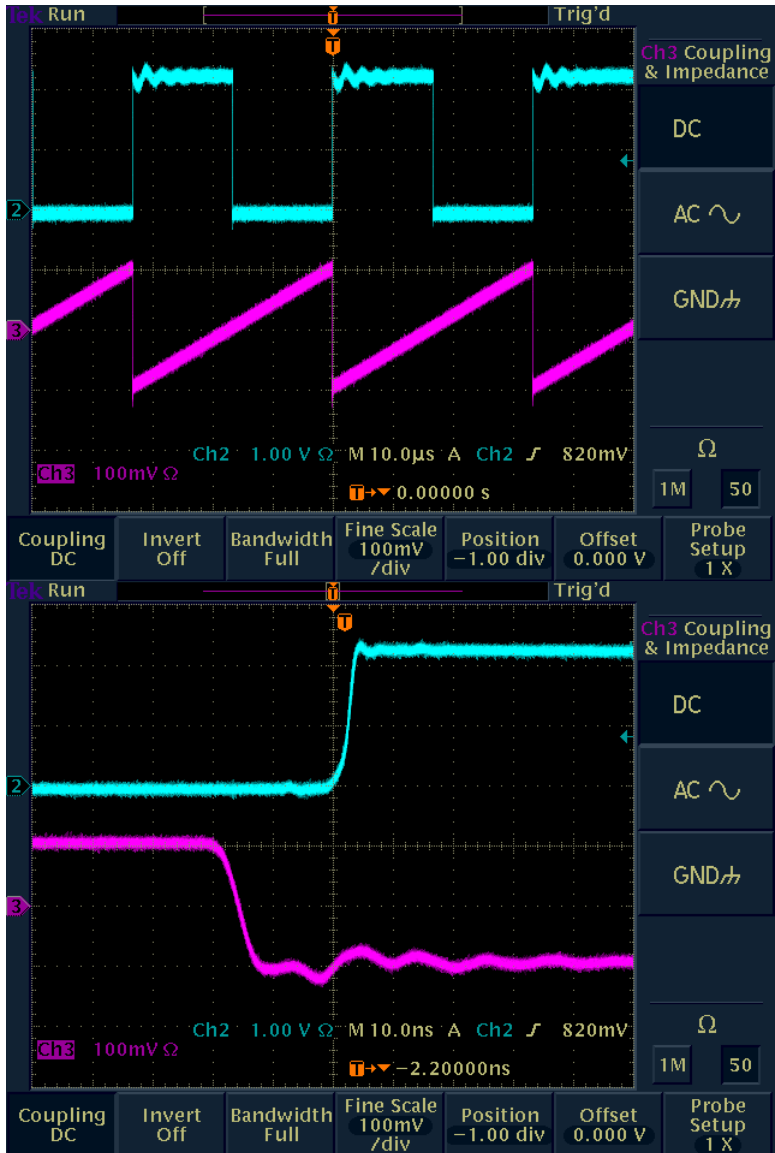
- Yi Wang at al.

**Thank you for your attention**

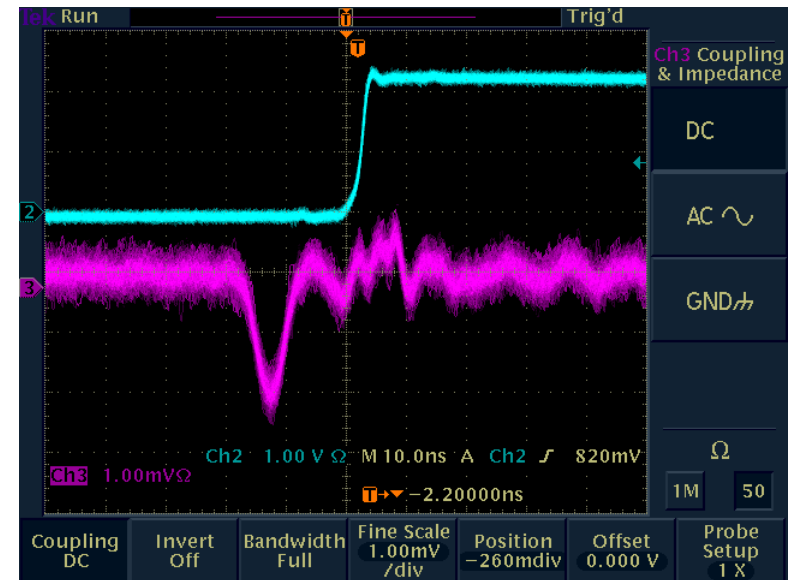
# Spare slides



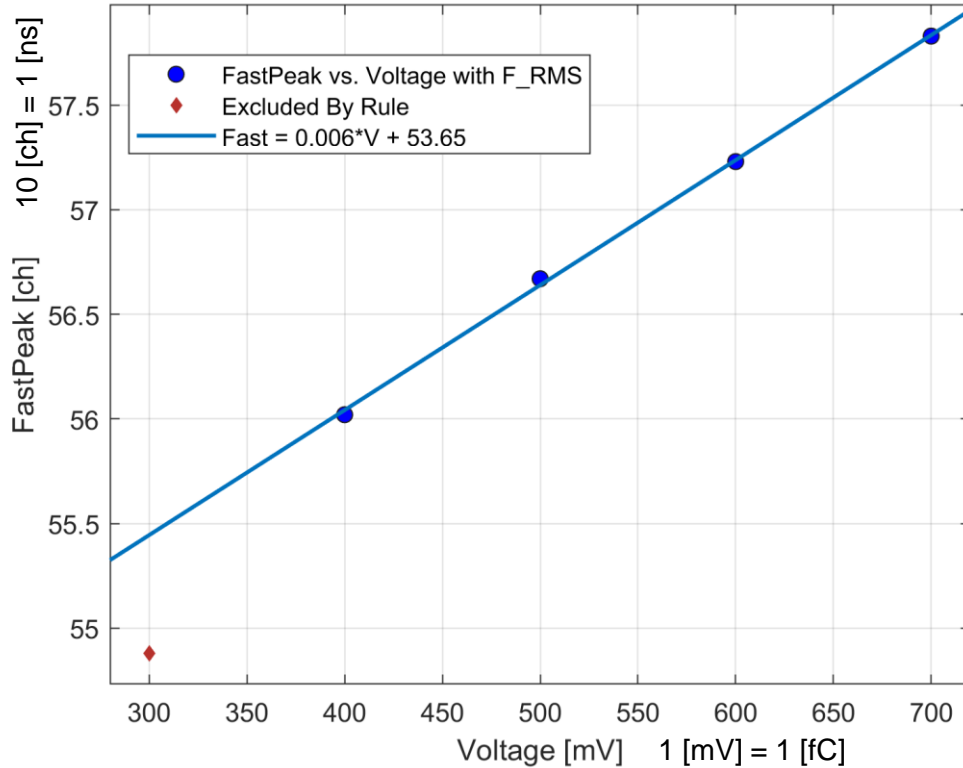
# Test signal forming chains and key parameters



1 pF diff capacitance  $\rightarrow$  200mV = 200 fC

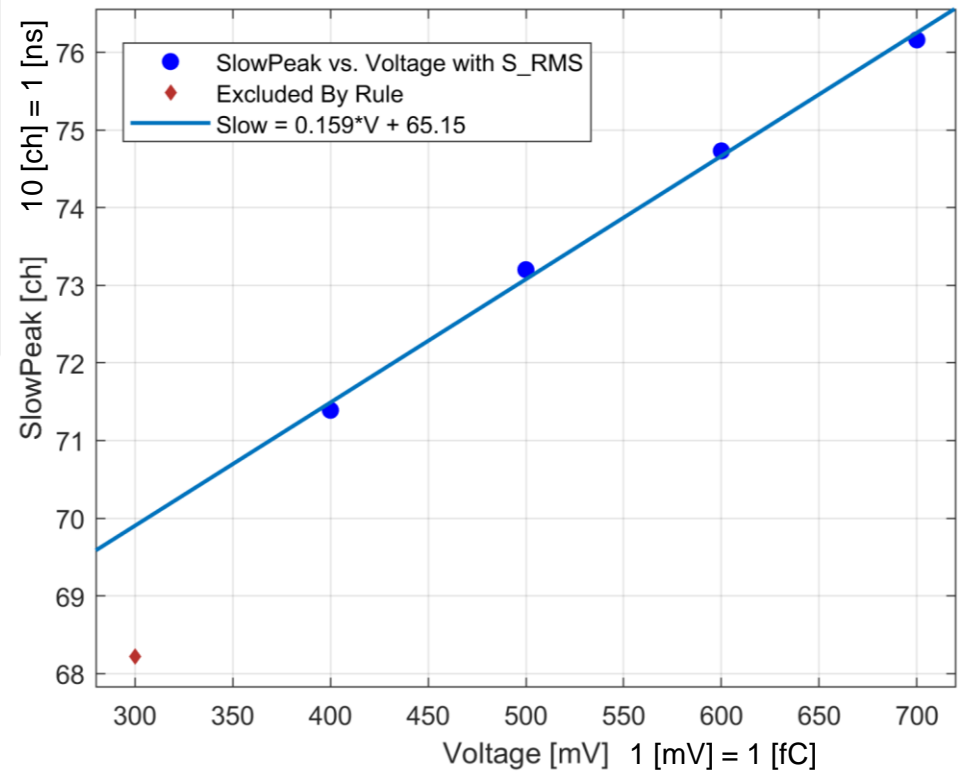


# Linear response to test signal for Fast and Slow output

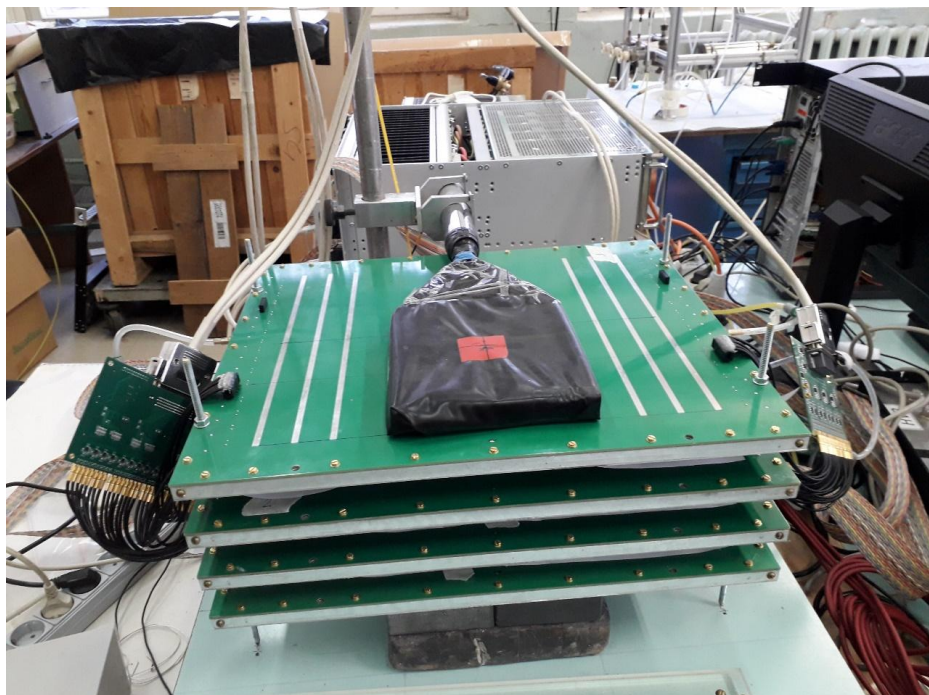


Fast peak width 5.5-6ns STD<100ps

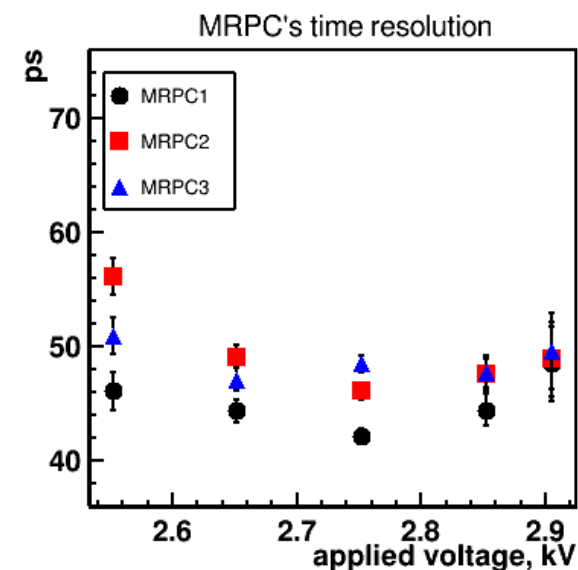
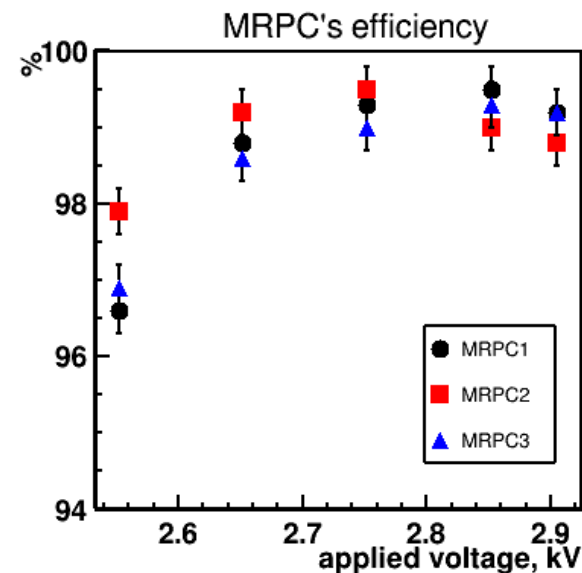
Slow peak width 7-7.6ns STD<90ps



# Protvino MRPC prototype for SPD project at NICA



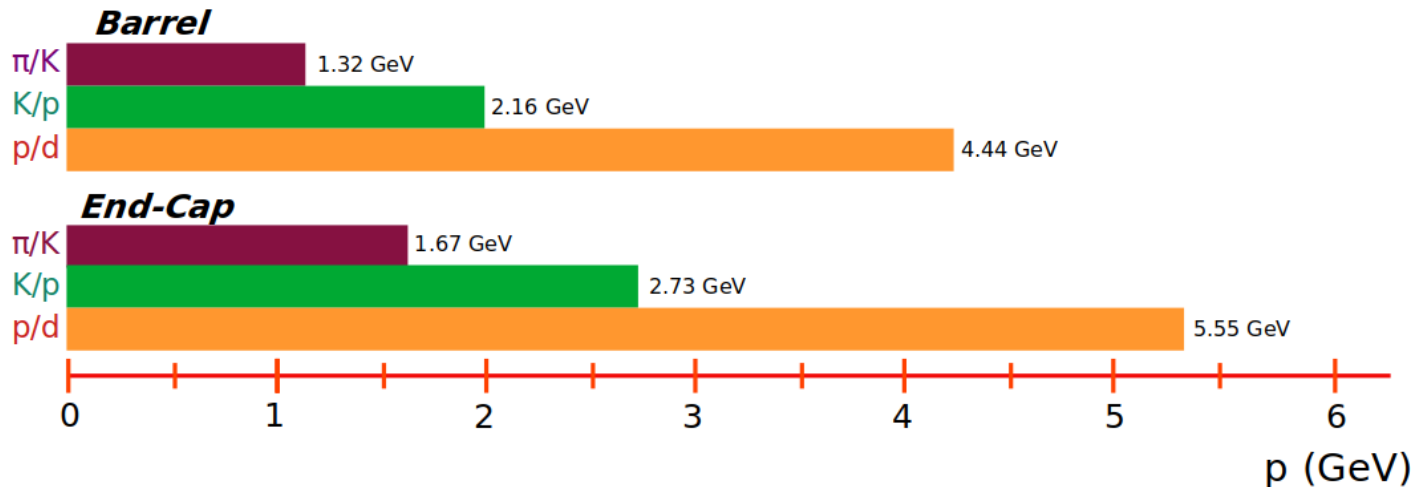
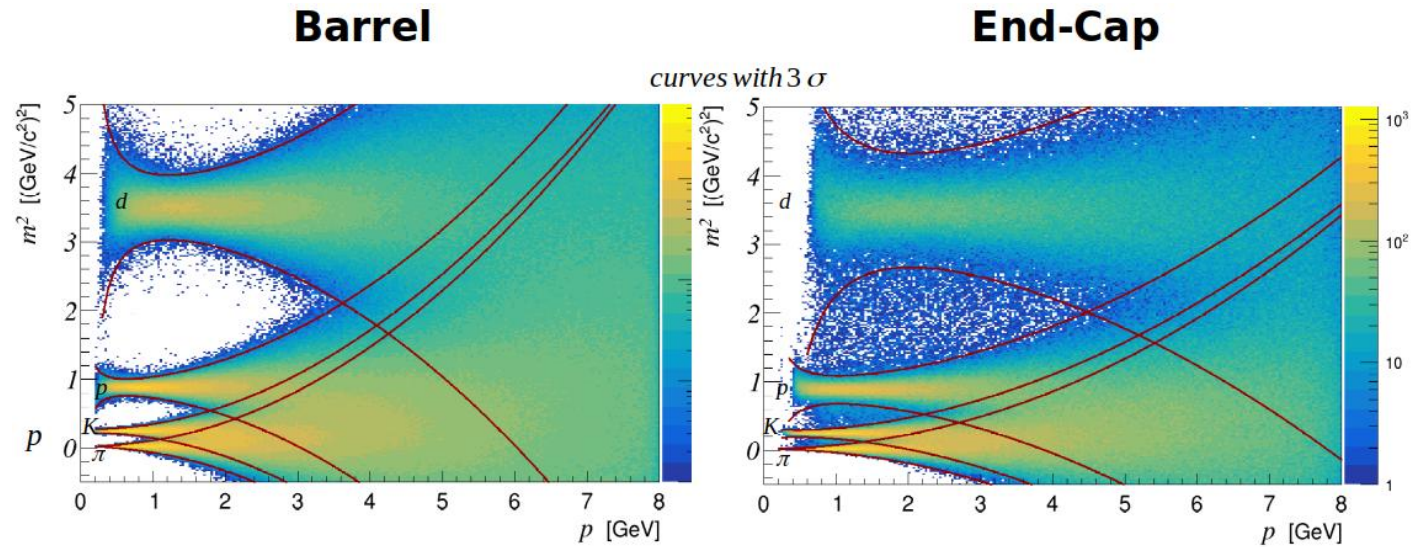
- To start MRPC and check functionality
- To obtain detection efficiency and time resolution on a new DAQ
- Preparation for using 3 MRPC as a servicing system at TEST AREA (Anton Baldin).



# Particles ID for $m^2$ vs. $p$



- $\pi/K/p/d$  discrimination for momenta  $< 2$  GeV
- Determination of  $t_0$
- Time resolution requirement  $< 60$  ps.

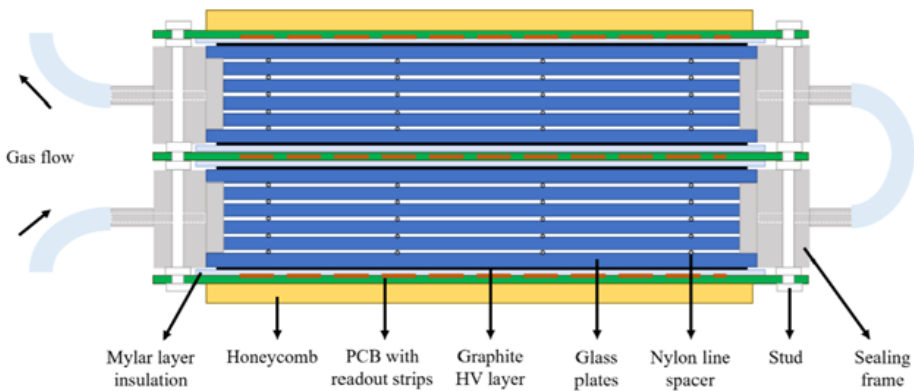




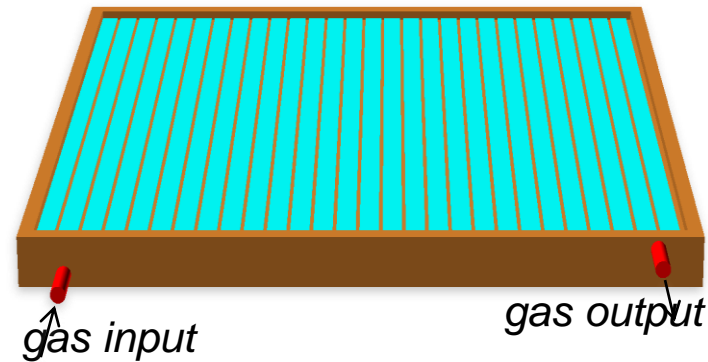
# Sealed MRPC for SPD TOF



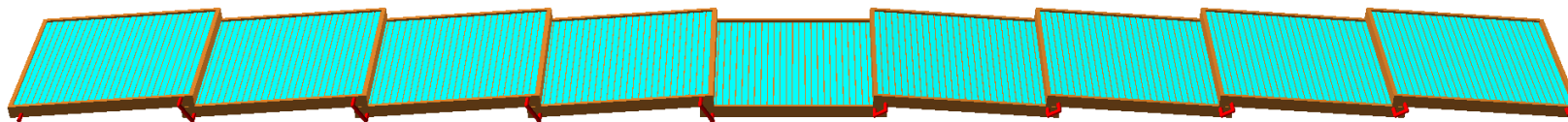
(B.Wang et al, JINST 15 (2020) 08, C08022)



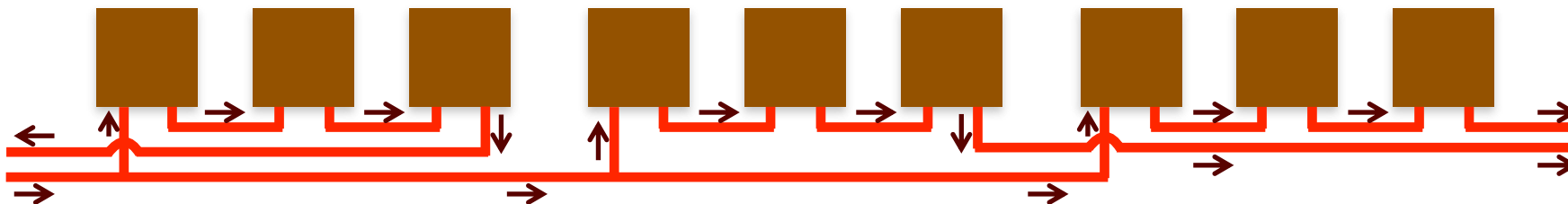
Sealed MRPC proposed for CBM-TOF



Sealed MRPC proposed for SPD-TOF



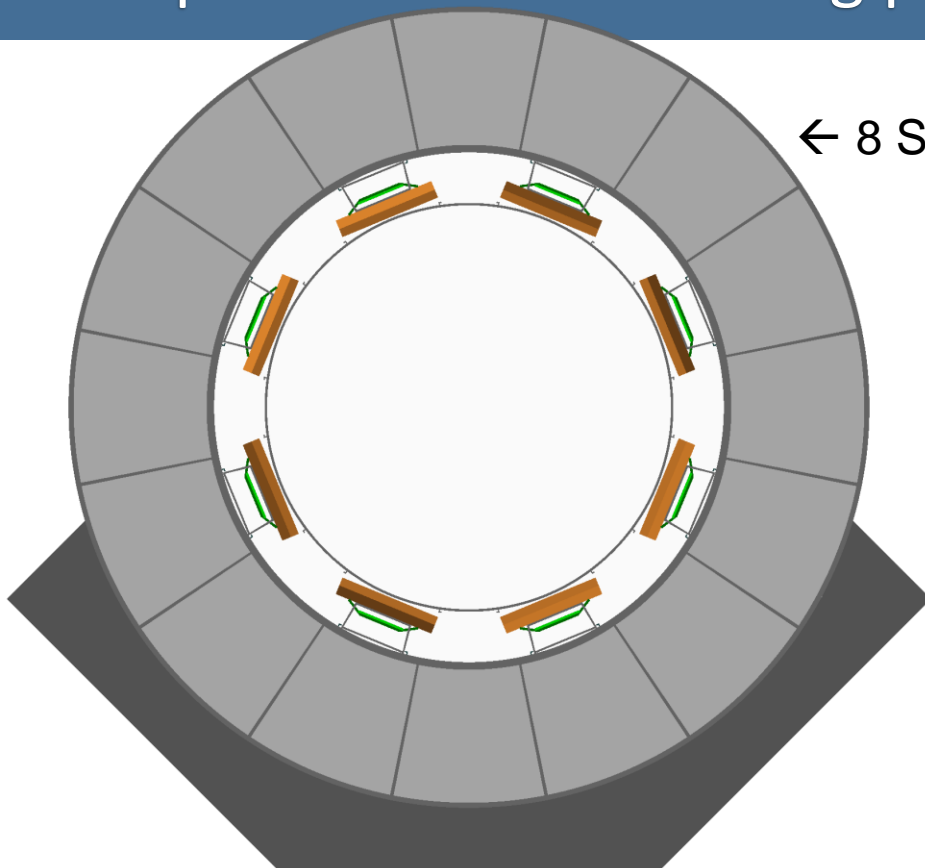
Serial gas connection of MRPCs in a single super module



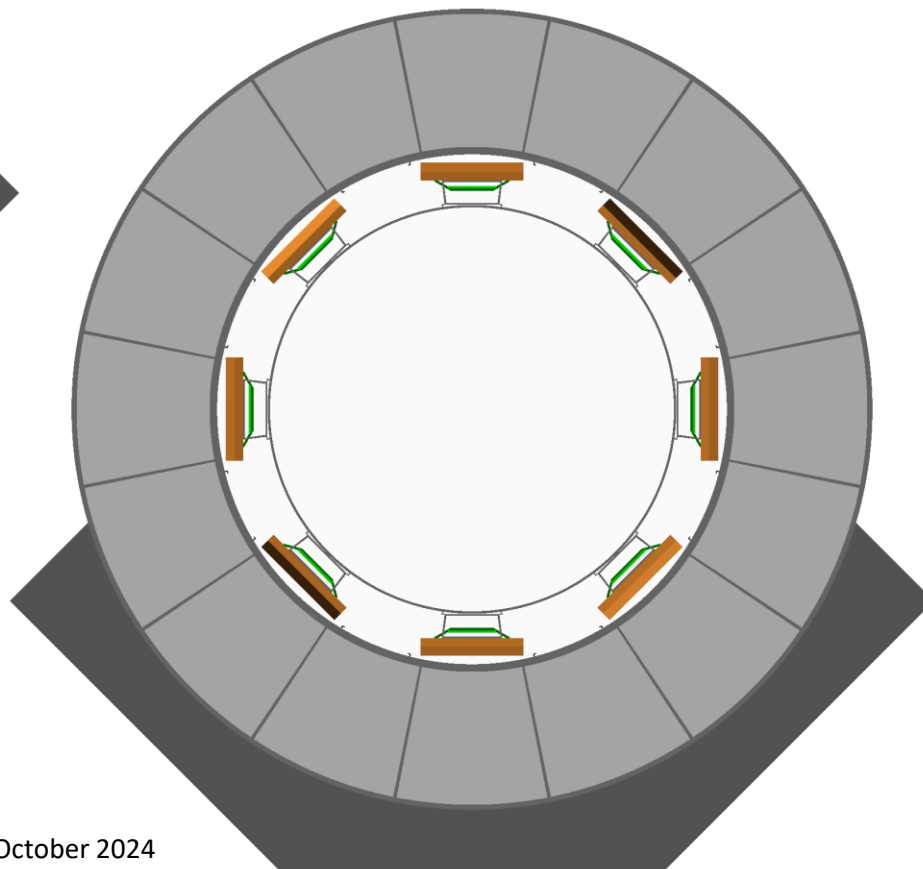
# Super modules mounting proposal



← 8 Super modules mounting on e-Calorimeter



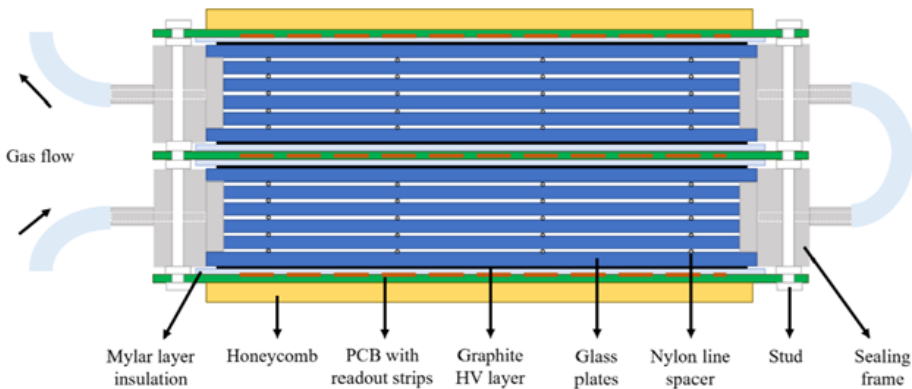
8 Super modules mounting on Straw crate →



# Sealed (MRPC) are the base option of today



(B.Wang et al, JINST 15 (2020) 08, C08022)



- The prototype was tested in cosmic rays along with 2 MRPC2 counters in the TRBv3 test stand.
- The plateau efficiency is 97%, with a 1.6 cluster size and a 100 ps flight-time resolution.
- The systematic time resolution of the prototype is about 60 ps. if we reasonably expect the same timing precision between two MRPCs.
- The prototype has the same working point at  $\pm 5.4$  kV with standard gas flow (Freon/ $iC_4H_{10}$  = 90/5/5)

