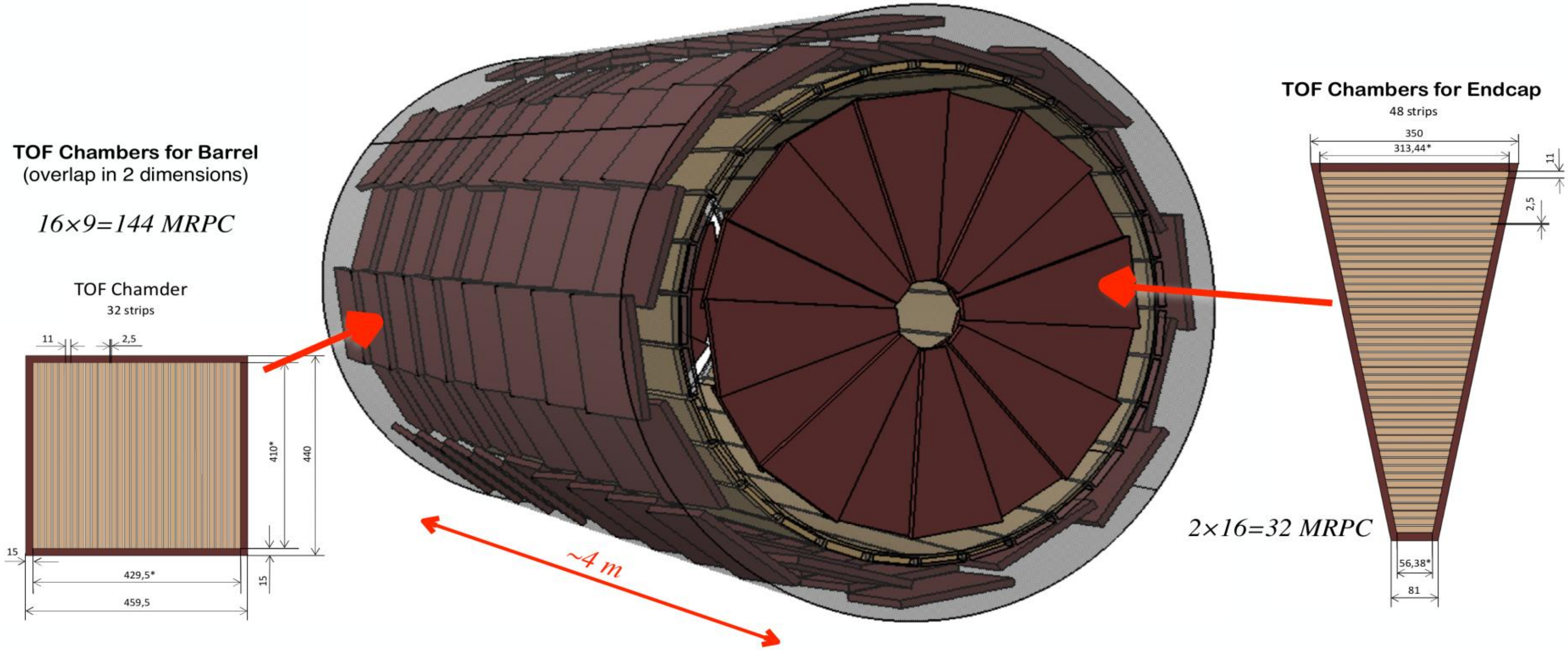
Time of Flight Detector
Status Report

Valery Chmill

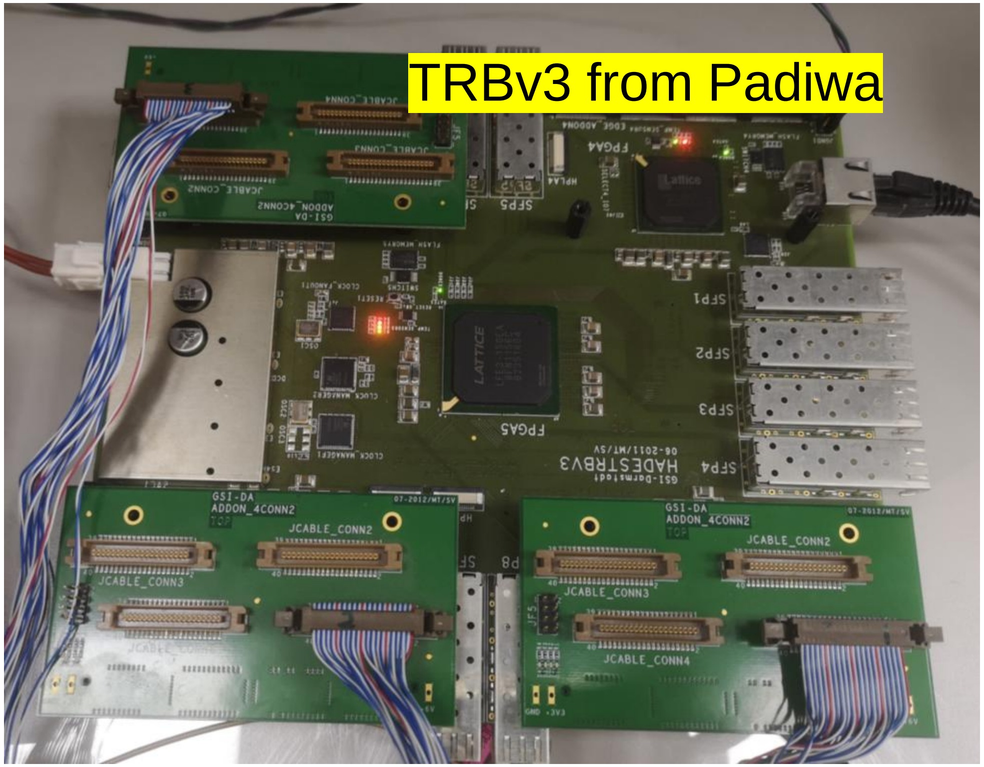
Time of Flight (TOF) detector proposal

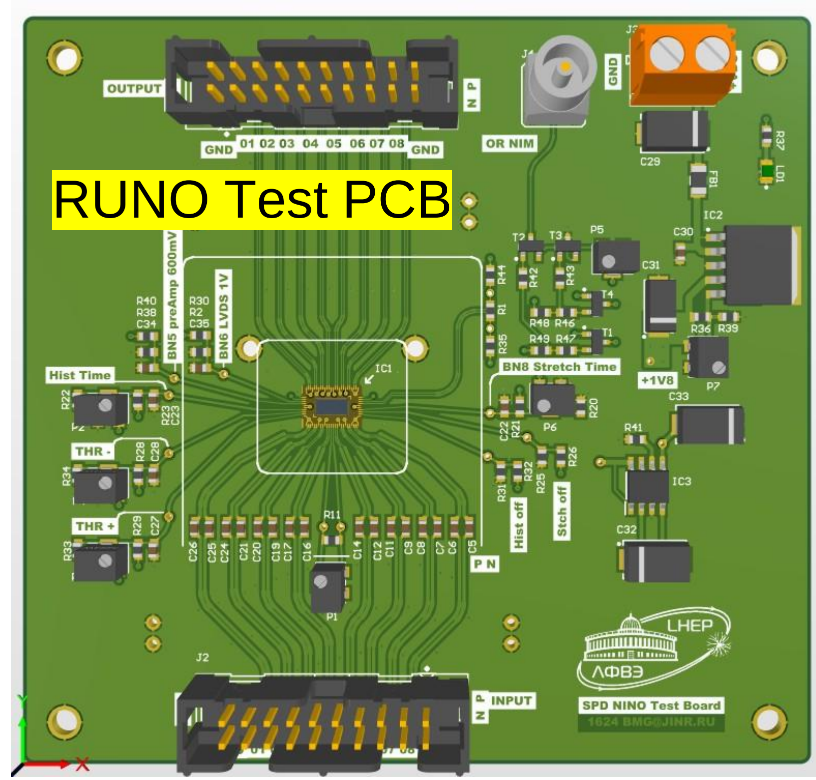


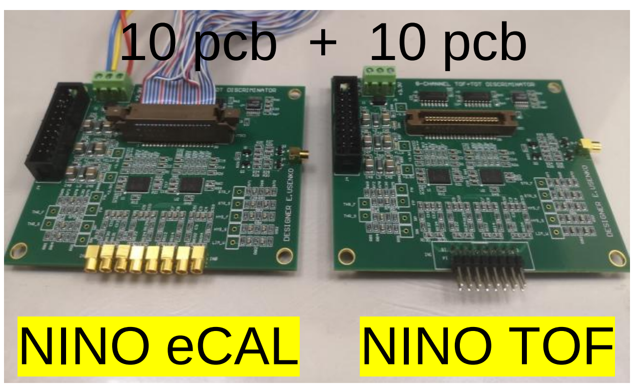
- π/K/p discrimination for momenta ≲2 GeV
- Determination of t0
- Time resolution requirement <60 ps.
- Sealed (MRPC) are the base option. B.Wang et al, JINST 15 (2020) 08, C08022

- Number of readout for Barrel is 144x2x32=9216 channels.
- Number of readout for Endcap is 32x2x48=3072 channels.
- Total amount is 12288 channels

DAQ (TRBv3) preparation and FEE news







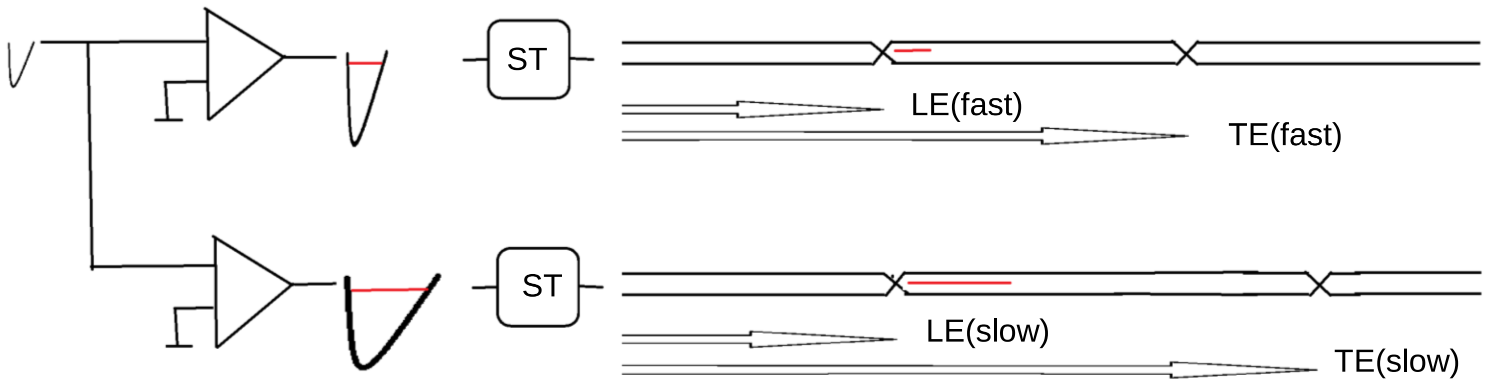
TDC-Readout-Board, Triggered/Triggerless-Readout-Board

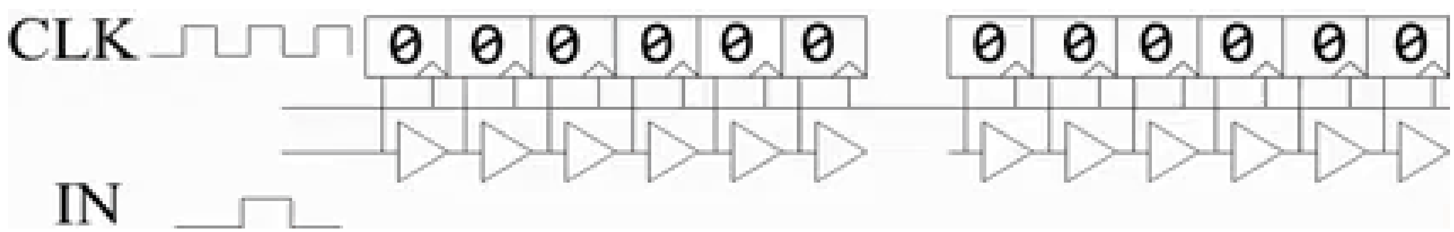
Item	Value
Supply Voltage	48 V (40-50V), galvanically isolated on board
Power Supply Current	0.5A minimum without AddOns
GbE-connectivity	max. 95 MBytes/s transfer per link
GbE-slow-control	up to 400 registers/transfer, speed depends on GbE latency
Connectivity	Max. 8 SFPs, each 2GBit/s on board. With hub-addon: max. 32 SFP
	4 AddONs on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate	about 300 kHz (depending on configuration and network size)
Max Hit Rate	50 MHz (burst of 63 hits)
TDC Channels	260 (Single edge detection)
Time Precision	<20 ps
Minimum pulse width	<500 ps

32ch!

TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

TDC on FPGA, TRB3 FEE from PADIWA

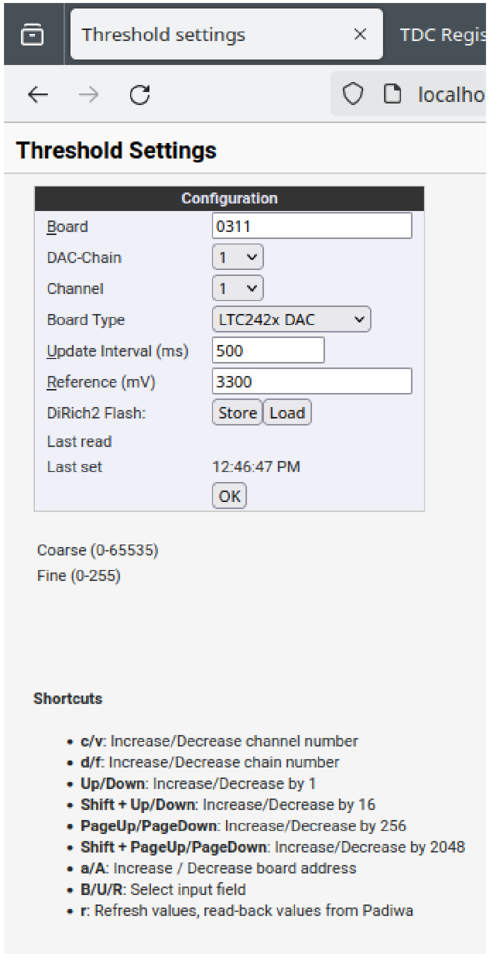


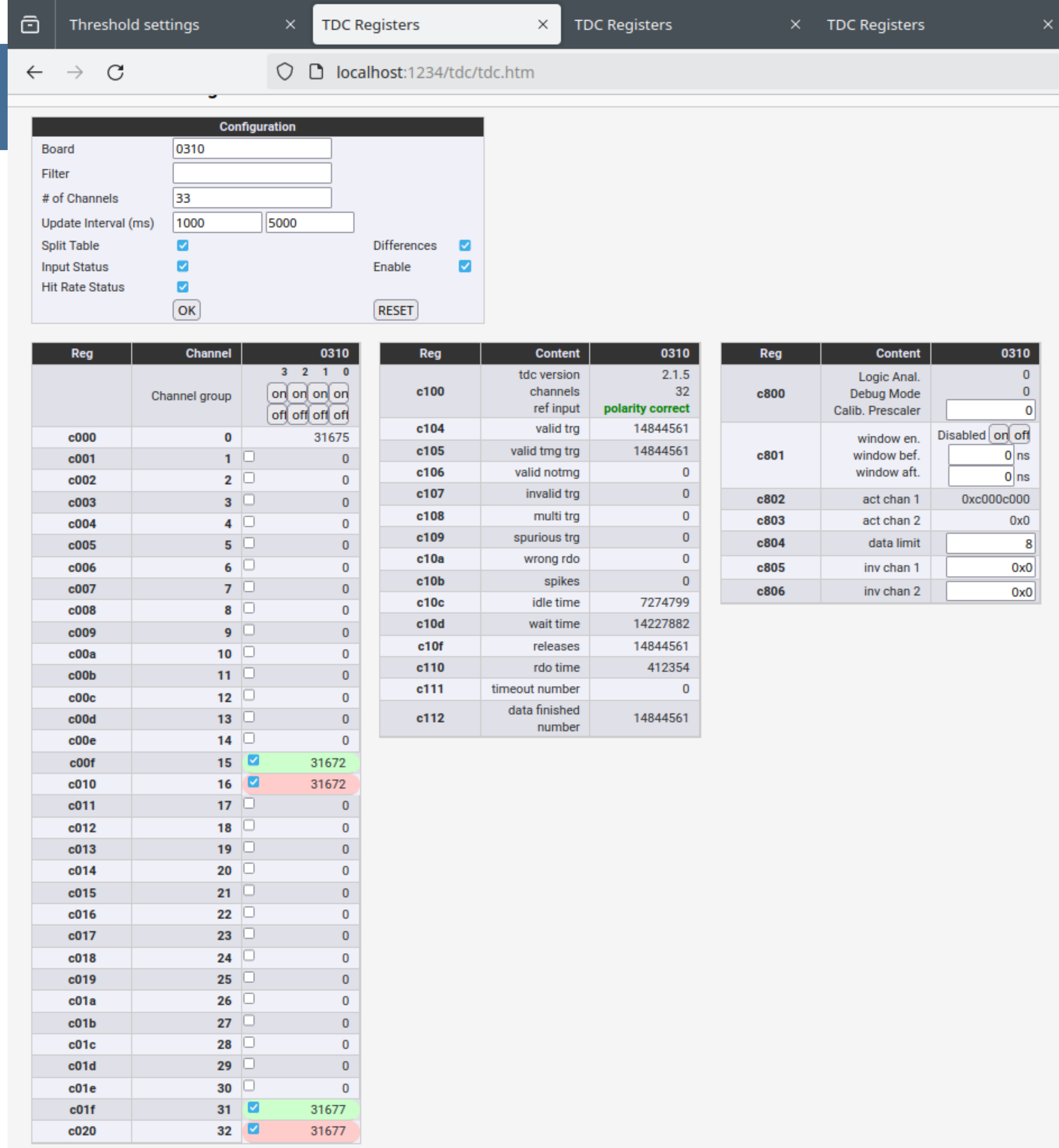


*

* Jinyuan Wu, Z. Shi и I. Wang   CERN2000

WEB GUI

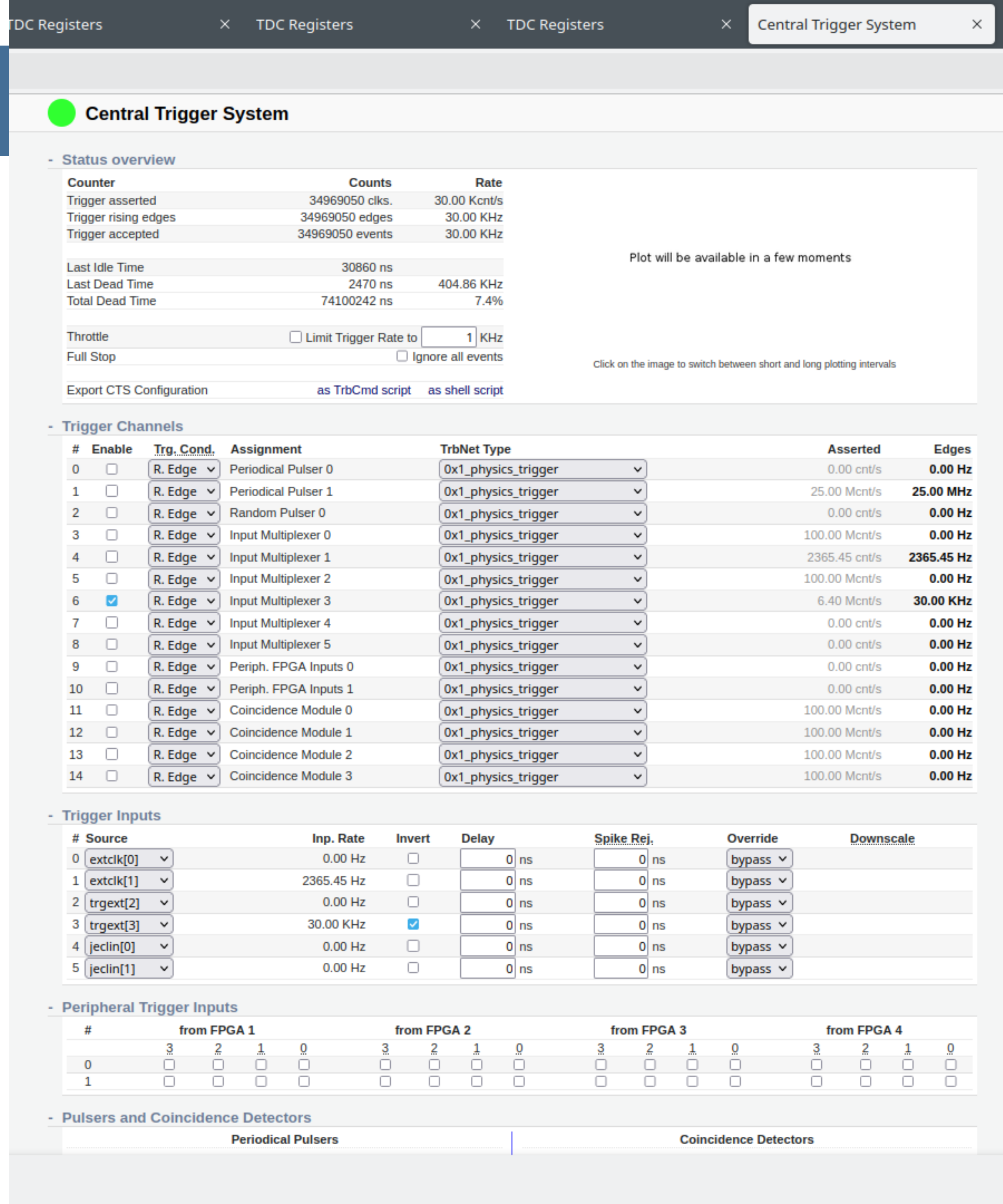

Threshold settings
TDC Regis
localho
Threshold Settings
Configuration
Board 0311
DAC-Chain 1
Channel 1
Board Type LTC242x DAC
Update Interval (ms) 500
Reference (mV) 3300
DiRich2 Flash: Store Load
Last read
Last set 12:46:47 PM
OK
Coarse (0-65535)
Fine (0-255)
Shortcuts
c/v: Increase/Decrease channel number
d/f: Increase/Decrease chain number
Up/Down: Increase/Decrease by 1
Shift + Up/Down: Increase/Decrease by 16
PageUp/PageDown: Increase/Decrease by 256
Shift + PageUp/PageDown: Increase/Decrease by 2048
a/A: Increase / Decrease board address
B/U/R: Select input field
r: Refresh values, read-back values from Padiwa


Threshold settings
TDC Registers
TDC Registers
TDC Registers
localhost:1234/tdc/tdc.htm
Configuration
Board 0310
Filter
# of Channels 33
Update Interval (ms) 1000 5000
Split Table
Differences
Input Status
Enable
Hit Rate Status
OK
RESET
Reg Channel 0310
Channel group 3 2 1 0 on on on on off off off off
c000 0 31675
c001 1 0
c002 2 0
c003 3 0
c004 4 0
c005 5 0
c006 6 0
c007 7 0
c008 8 0
c009 9 0
c00a 10 0
c00b 11 0
c00c 12 0
c00d 13 0
c00e 14 0
c00f 15 31672
c010 16 31672
c011 17 0
c012 18 0
c013 19 0
c014 20 0
c015 21 0
c016 22 0
c017 23 0
c018 24 0
c019 25 0
c01a 26 0
c01b 27 0
c01c 28 0
c01d 29 0
c01e 30 0
c01f 31 31677
c020 32 31677
Reg Content 0310
c100 tdc version 2.1.5
channels 32
ref input polarity correct
c104 valid trg 14844561
c105 valid tmg trg 14844561
c106 valid notmg 0
c107 invalid trg 0
c108 multi trg 0
c109 spurious trg 0
c10a wrong rdo 0
c10b spikes 0
c10c idle time 7274799
c10d wait time 14227882
c10f releases 14844561
c110 rdo time 412354
c111 timeout number 0
c112 data finished number 14844561
Reg Content 0310
c800 Logic Anal. 0
Debug Mode 0
Calib. Prescaler 0
c801 window en. Disabled on off
window bef. 0 ns
window aft. 0 ns
c802 act chan 1 0xc000c000
c803 act chan 2 0x0
c804 data limit 8
c805 inv chan 1 0x0
c806 inv chan 2 0x0

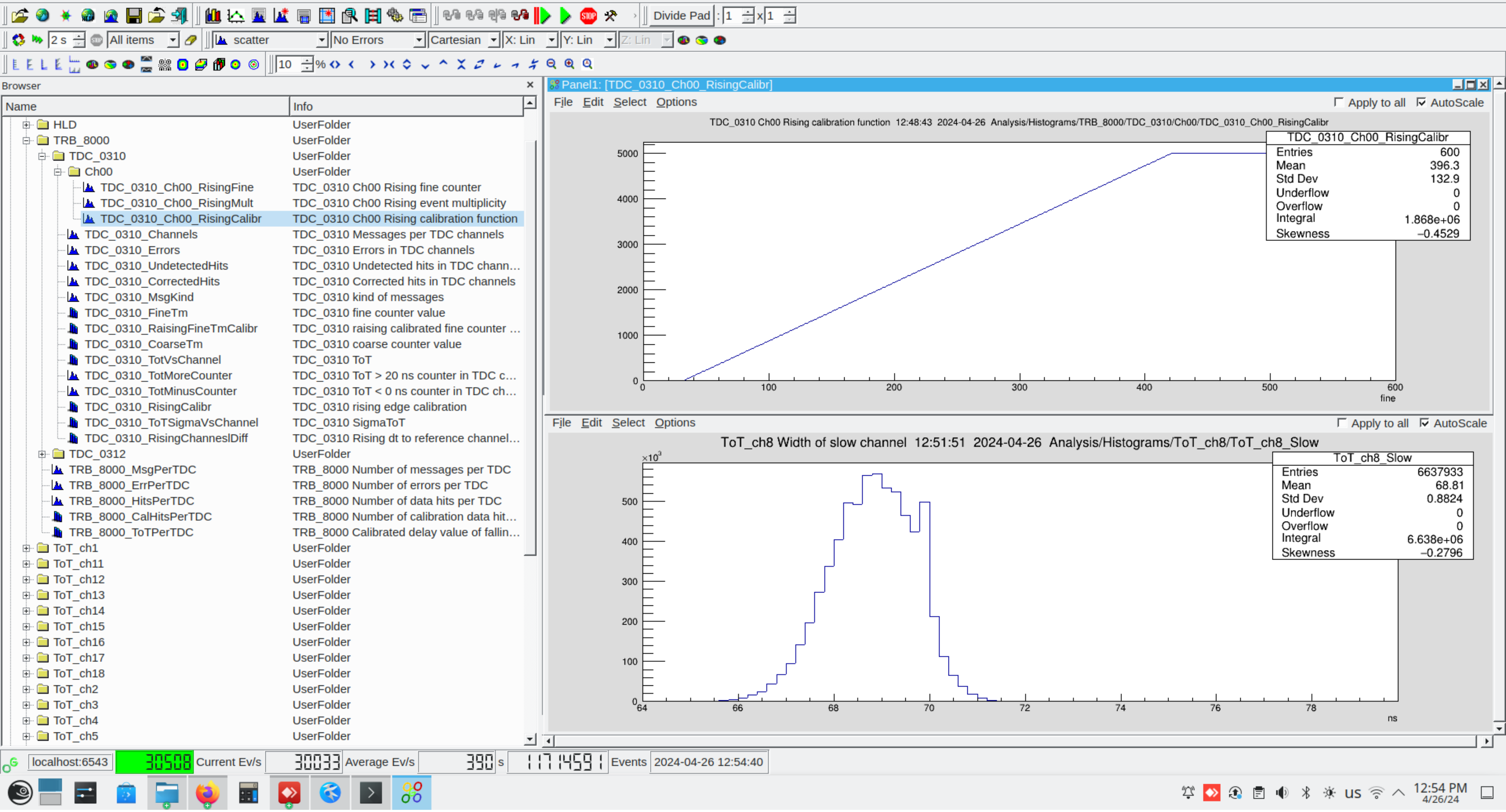
WEB CTS

ZOO on SUSE Tumbleweed:

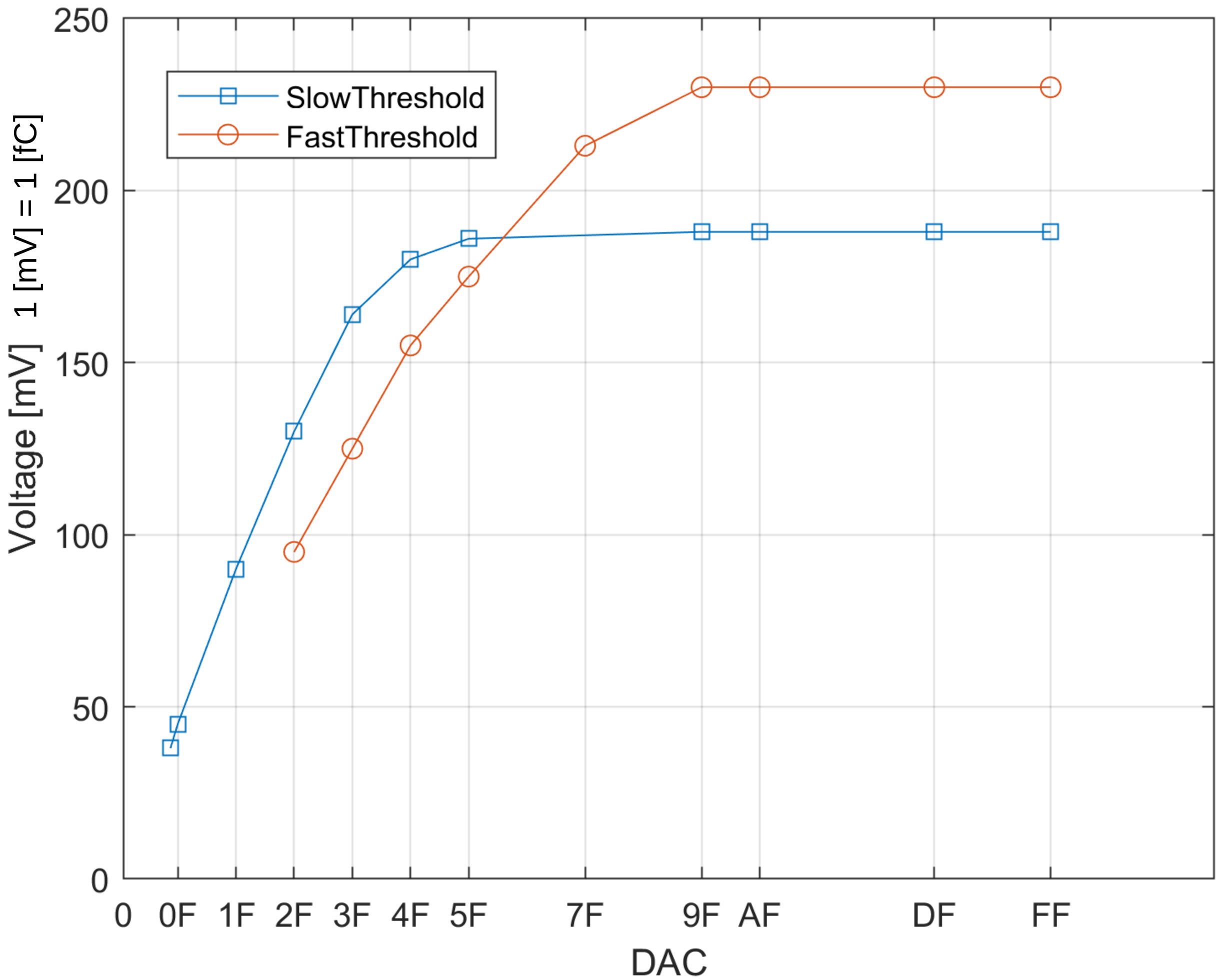
- **VHDL** is a hardware description language that can model the behavior and structure of digital system at multiple levels of abstraction.
- **Perl** Practical Extraction and Report Language.
- **XML** ExtensibleMarkupLanguage for storing, transmitting, and reconstructing arbitrary data.
- **C++** (ROOT etc.)

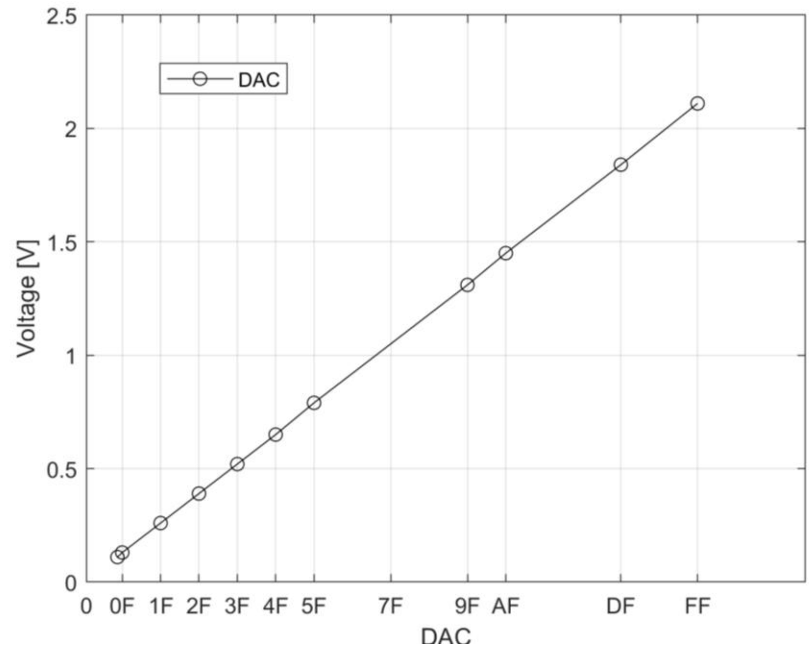


GO4 for data visualization and analysis



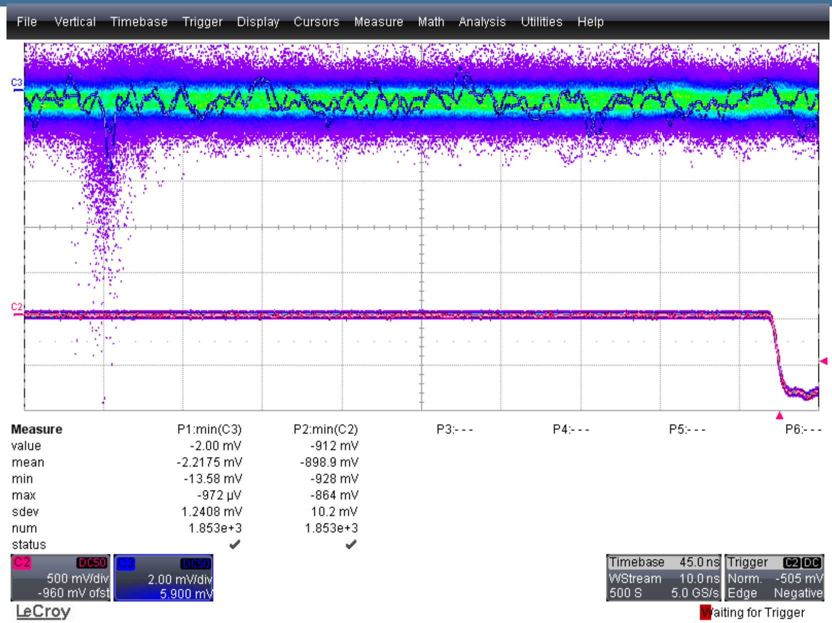
Threshold for Fast and Slow FEE output

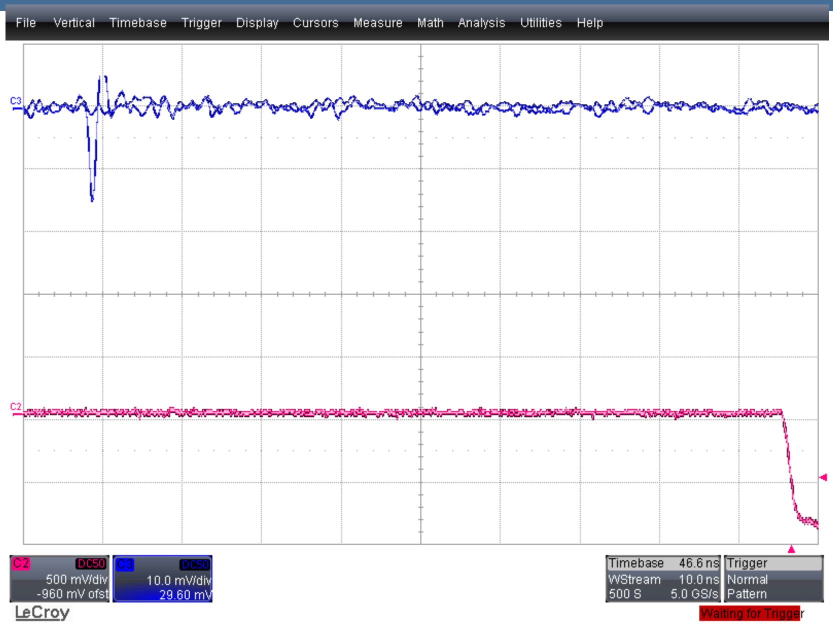


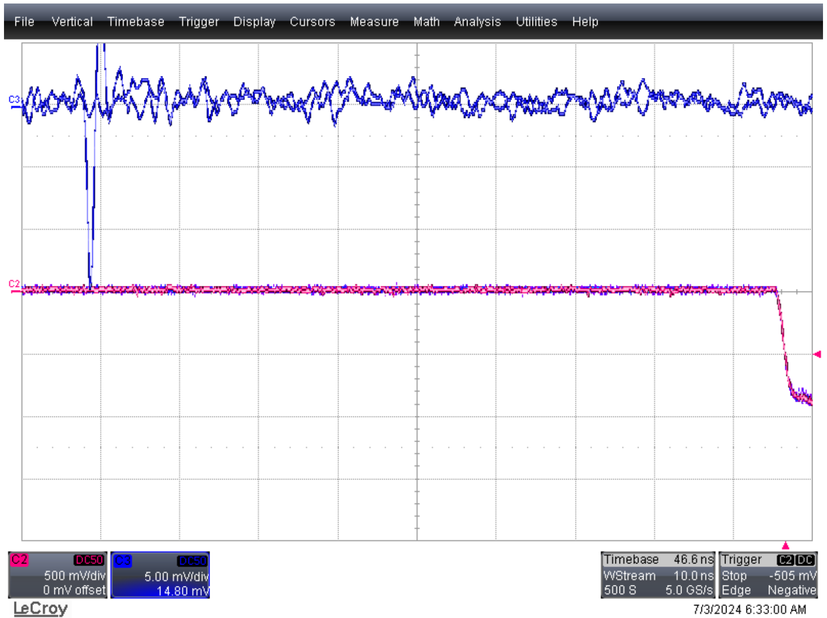


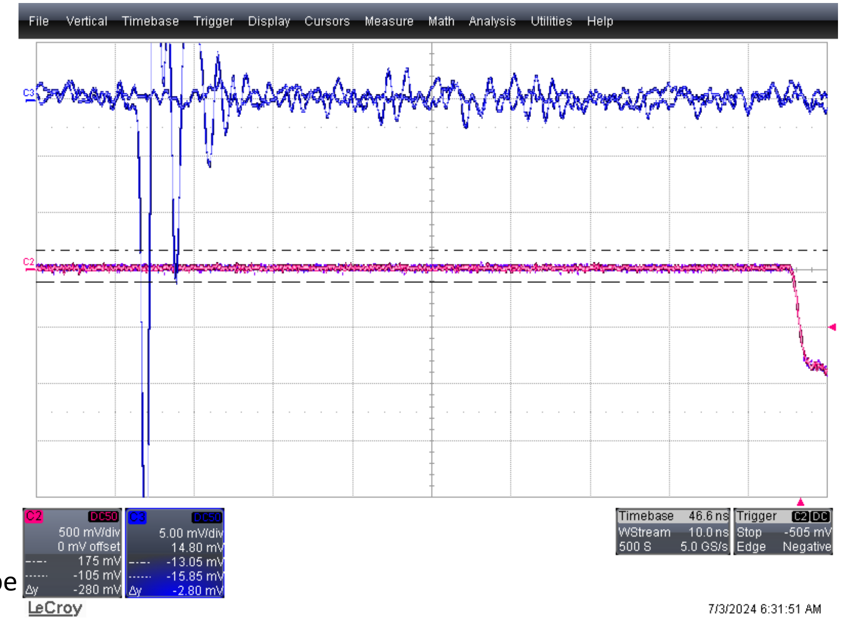
Counts on Fast and after for Slow channels becomes equal to triggers number (Threshold)

Signals from MRPC

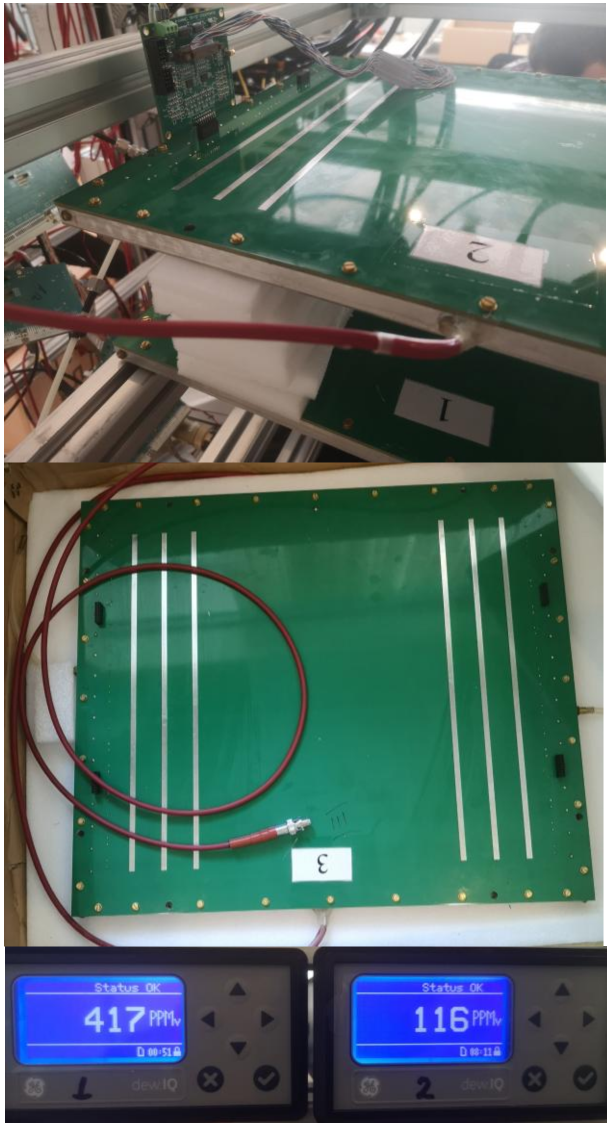


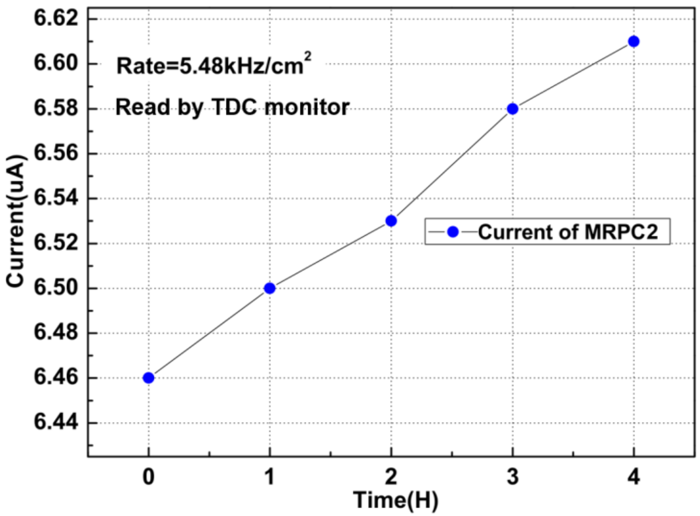


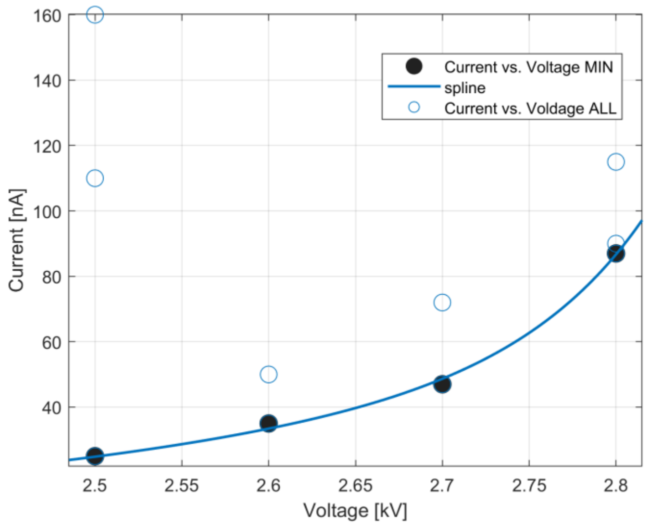


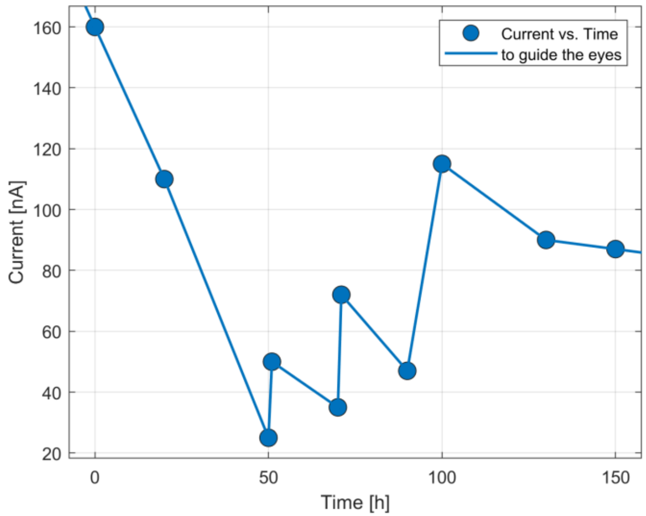


IV of MRPC#2 from Protvino vs. Sealed (Yi Wang)

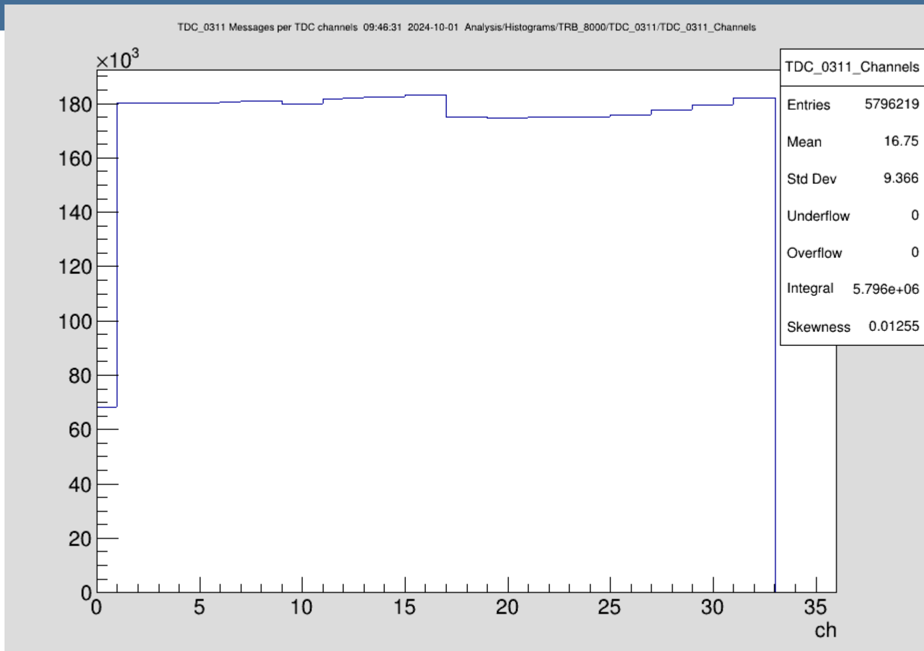




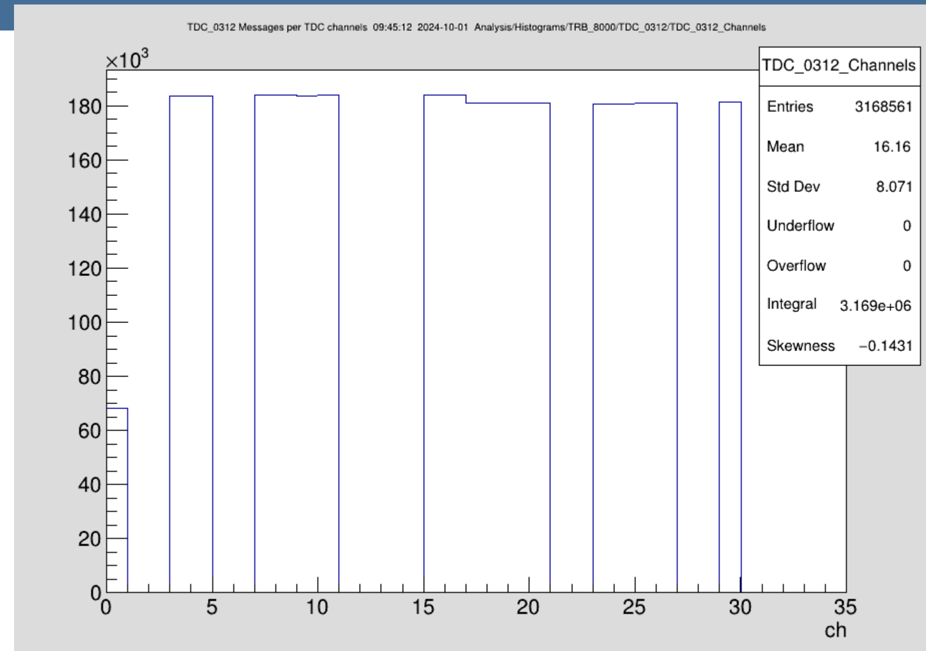


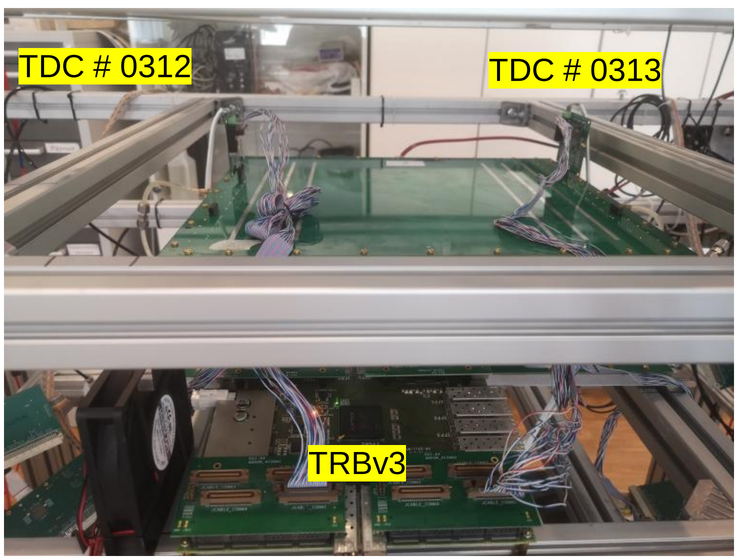


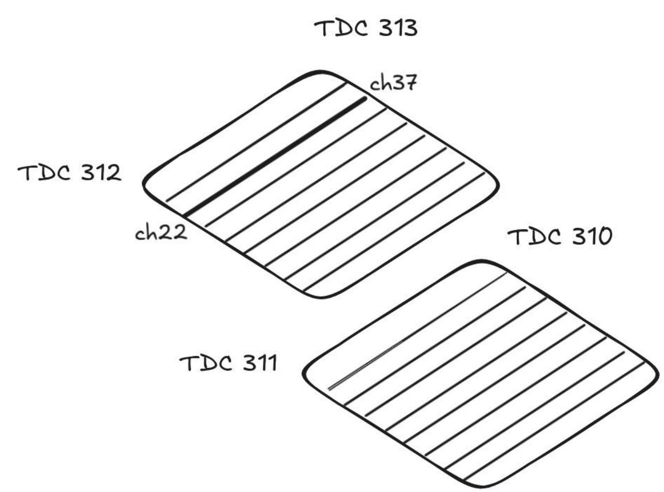
TDC#0311



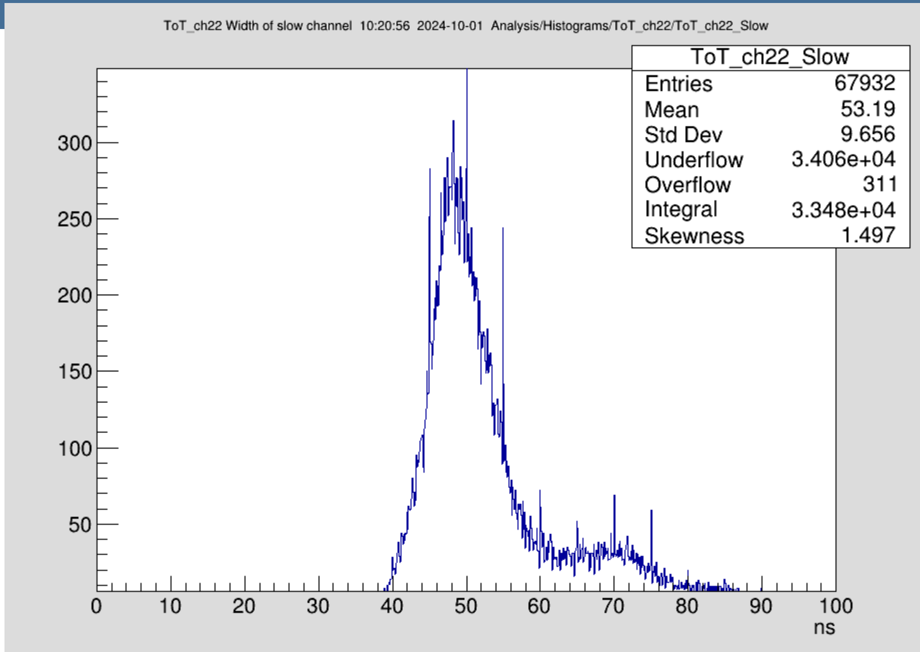
TDC#0312

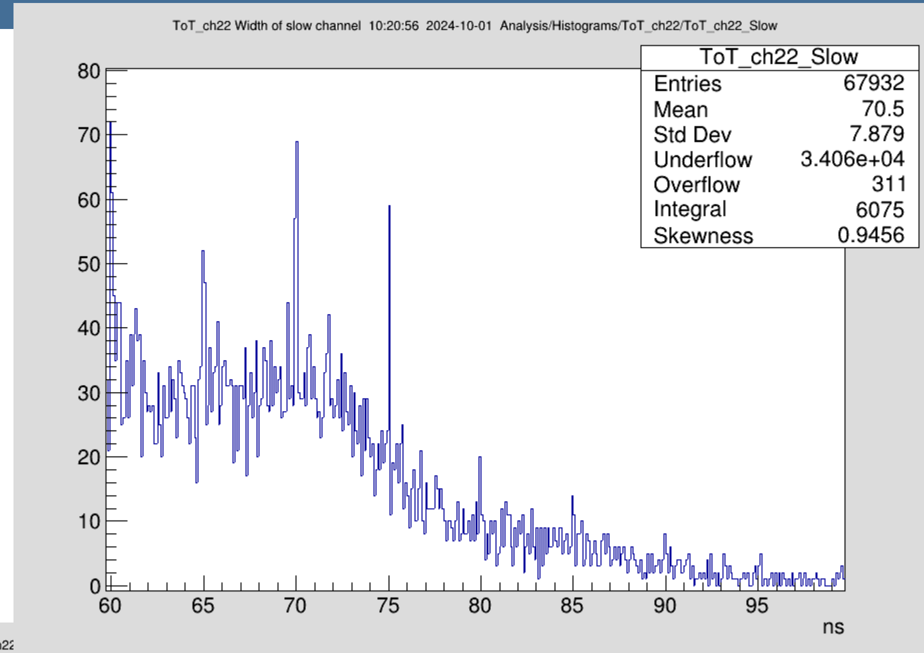


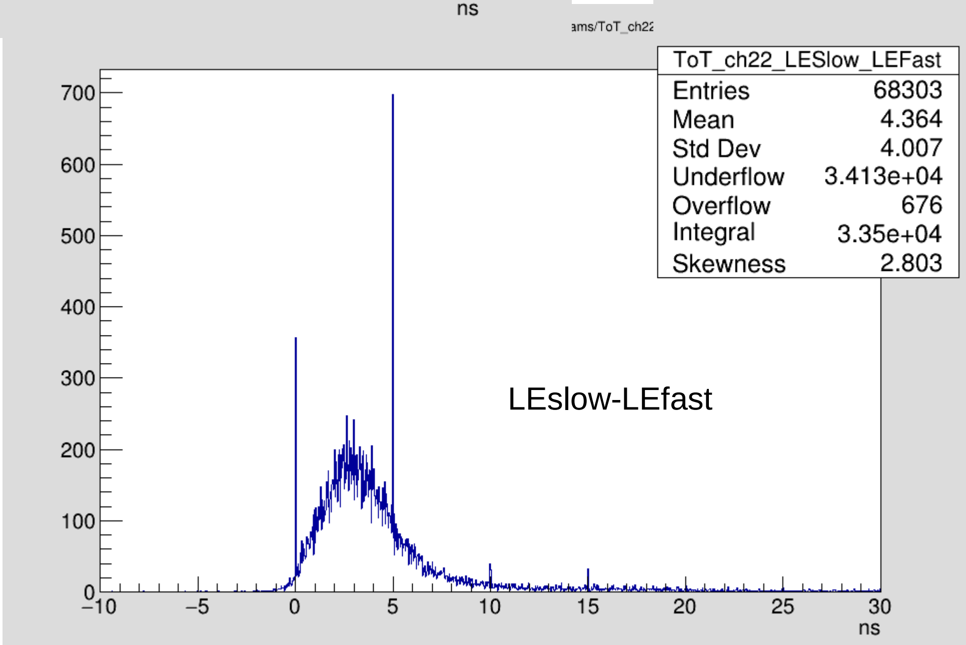




CH#22 slow from TDC#0312







Possible FEE and Digitization

https://www.caen.it/subfamilies/fers-5200/

- Sensor (SiPM)
- ASIC (WEEROC family, citiroc-1A)
- FPGA
- Data Transmitting

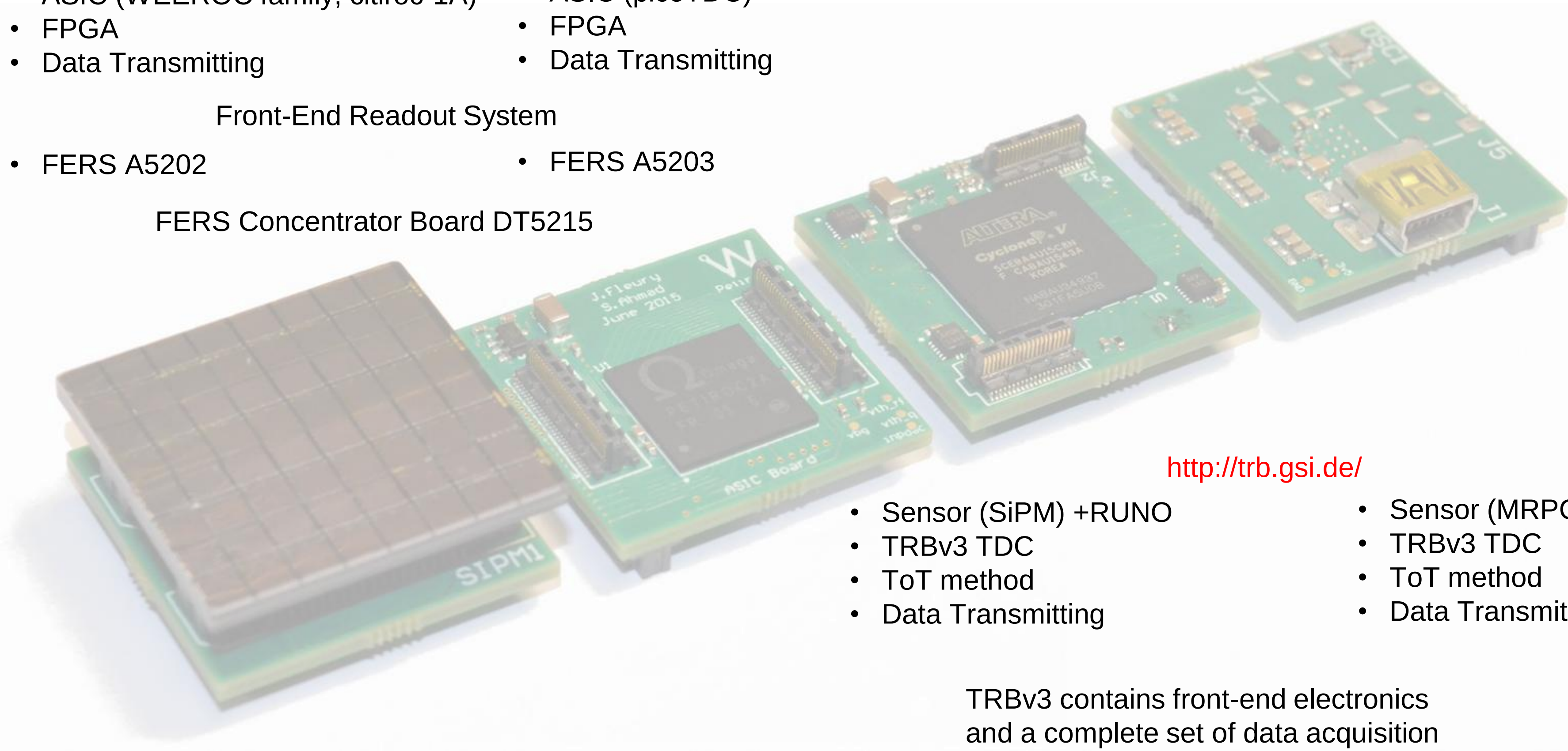
- Sensor (MRPC) + NINO
- ASIC (picoTDC)
- FPGA
- Data Transmitting

Front-End Readout System

- FERS A5202

- FERS A5203

FERS Concentrator Board DT5215



http://trb.gsi.de/

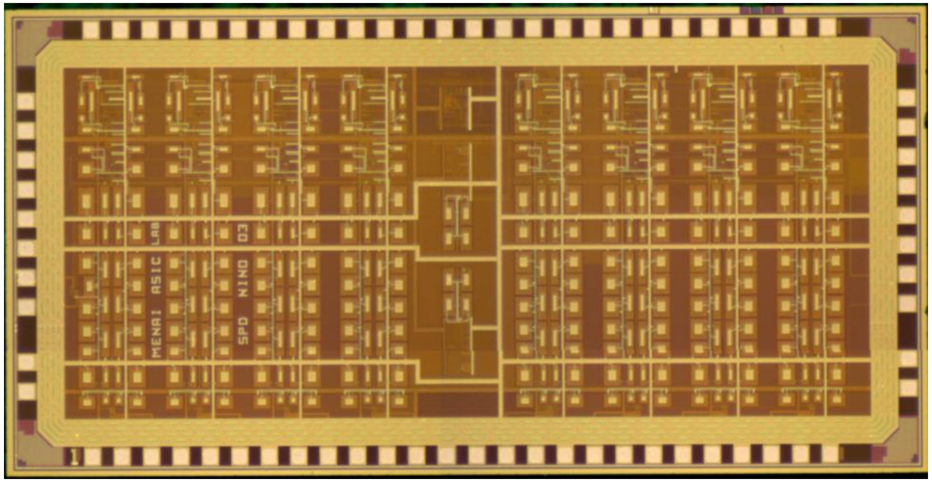
- Sensor (SiPM) +RUNO
- TRBv3 TDC
- ToT method
- Data Transmitting

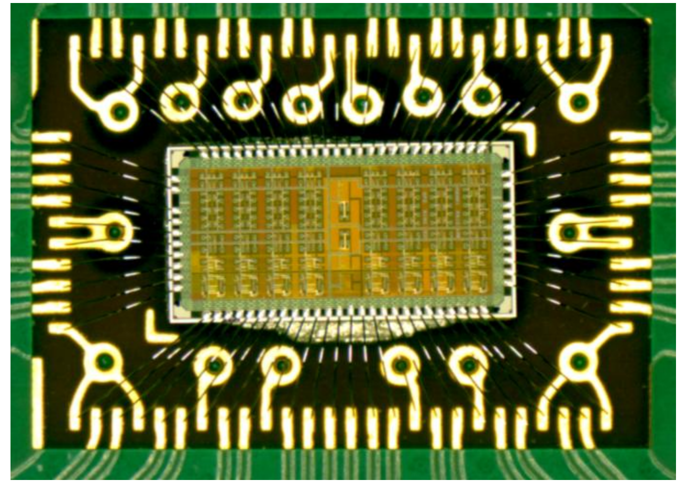
- Sensor (MRPC) + RUNO
- TRBv3 TDC
- ToT method
- Data Transmitting

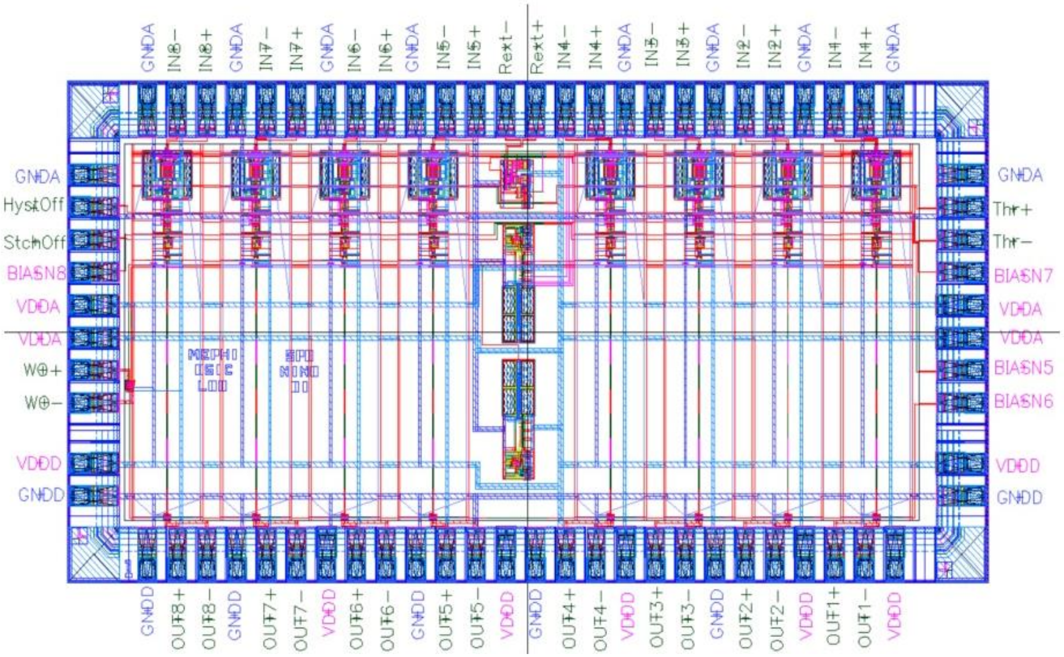
TRBv3 contains front-end electronics and a complete set of data acquisition and control software.

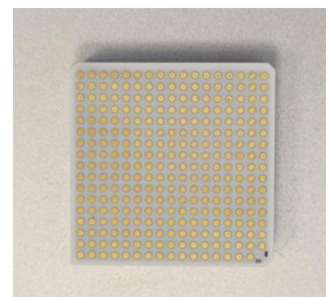
FERS FERS+NINO vs. TRBv3 FPGA-TDC+RUNO

RUNO

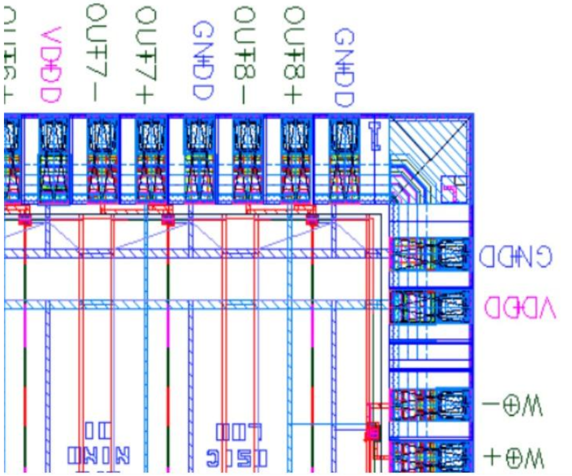


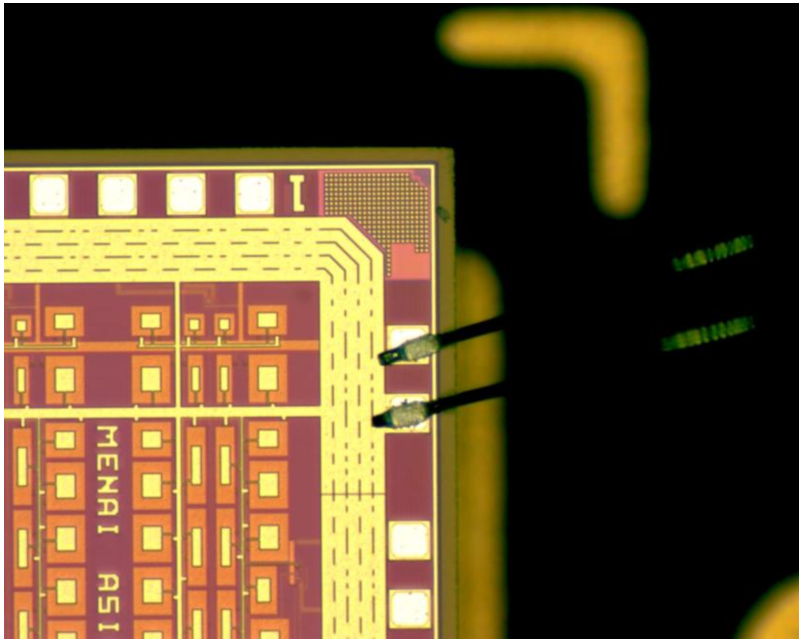


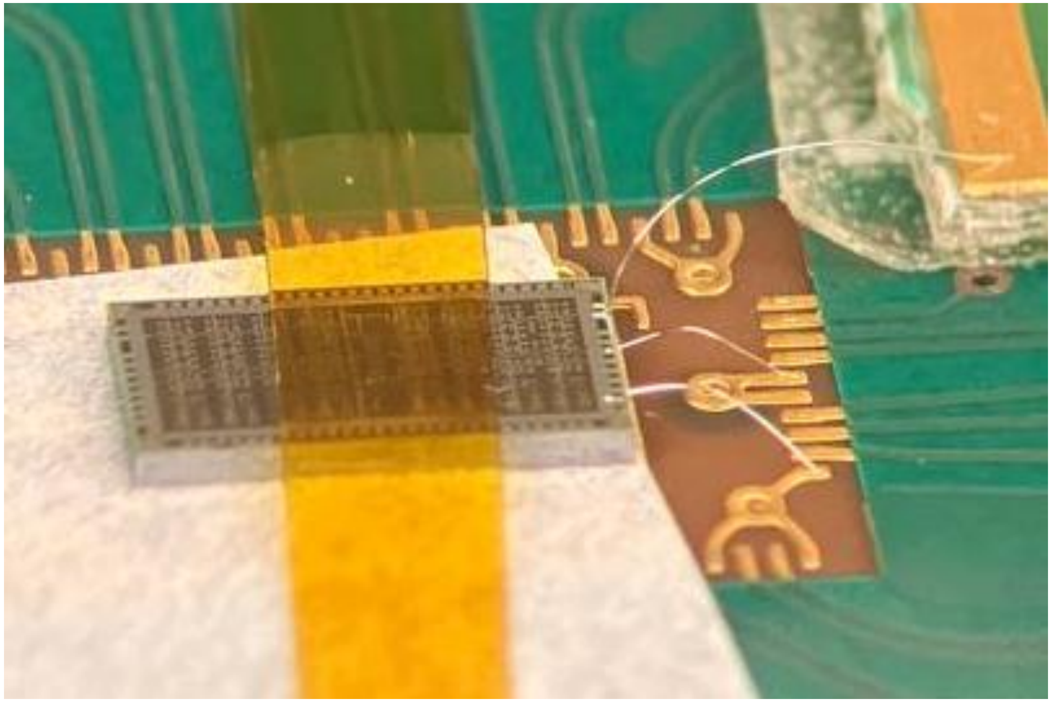

GNDA
IN8−
IN8+
GNDA
IN7−
IN7+
GNDA
IN6−
IN6+
GNDA
IN5−
IN5+
Rext−
Rext+
IN4−
IN4+
GNDA
IN3−
IN3+
GNDA
IN2−
IN2+
GNDA
IN1−
IN1+
GNDA
GNDA
HystOff
StchOff
BIASN8
VDDA
VDDA
WO+
WO−
VDDD
GNDD
GNDA
Thr+
Thr−
BIASN7
VDDA
VDDA
BIASN5
BIASN6
VDDD
GNDD
GNDD
OUT8+
OUT8−
GNDD
OUT7+
OUT7−
VDDD
OUT6+
OUT6−
GNDD
OUT5+
OUT5−
VDDD
GNDD
OUT4+
OUT4−
VDDD
OUT3+
OUT3−
GNDD
OUT2+
OUT2−
VDDD
OUT1+
OUT1−
VDDD



RUNO







- RUNO has very low impedance on power line
- VddA and VddD are short-circuited
- GNDD and GNDA as well
- We need some time to relax and enjoy the life

F. Garzetti et al.: TDC IP-Core for FPGA at State of the Art

TABLE 1. Most significant implementations of TDL-TDCs in Xilinx FPGA devices, sorted by resolution (LSB).

Reference	FPGA device	Tech. Node	LSB	σ_{CH}	FSR	DNL	INL	Ch. Rate
[23]	Virtex–6	40–nm	10.0 ps	19.6 ps r.m.s.	N.A.	15.0 ps	22.5 ps	N.A.
[24]	Virtex–5	65–nm	16.3 ps	N.A.	N.A.	48.9 ps	81.5 ps	N.A.
[25]	Virtex–6	40–nm	1.70 ps	4.2 ps r.m.s.	N.A.	1.36 ps	1.70 ps	N.A.
[26]	Kintex–7	28–nm	17.6 ps	12.7 ps r.m.s.	N.A.	17.6 ps	15.3 ps	N.A.
[27]	Virtex–6	40–nm	10.0 ps	10.0 ps r.m.s.	N.A.	19.1 ps	22.0 ps	N.A.
[28]	Kintex–7	28–nm	10.6 ps	8.13 ps r.m.s.	N.A.	10.6 ps	45.6 ps	N.A.
[28]	Virtex–6	40–nm	10.1 ps	9.82 ps r.m.s.	N.A.	11.9 ps	33.3 ps	N.A.
[28]	Spartan–6	40–nm	16.7 ps	12.8 ps r.m.s.	N.A.	20.4 ps	42.4 ps	N.A.
[29]	UltraScale	20–nm	2.25 ps	3.90 ps r.ms.	N.A.	N.A.	N.A.	N.A.
[30]	Virtex–5	65–nm	7.40 ps	6.80 ps r.m.s.	N.A.	5.48 ps	11.6 ps	N.A.
[31]	Virtex–7	28–nm	1.15 ps	3.50 ps r.m.s.	N.A.	4.03 ps	6.79 ps	N.A.
[12]	Virtex–7	28–nm	10.5 ps	14.6 ps r.m.s.	N.A.	0.84 ps	1.16 ps	N.A.
[12]	UltraScale	20–nm	5.02 ps	7.80 ps r.m.s.	N.A.	0.60 ps	2.31 ps	N.A.
[32]	Virtex–5	65–nm	18.0 ps	25.0 ps r.m.s.	10.7 s	N.A.	N.A.	5 MHz
[33]	Artix–7	28–nm	10.0 ps	15 ps r.m.s.	10.7 s	N.A.	N.A.	10 MHz
[34]	Artix–7	28–nm	250 fs	12 ps r.m.s.	10.3 s	N.A.	4.2 ps	20 MHz
[35]	Artix–7	28–nm	250 fs	12 ps r.m.s.	10.3 s	33 fs	4.6 ps	45 MHz
[36], [37]	Zynq–7000	28–nm	2 ps	12 ps r.m.s.	10.7 s	N.A.	N.A.	45 MHz
[38]	UltraScale	20–nm	305 fs	8.5 ps r.m.s.	10.2 μs	N.A.	N.A.	50 MHz
[39]	Spartan–6	40–nm	7.70 ps	8.90 ps r.m.s.	N.A.	22.3 ps	67.8 ps	40 MHz
[40]	Virtex–7	28–nm	6.00 ps	7.00 ps r.m.s.	2.1 s	N.A.	N.A.	125 MHz

TABLE 14. Implementation results and measurements. In particular, Artix-7 column refers to the device selected for testing the IP-Core.

Performance	Artix–7	Virtex–5	Spartan–6	Kintex–7	Zynq–7000	Kintex UltraScale
Resolution	366 fs	18 ps	25 ps	250 fs	2 ps	305 fs
Precision	8.0 ps r.m.s.	25.0 ps r.m.s.	17 ps r.m.s.	8.0 ps r.m.s.	12 ps r.m.s.	8.5 ps r.m.s.
Full Scale Range	10.3 s	10.7 s	640 ns	10.3 s	10.7 s	10.2 μs
DNL	250 fs	N.A.	N.A.	200 fs	1.4 ps	N.A.
INL	2.5 ps	N.A.	N.A.	2.2 ps	5 ps	N.A.
Number of Channels	16	16	4	16	8	24
Channel Rate	150 MHz	5 MHz	N.A.	150 MHz	45 MHz	50 MHz
Dead–Time	5 ns	N.A.	N.A.	5 ns	20 ns	N.A.
Temperature Sensitivity	286 fs/°C	N.A.	N.A.	N.A.	N.A.	N.A.

Master of Science Thesis in Electrical Engineering

A 1.8 ps Time-to-Digital Converter (TDC) Implemented in a 20 nm Field-Programmable Gate Array (FPGA) Using a Ones-Counter Encoding Scheme with Embedded Bin-Width Calibrations and Temperature Correction:

Sven Engström
LiTH-ISY-EX--20/5343--SE

5.1 Resolution

The best resolution of 1.8 ps was achieved using external calibration in combination with the pulsed edge mode. This result is better than previously published FPGA-based TDCs [6]. A small comparison to previous works can be seen in table 5.1.

Ref.-Year	Device	Method	Precision	Resources
[11]-14	Spartan-6	Wave union across multiple TDLs	6 ps	144 SLICEs
[10]-15	Virtex-6	Average multiple TDCs	4.2 ps	–
[9]-17	Virtex-7	Average multiple TDCs	3.5 ps	12758 LUTs
[2]-16	Kintex-7	Average multiple TDCs, wave union	3.1 ps	–
[13]-17	Kintex-7	Multiple TDLs, ones-counter	3.9 ps	2433 LUTs
[5]-16	Kintex UltraScale	Dual sampling	3.9 ps	–
This work	Kintex UltraScale	Internal calibration, dual sampling, ones-counter	2.5 ps	1972 LUTs
		Wave union, dual sampling, ones-counter	1.8 ps	

Table 5.1: *Comparison of recent, high resolution, FPGA-based TDCs*

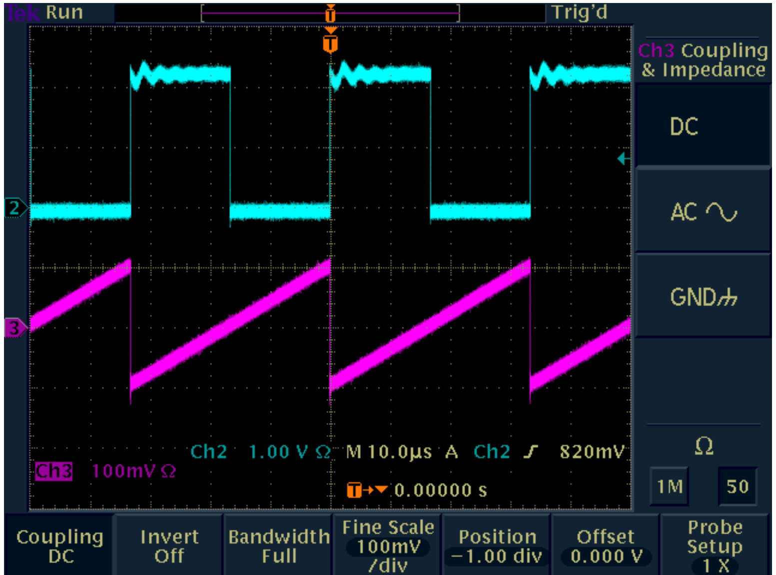
The only way to do great work is to love what you do. © S.J.

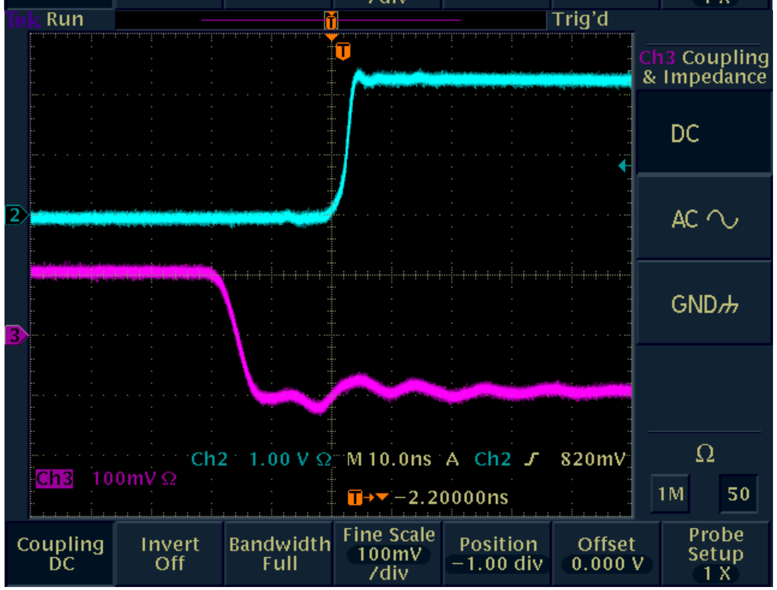
- **Artem Semak, Evgeni Ladygin**
- **Sergei Morozov, Evgeni Usenko**
- **Artem Ivanov**
- **Vladimir Ladygin, Aleksey Tishevsky**
- **Vadim Babkin, Mikhail Buryakov, Oleg Tarasov**
- **Yi Wang at al.**

Thank you for your attention

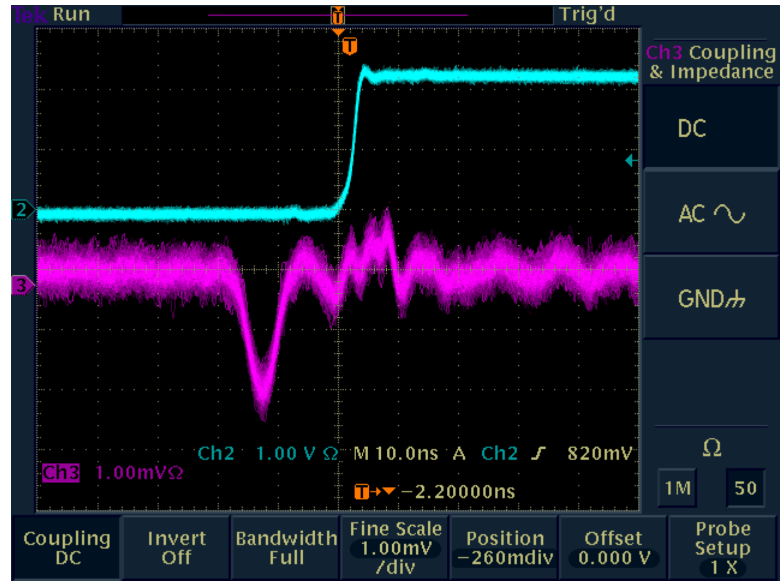
Spare slides

Test signal forming chains and key parameters

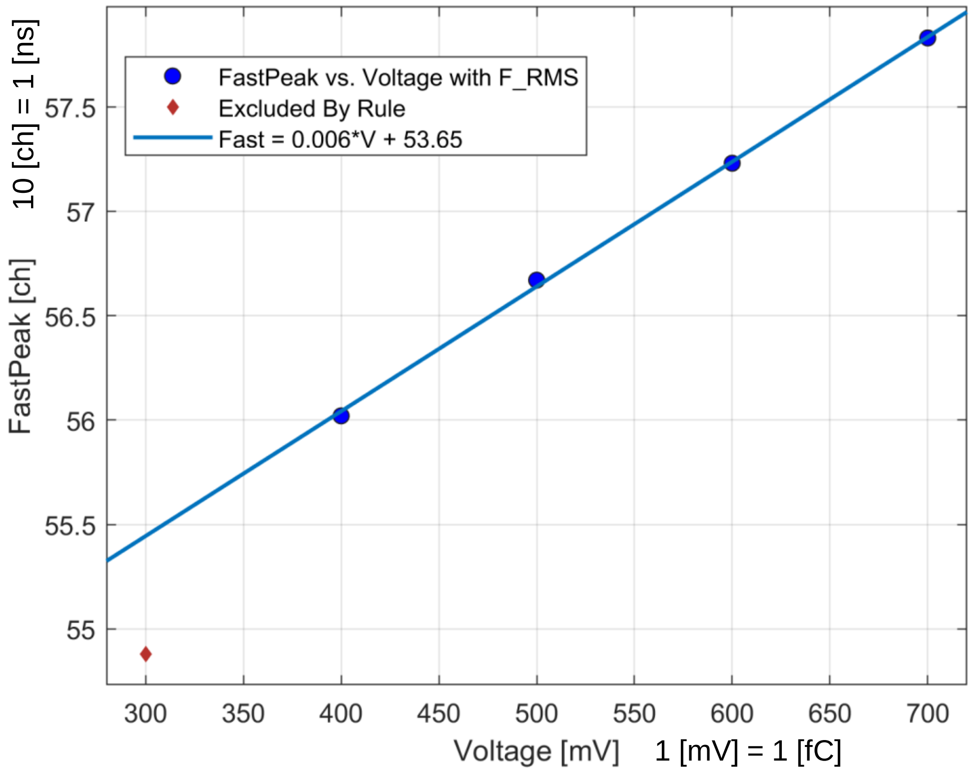




1 pF diff capacitance → 200mV = 200 fC

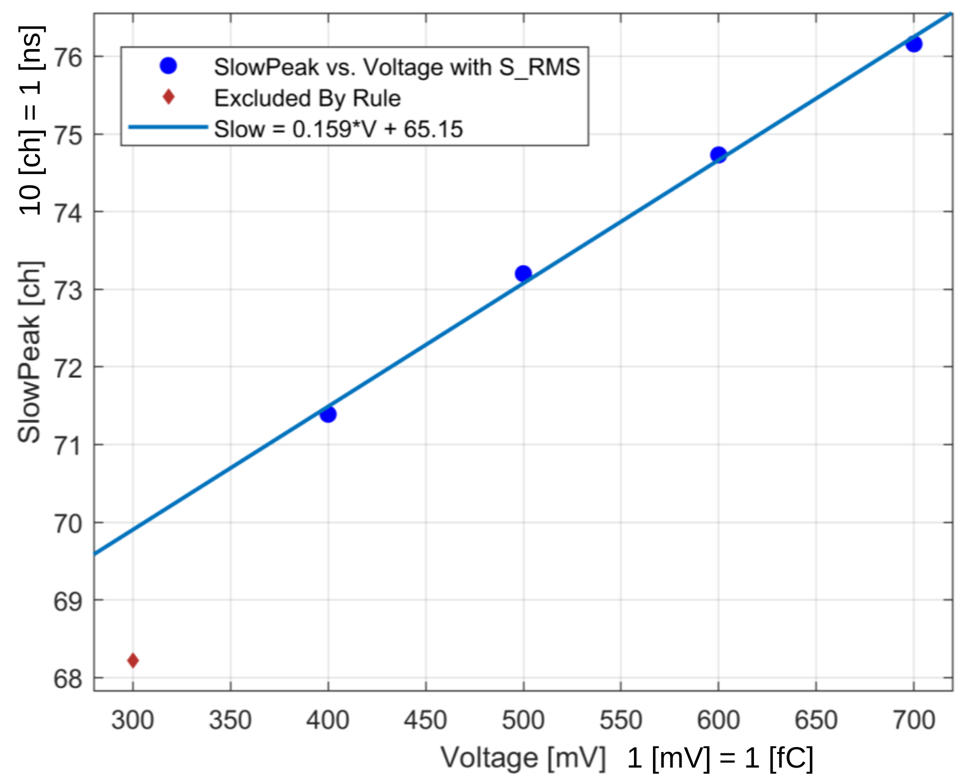


Linear response to test signal for Fast and Slow output

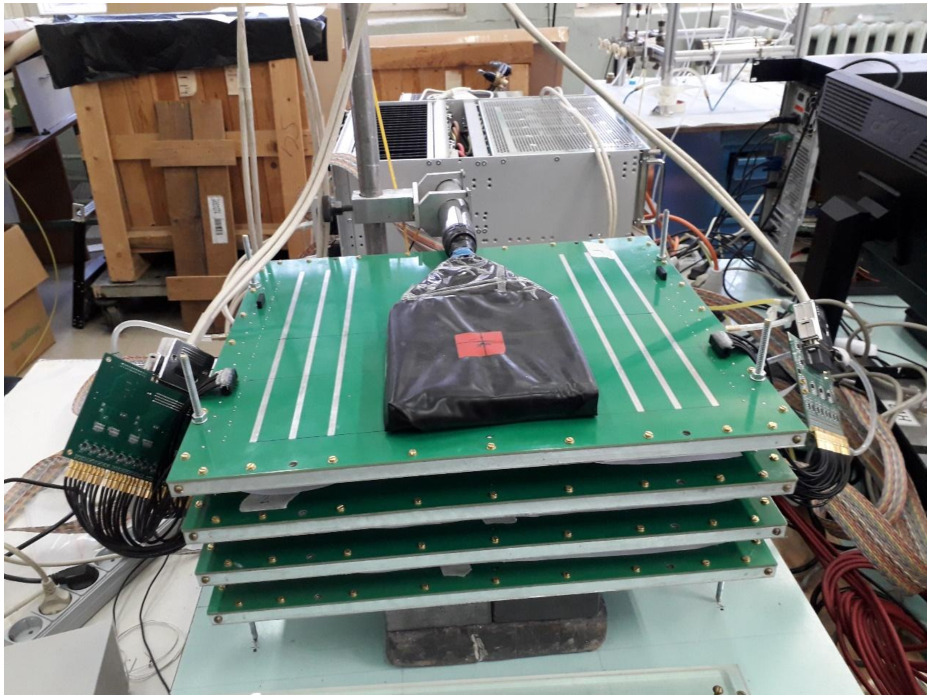


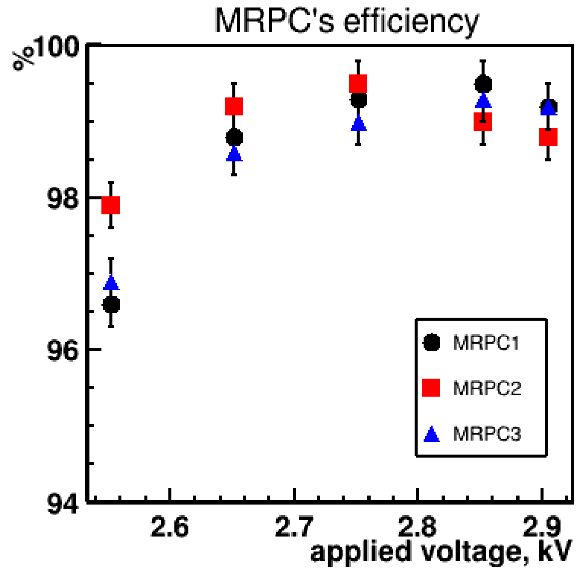
Fast peak width 5.5-6ns STD<100ps

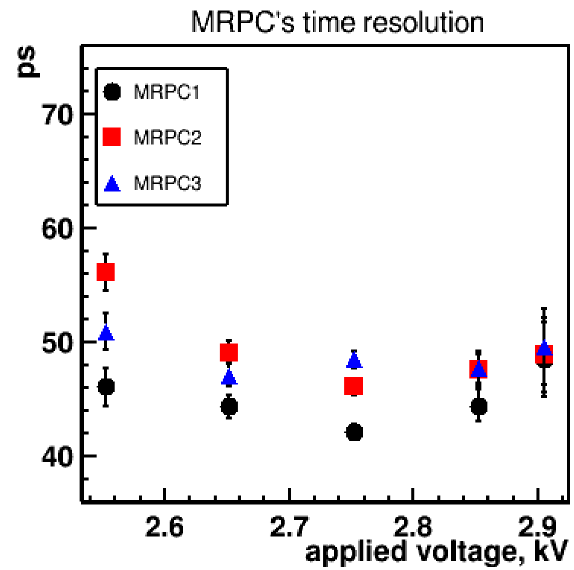
Slow peak width 7-7.6ns STD<90ps



Protvino MRPC prototype for SPD project at NICA



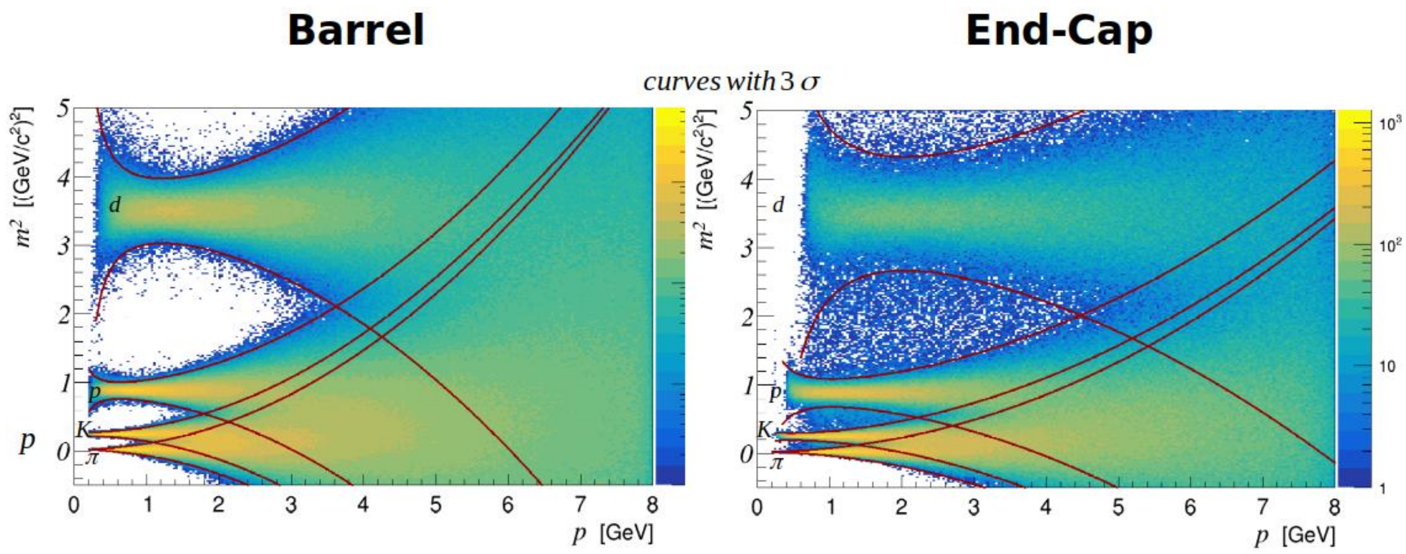


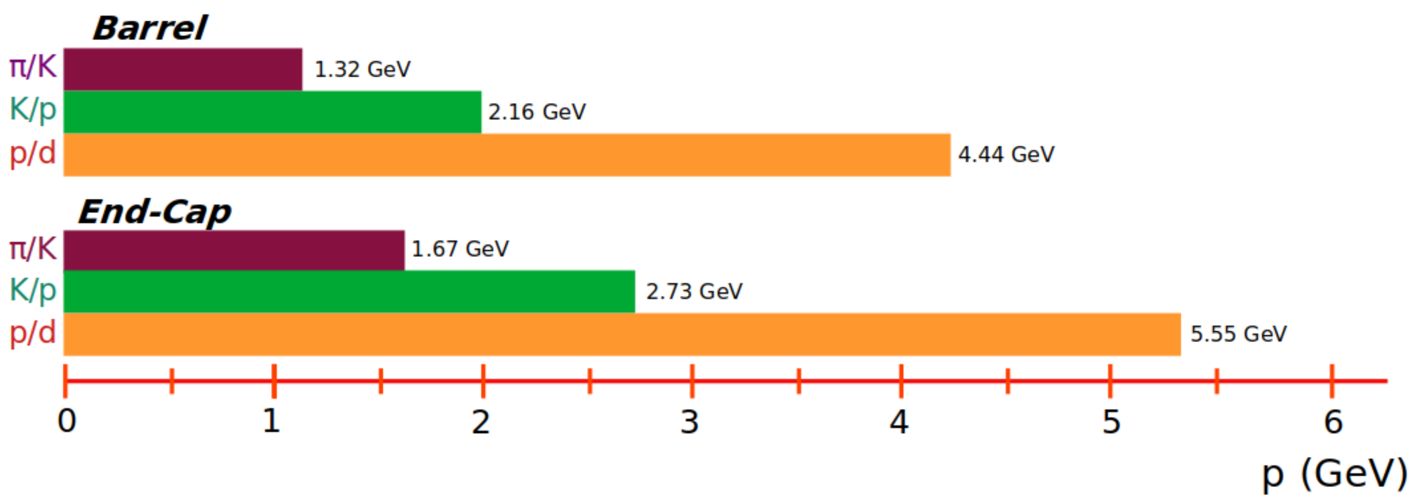


- To start MRPC and check functionality
- To obtain detection efficiency and time resolution on a new DAQ
- Preparation for using 3 MRPC as a servicing system at TEST AREA (Anton Baldin).

Particles ID for m^2 vs. p

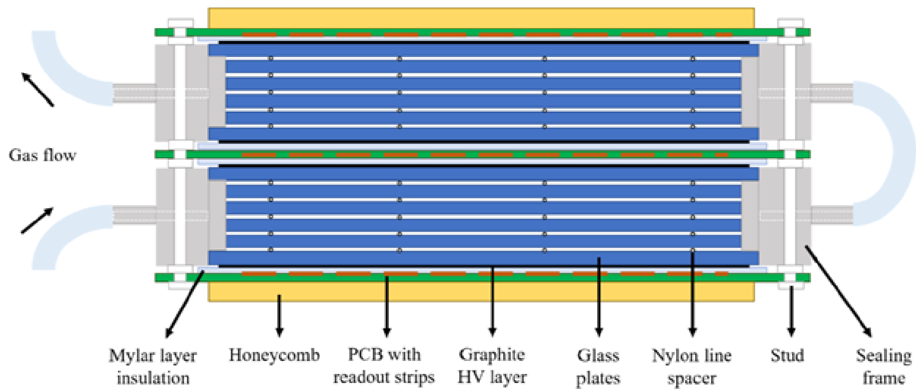
- π/K/p/d discrimination for momenta <2 GeV
- Determination of t0
- Time resolution requirement <60 ps.



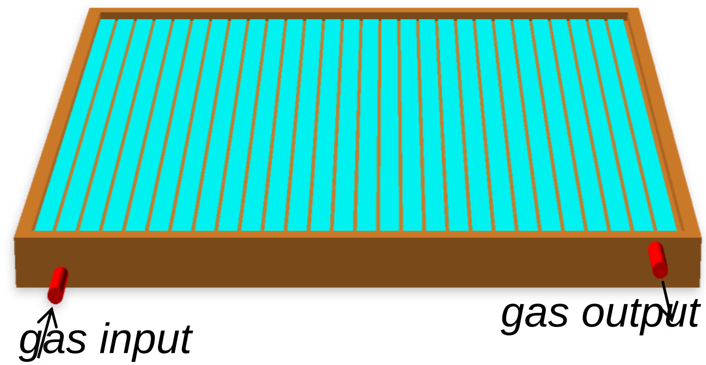


Sealed MRPC for SPD TOF

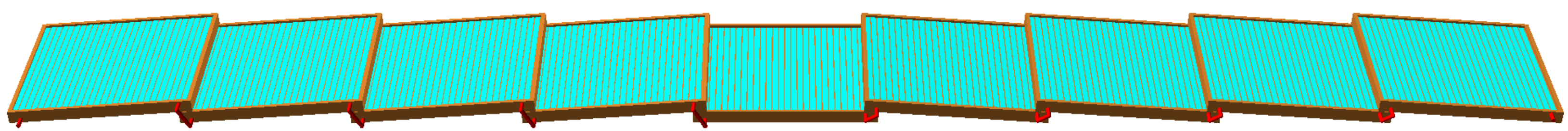
(B.Wang et al, JINST 15 (2020) 08, C08022)



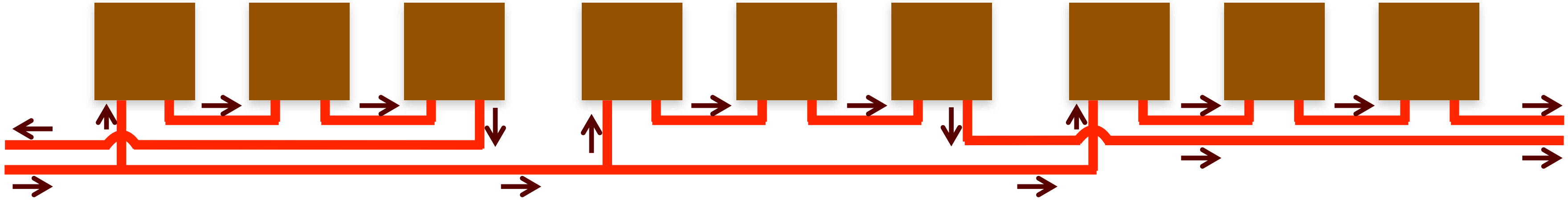
Sealed MRPC proposed for CBM-TOF



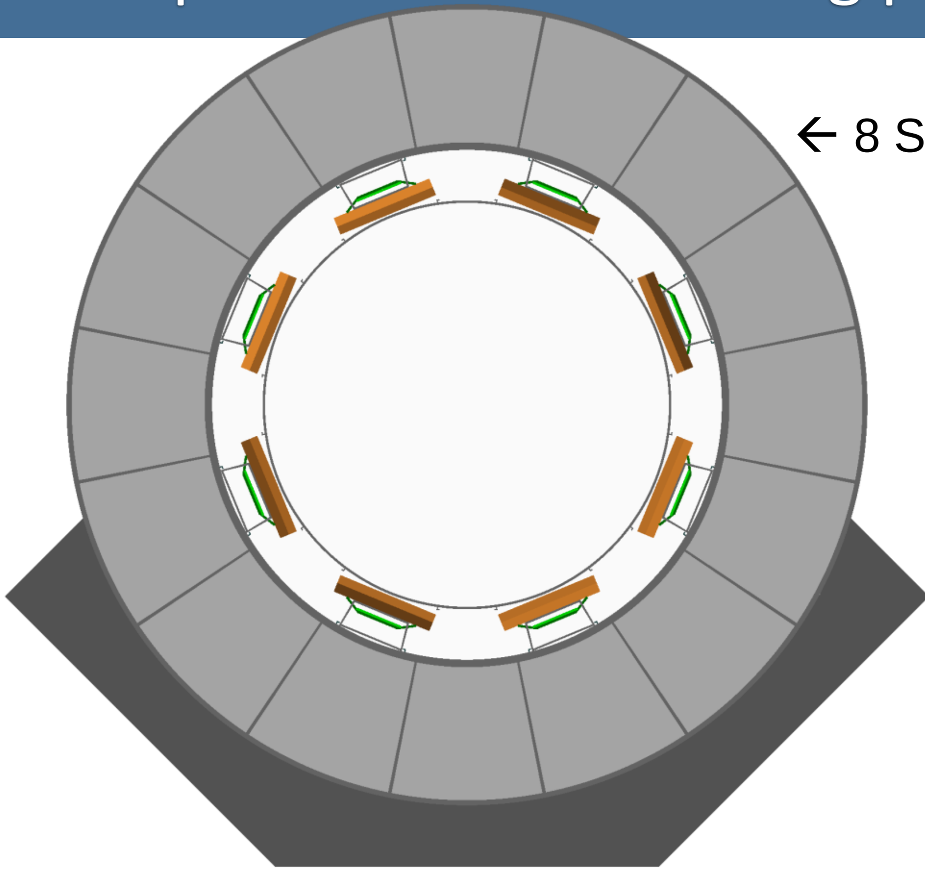
Sealed MRPC proposed for SPD-TOF



Serial gas connection of MRPCs in a single super module

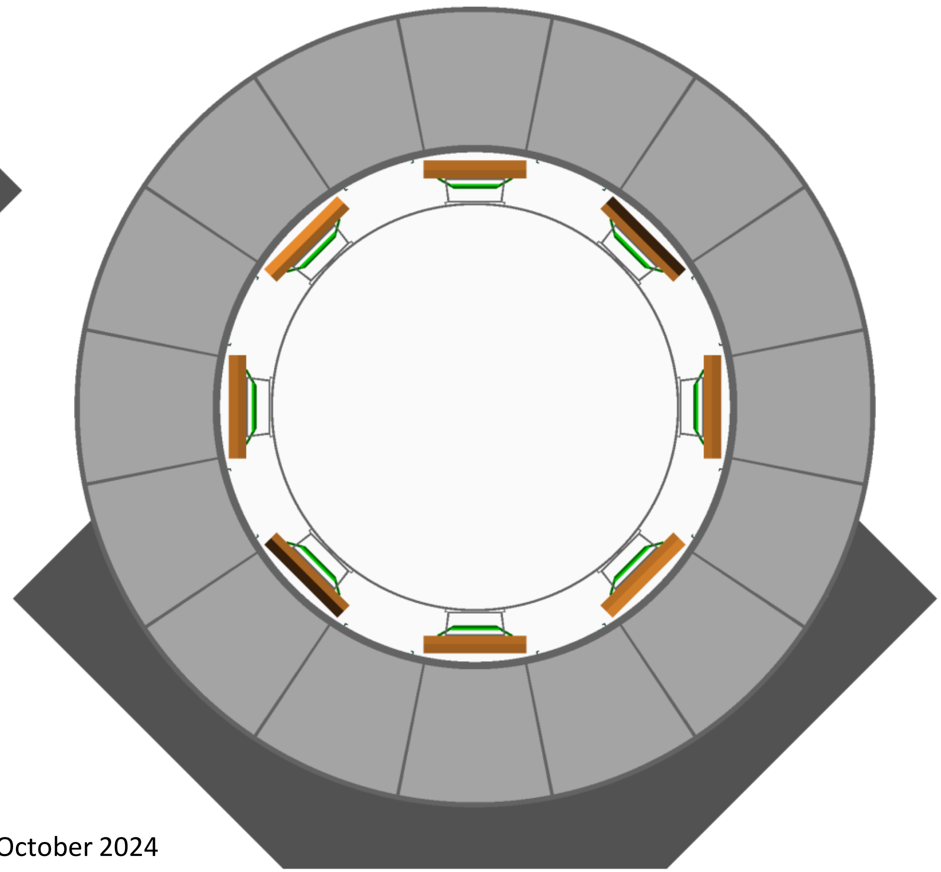


Super modules mounting proposal



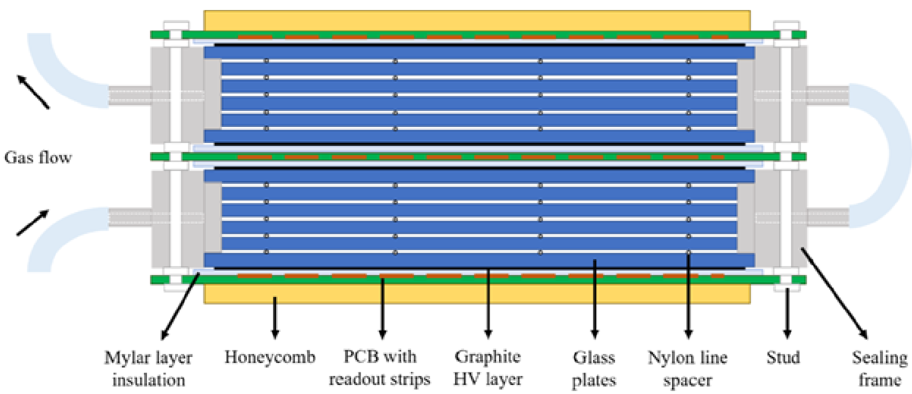
← 8 Super modules mounting on e-Calorimeter

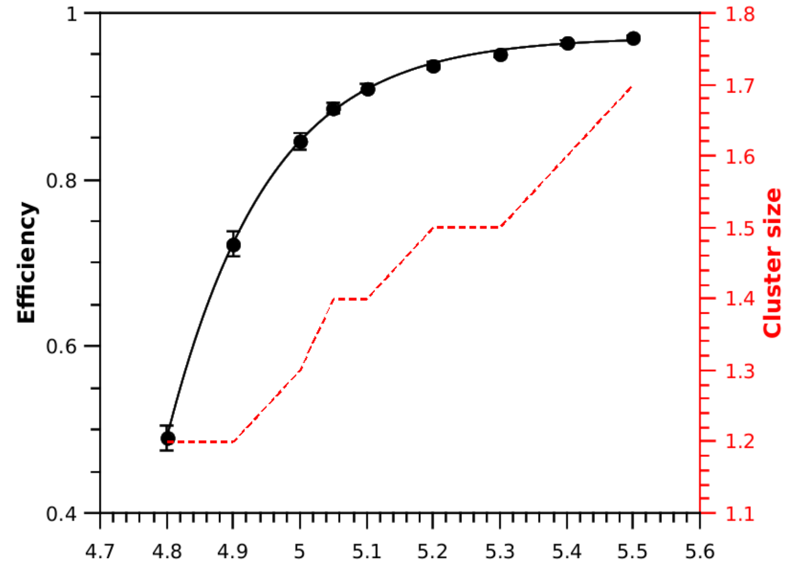
8 Super modules mounting on Straw crate →



Sealed (MRPC) are the base option of today

(B.Wang et al, JINST 15 (2020) 08, C08022)





- The prototype was tested in cosmic rays along with 2 MRPC2 counters in the TRBv3 test stand.
- The plateau efficiency is 97%, with a 1.6 cluster size and a 100 ps flight-time resolution.
- The systematic time resolution of the prototype is about 60 ps. if we reasonably expect the same timing precision between two MRPCs.
- The prototype has the same working point at ±5.4 kV with standard gas flow (Freon/iC_4H_{10} = 90/5/5