Tests of the new FPGA based Front-End Electronics for BBC detector

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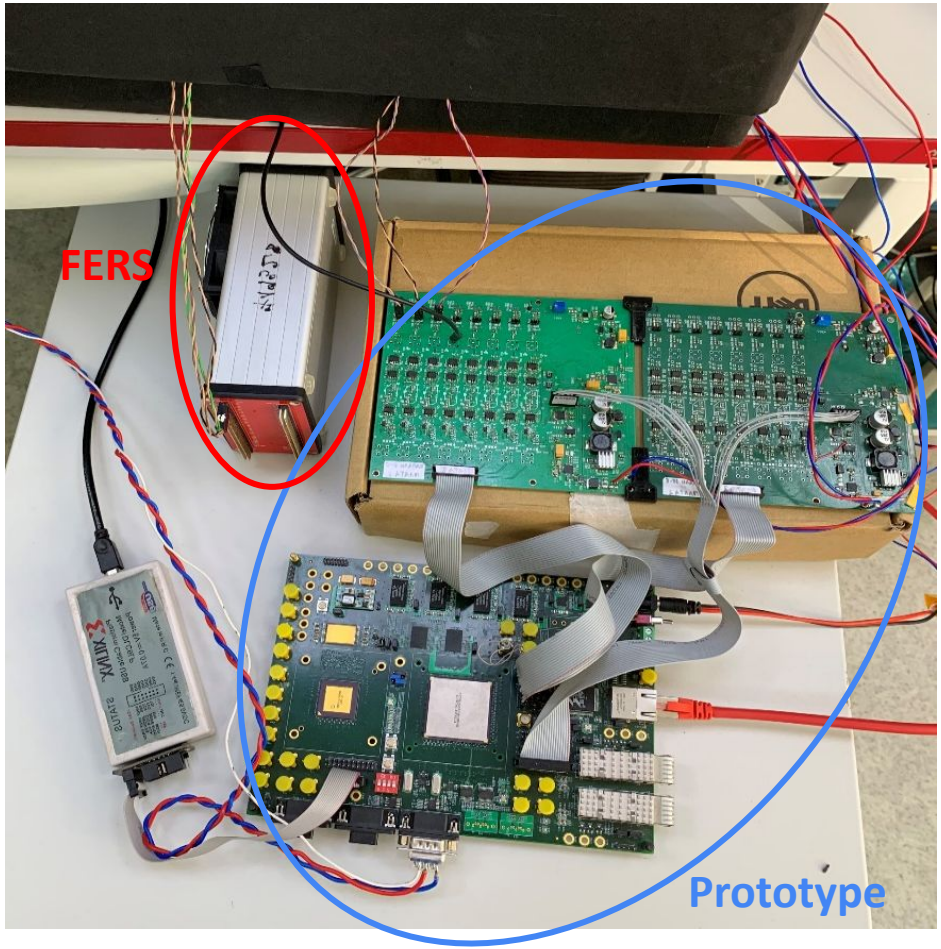
Motivation

- The data acquisition for the SPD is planned to be conducted in a triggerless mode using shared concentrators for synchronization and readout.
- The current CAEN FERS system has limited compatibility with SPD concentrators, making it suboptimal for the project's requirements.
- A new FEE system is being developed alongside with Phase 0 preparations to address existing limitations.



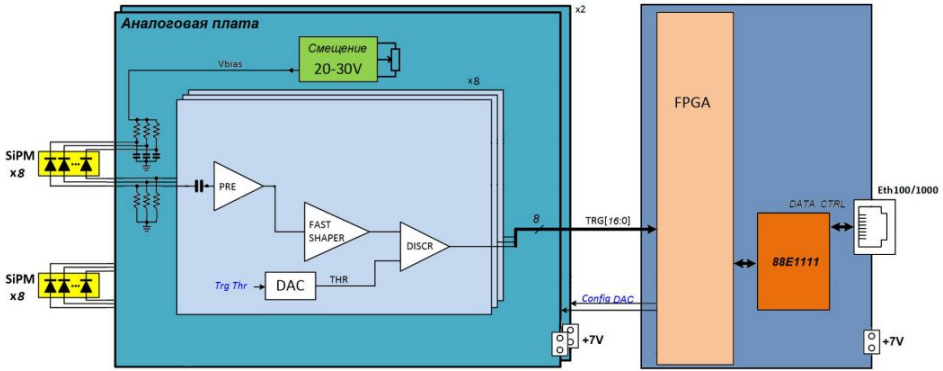
The leader of development is

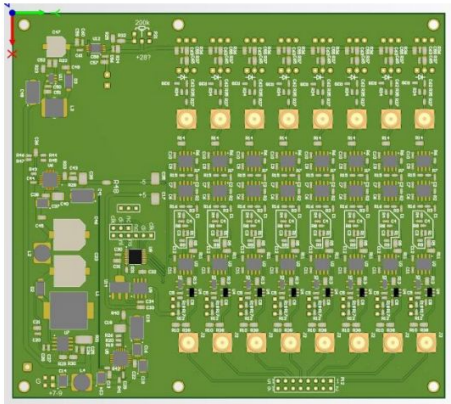
P. V. Nekrasov (MEPhI)

Prototype FEE specifications

Number of channels	16
Signal polarity	positive
Time resolution	18 ps
Discriminator threshold	12 bit programmable, for each channel
Power source	20-30 V
Working mode	streaming
Frequency	til 2 kHit/s
Shaping time	fixed, 20 ns
Time tagging	48 bit counter, 3 ns step
Interface	Ethernet 100/1000

New electronics scheme





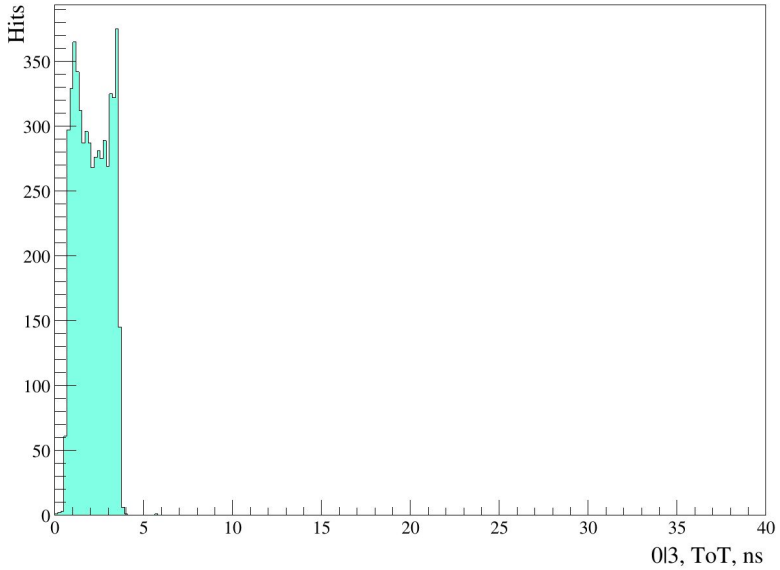
Front-end units
(SiPM supply, signal reading)

TDC based on FPGA
(XILINX VIRTEX-5)

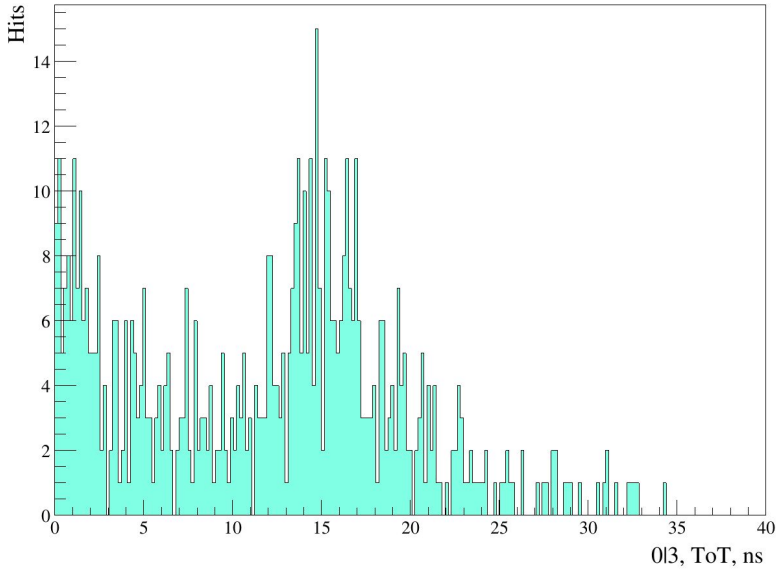
Tests with SiPM array using LED

For this test the assembly of 16 SiPM and LED connected to the signal generator are used.
Different conditions were tested.

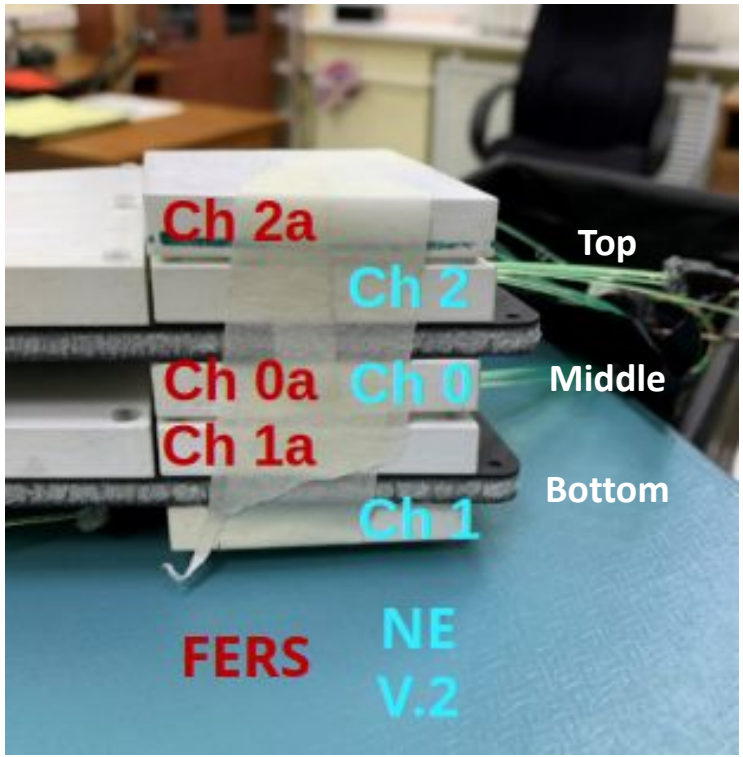
All channels occupied on the board

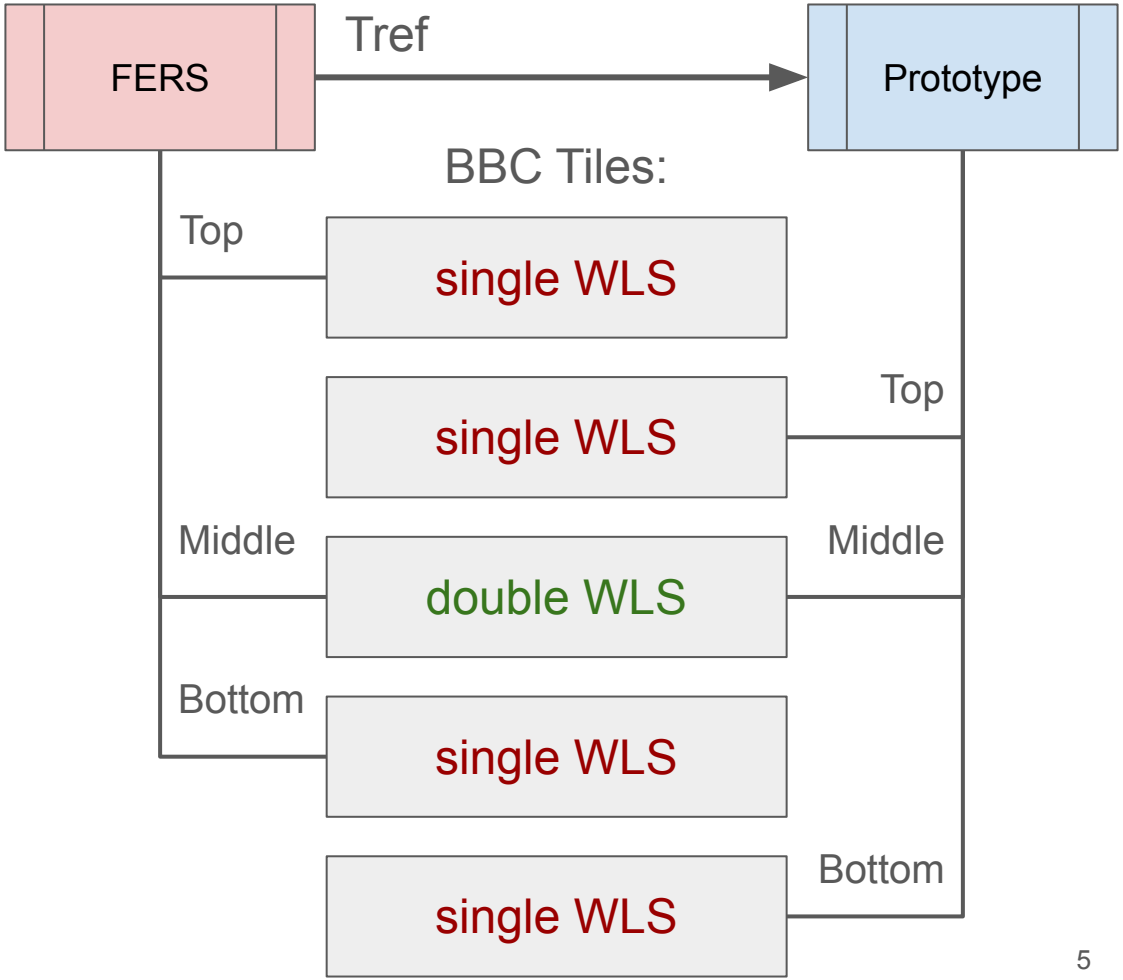


Occupied only 4 channels



FERS-Prototype comparison experimental setup

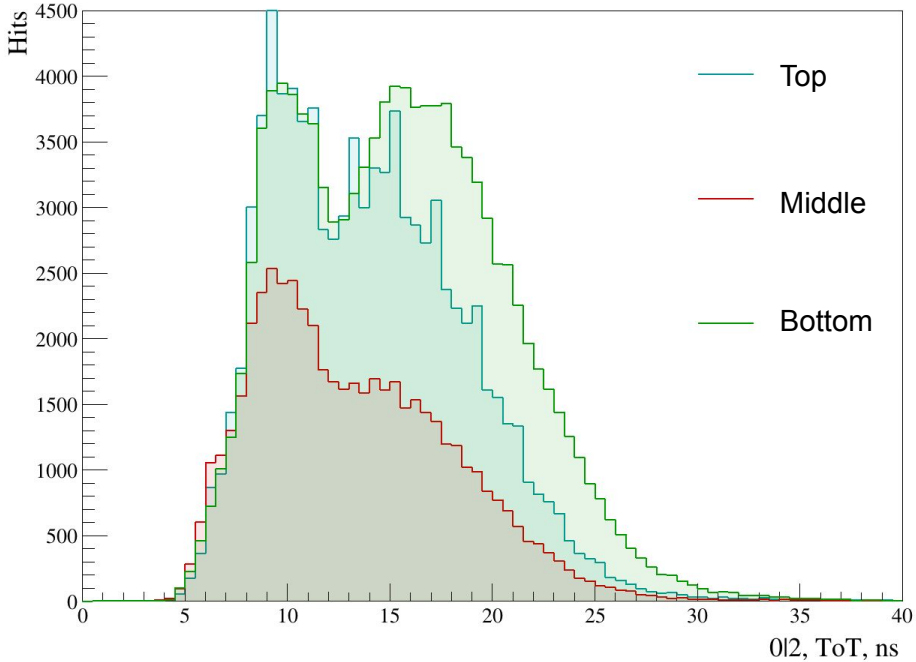


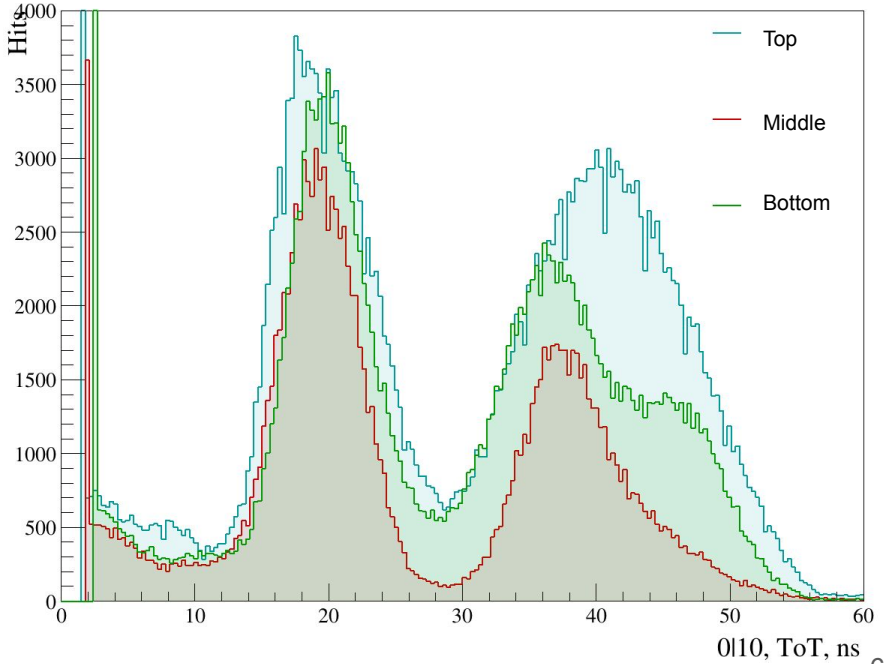


Independent Time-over-threshold distributions

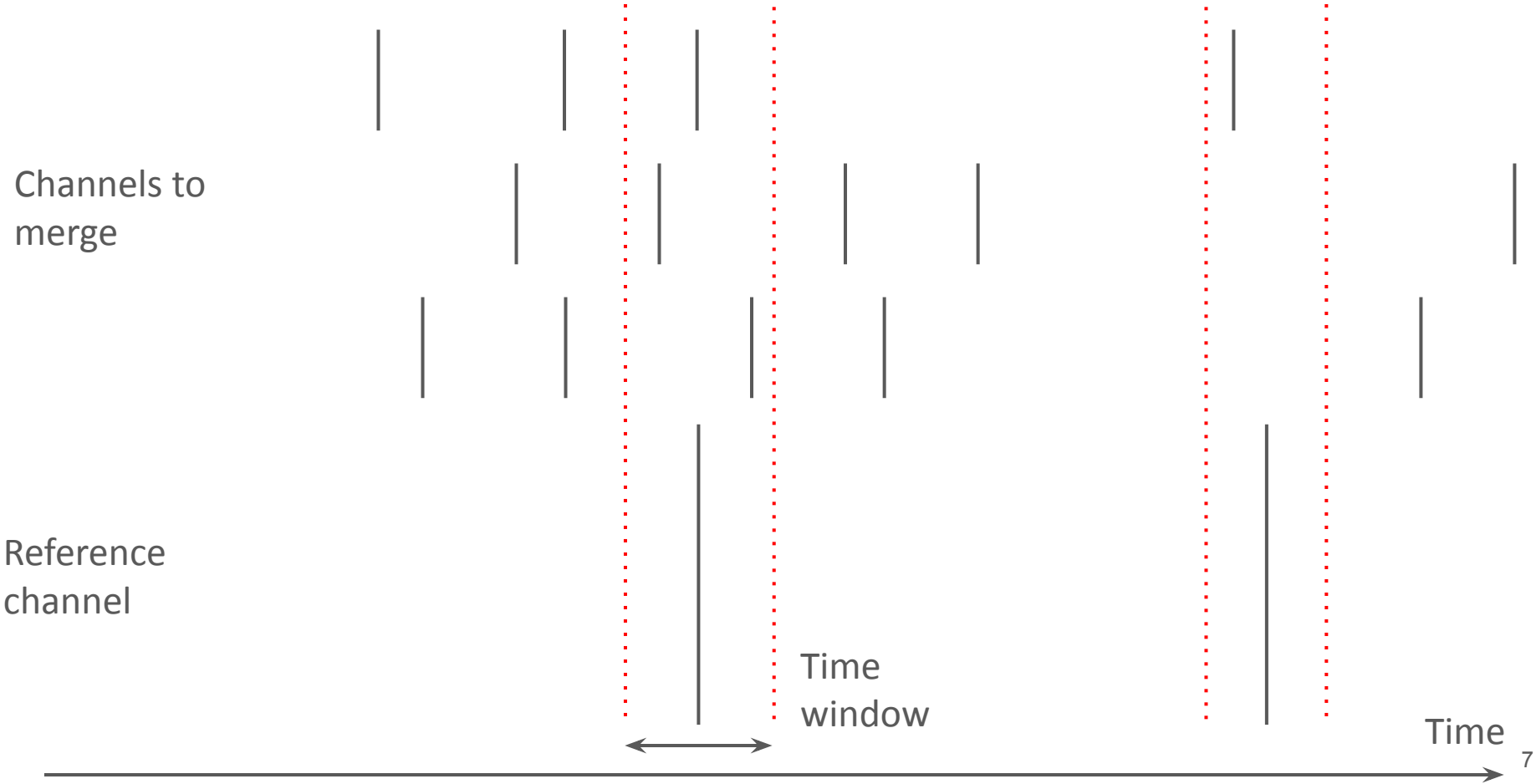
FERS

Prototype



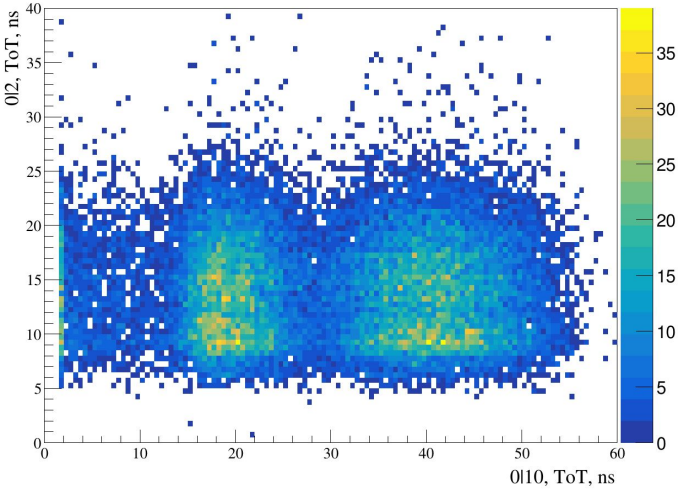


Selection scheme for direct comparison

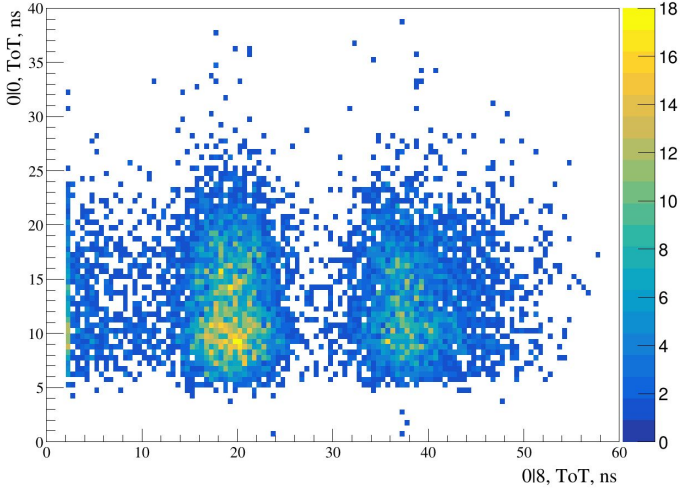


FERS-Prototype direct comparison

Top tiles



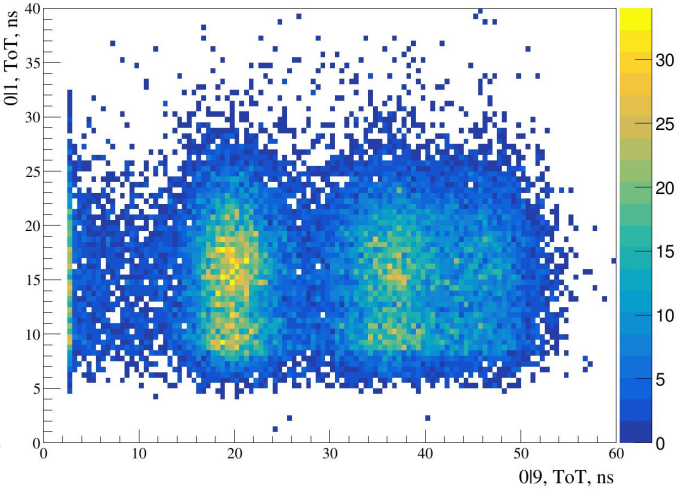
Middle tile



X - Prototype

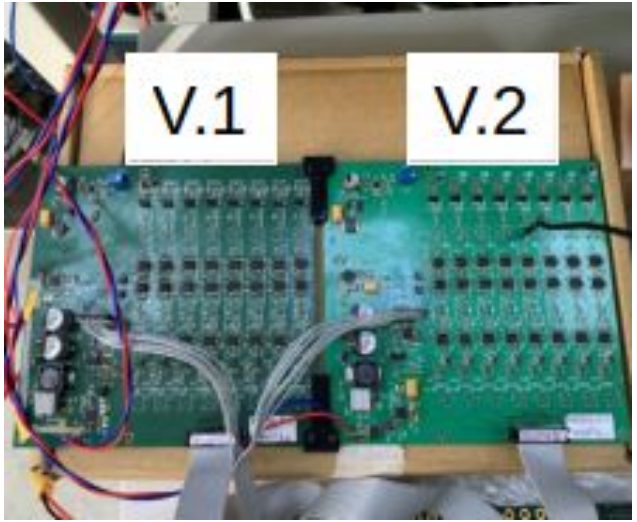
Y - FERS

Bottom tiles

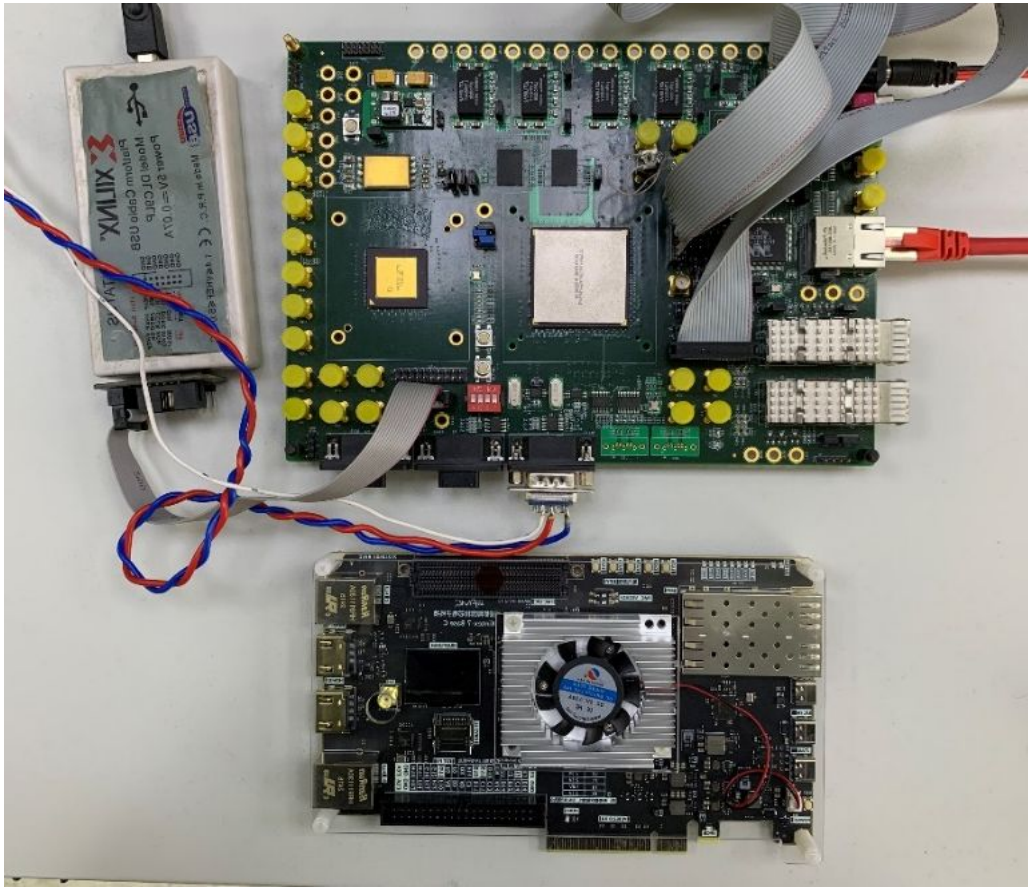


Nearest plans

- New analog part version (V.3)
- Transfer to the new FPGA board
- New tests!



FPGA XILINX VIRTEX-5 (current)



FPGA KINTEX-7 (new)

Conclusion

- The **first version** of the new FPGA based **Front-End Electronics** for BBC was **developed**.
- **Cross-FEE test** using **Prototype** and **FERS** with 5 tiles telescope were **performed**.
- The **next 64 channels version** of **FEE** that uses **KINTEX-7 FPGA** and **new analog part** is under **active development**.

THANKS TO YOU!
SINCERELY