# Status of DAQ system

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on behalf of DAQ group

# Why trigger-less DAQ?

**Bunch crossing each 76 ns; crossing rate 13.1 MHz,**
**Collision rate ~3–4 MHz** (1$^{st}$ stage about 100kHz)→
**Triggerless (or streaming) DAQ to avoid any hardware biases**

**Data flux was estimated for the maximum luminosity L = 10$^{32}$ cm$^{-2}$c$^{-1}$ and maximum energy √s = 27 GeV. Within simplified simulation and some safety margin the data flux is estimated as 20 GBytes/s.**

- No fast detectors to form a "classic" trigger signal
- No 4π detector with 100% efficiency to detect the collisions
- The wide SPD physical program eliminates a possibility of rejecting events at hardware level
- Bunch crossing time we will get from NICA via White Rabbit (probably). It will be used at event reconstructions to speed up the procedure.
- Probably the "Bunch crossing signal" can be used to reject a background/noise signal between the bunch crossing for the fast (SiPM based) detectors as a suppression signal to the Frond-End electronics or as a hardware filter based on the recorded time at the stage of data transfer.
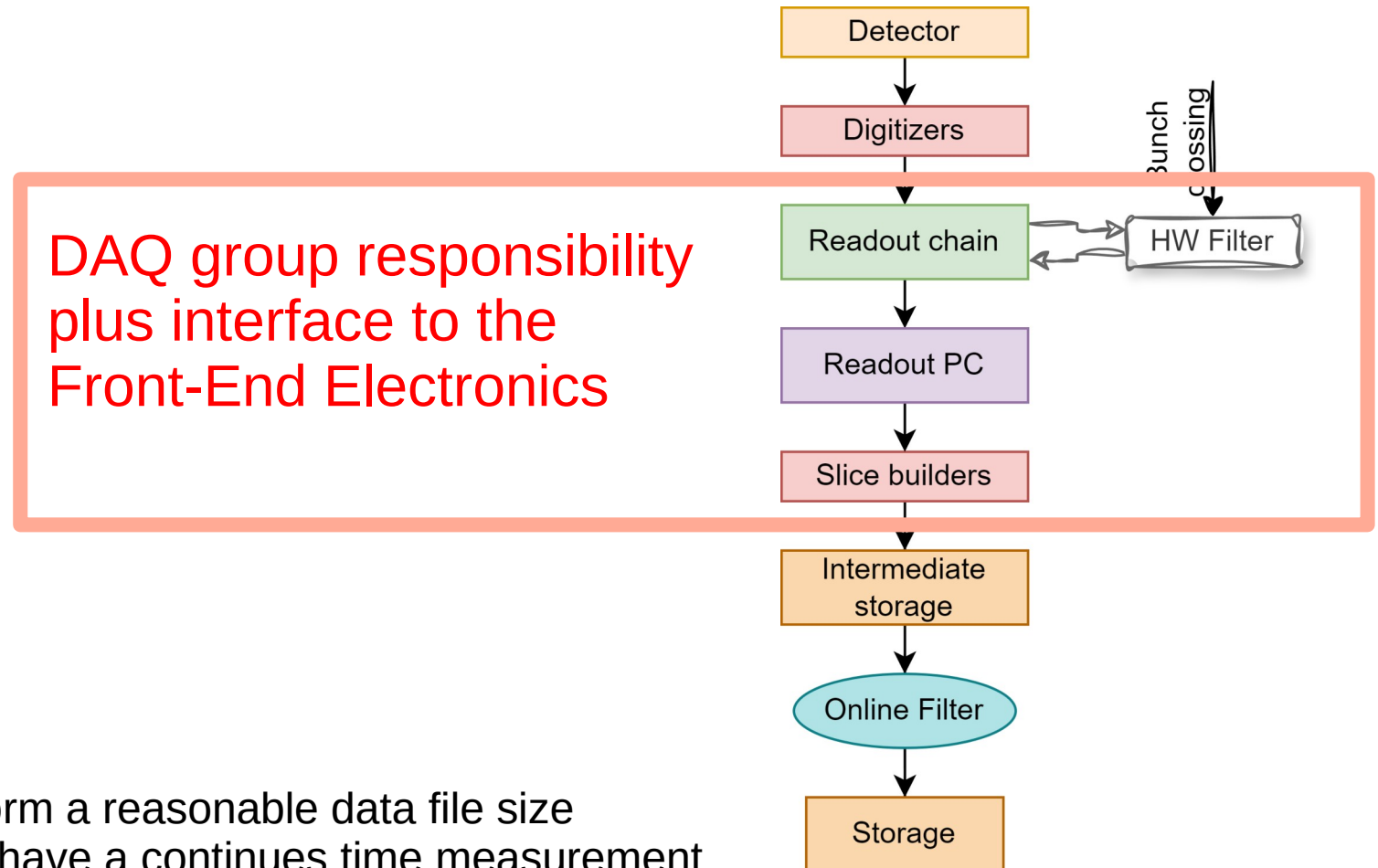  It is the only possible "hardware trigger", better say "data rejection".

# Front-end electronics for the triggerless DAQ

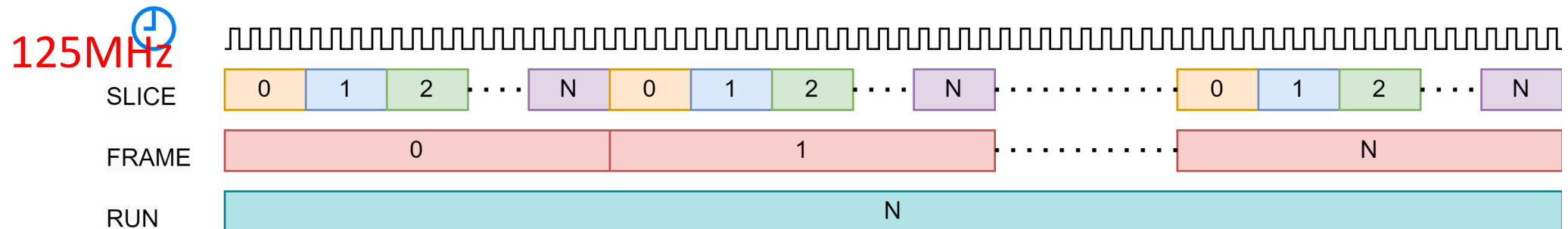Front-end electronics of the detectors has to meet the requirements of a free-running DAQ

General FEE requirements from the DAQ system:

○ Self-triggered (*trigger-less*) FEE operation

○ Digitizing on-board

○ Timestamp included in the output format – global clock 125MHz

○ Large memory to store the data accumulated in a time slice

○ Zero suppression

○ FPGA based digital output to DAQ with support of the DAQ control signals
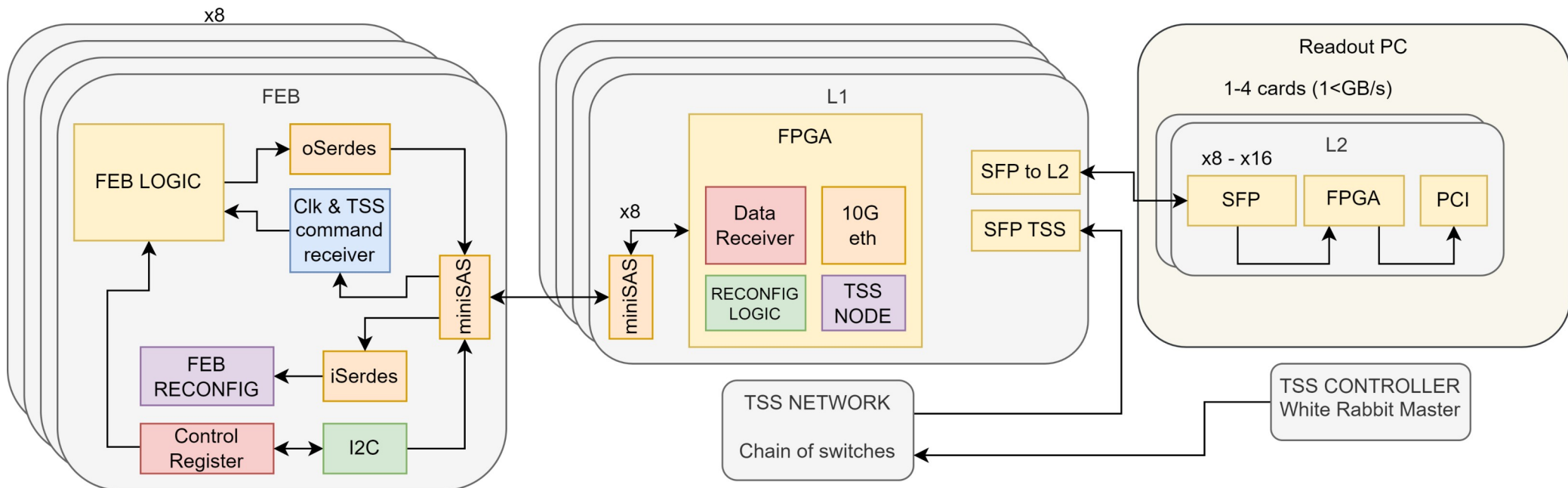
# Free-running / Streaming / Triggerless DAQ

DAQ group responsibility plus interface to the Front-End Electronics

Detector → Digitizers → Readout chain ↔ HW Filter (Bunch Crossing) → Readout PC → Slice builders → Intermediate storage → Online Filter → Storage

Slice: 10-100 µs – to form a reasonable data file size
Frame: 0.1-10 s – will have a continues time measurement

125MHz

SLICE: 0 1 2 ... N 0 1 2 ... N ... 0 1 2 ... N
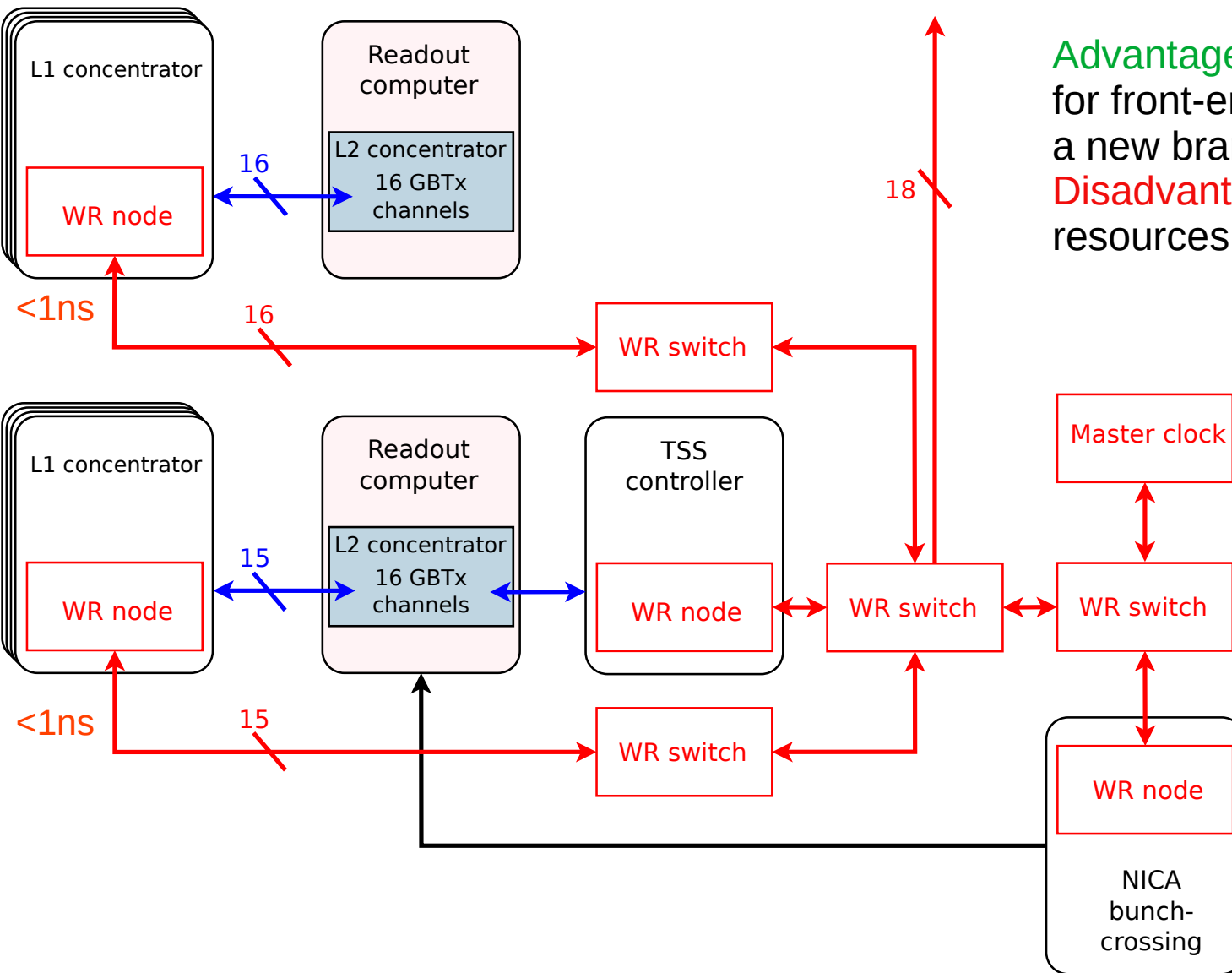
FRAME: 0 1 ... N

RUN: N

# SPD data transfer structure

# Readout chain

# Time Synchronization System with WR-based delivery



Advantages: time calibration needed for front-end cards only. Easy adding of a new branch/detector at any distance.
Disadvantages: expensive, time and resources consuming implementation.

White Rabbit is almost fixed as the synchronization protocol.

# L1 concentrator (Current prototype)

- Cyclone 10GX (105YF780E6G)
- 8x Links for connect front-end boards (miniSAS connectors) 8 diff pairs per connector
- SFP+ 10Gb transceiver for data transmission to L2
- SFP+ transceiver for TSS (White Rabbit)

Concentrator tasks:
- Collecting data from the front-end boards
- Distribution of clock and commands from TSS
- Data integrity and timestamp control
- Slow control for FEB
- Reconfiguring front-end boards (firmware)
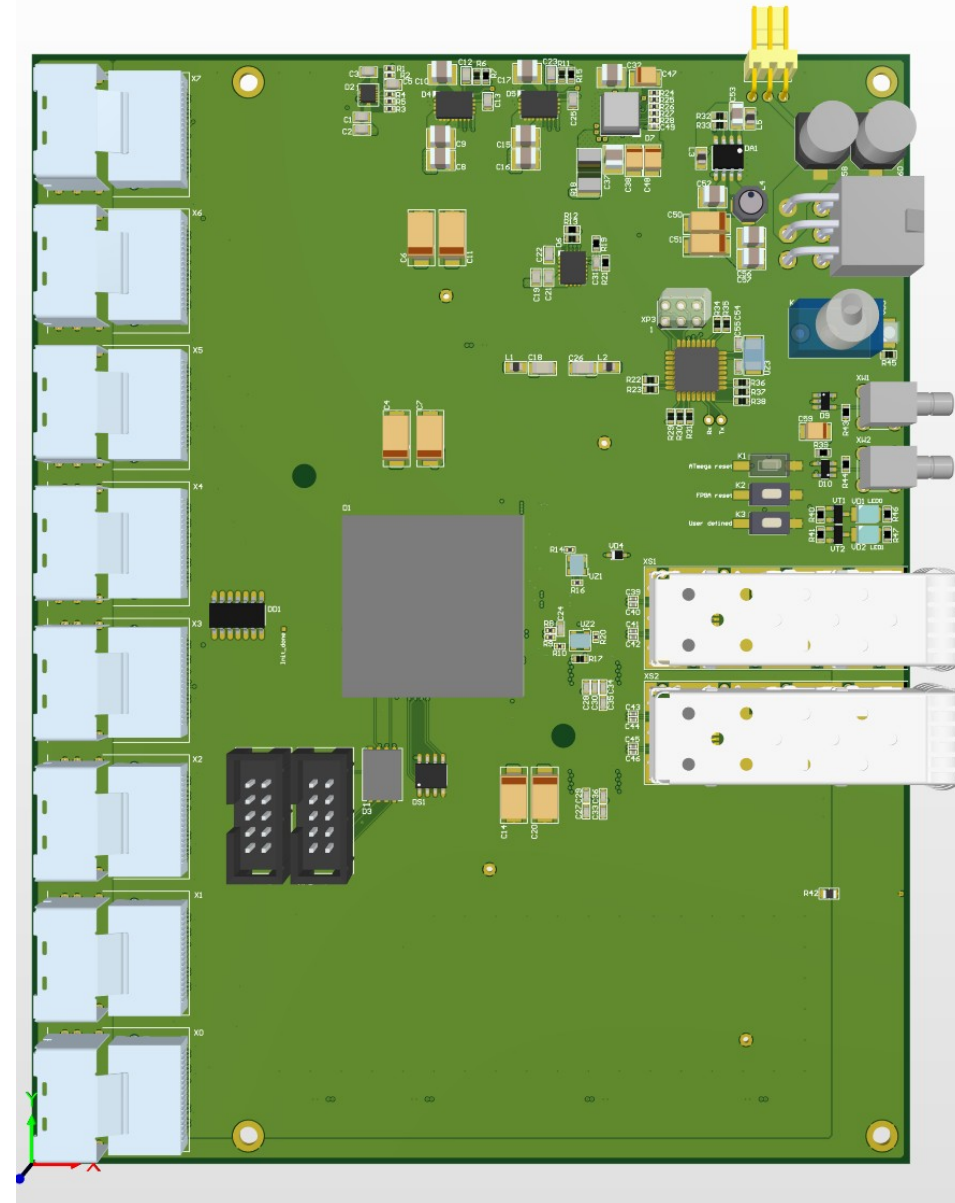


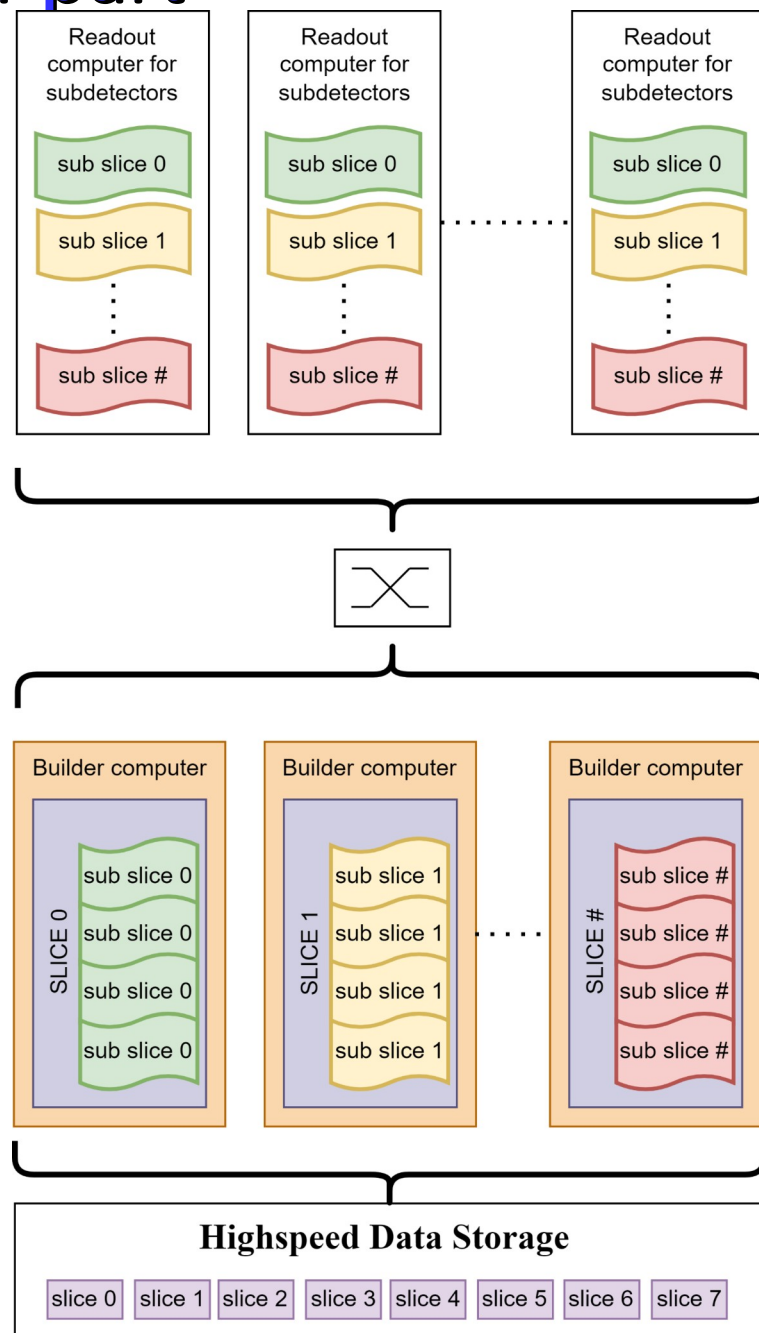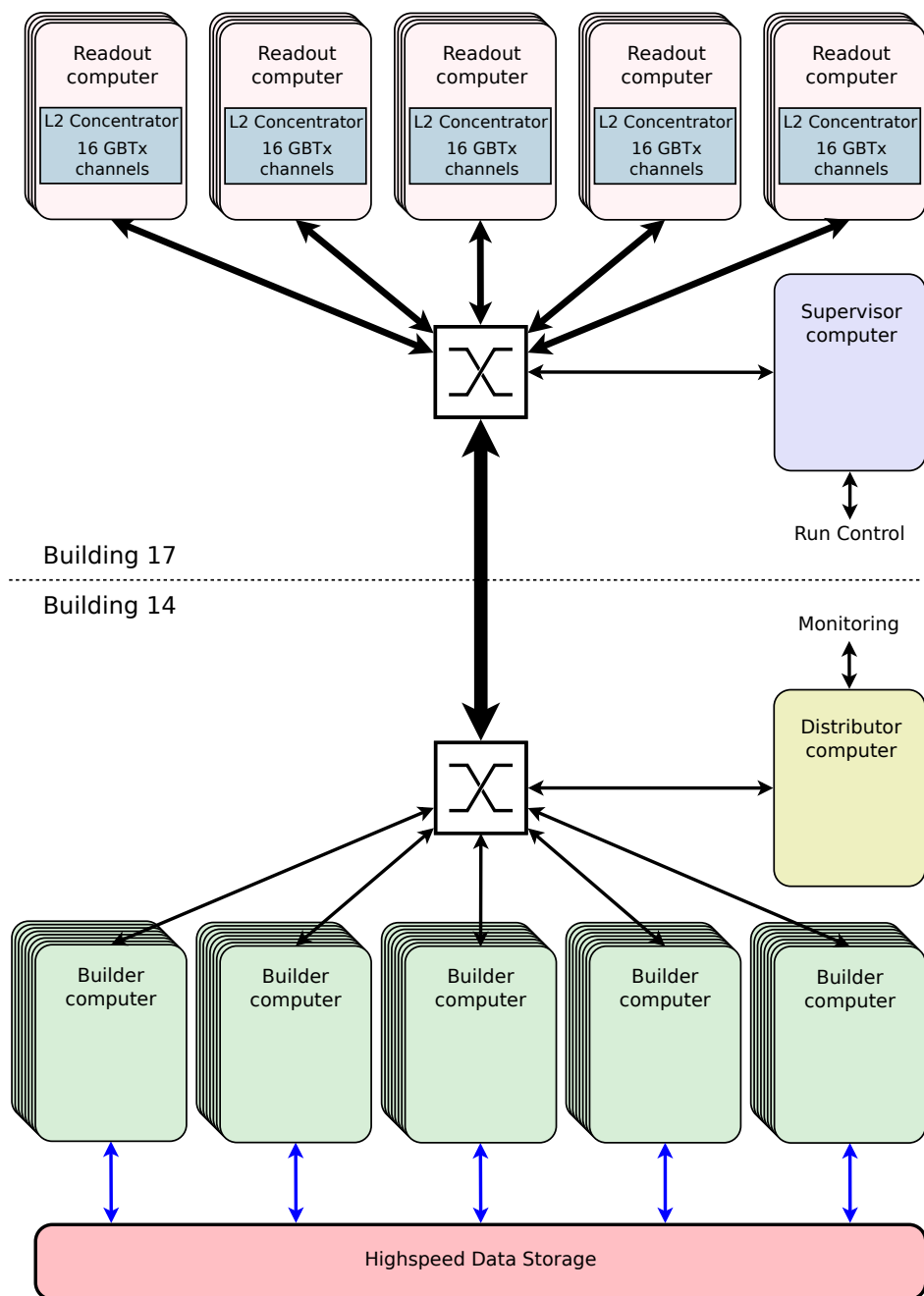The results of L1 development will be presented in the next talks.

# Development board for L2 concentrator

Prototype of L2 concentrator card:
ZYNQ UltraScale+ FPGA Development Board Z19-P form Alinx.



The results of L2 development will be presented in the next talks.
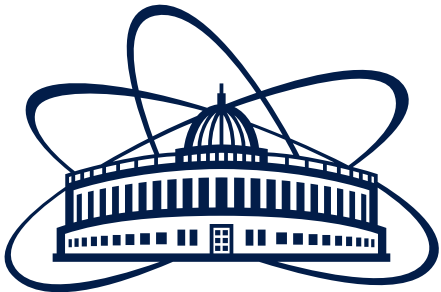
# DAQ computer part

# Open questions

- The prototype of Front Electronics cards exists for RS and for Micromegas Tracker under development. We NEED contribution from all other detector groups.

- Where L1 Concentrator will be installed: inside or outsides the Range system? (e-link <10m)
- Radiation hardness of FPGA, in the case of installation of L1 Concentrator inside the Range system
- Which Time Synchronization: White Rabbit is almost fixed as the synchronization protocol.

# Continue R&D

# Progress

- We have prepared a paper for the NIM journal.
- We have the really working collaboration for development of the DAQ hardware:
  JINR Dubna,
  St. Petersburg Polytechnical University,
  Tomsk State University.

# Thank you for your attentions.