Status of L1 concentrator

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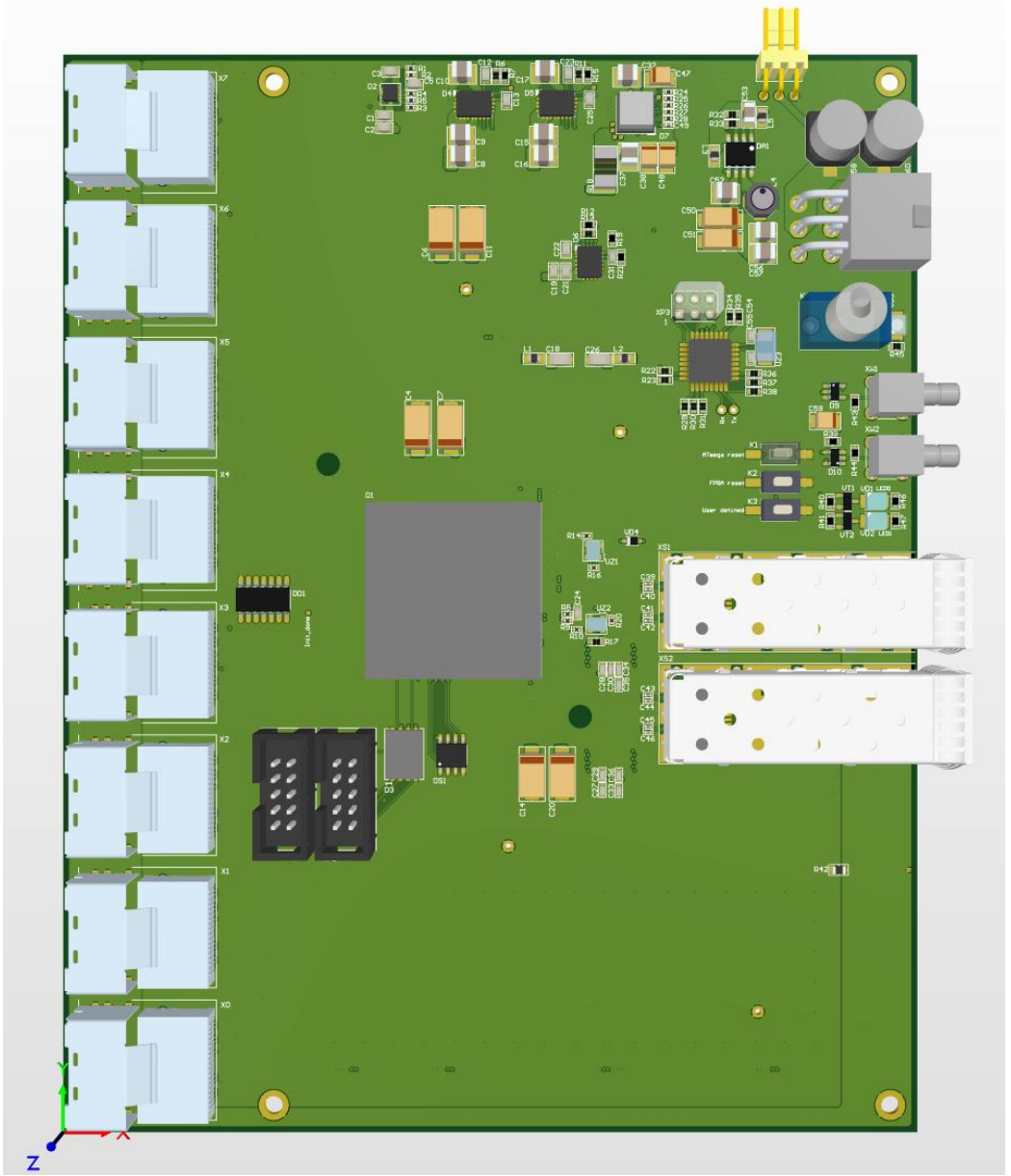
PCB of L1 concentrator (Current prototype)

- Cyclone 10GX (105YF780E6G)
- 8x Links for connect front-end boards (miniSAS connectors) 8 diff pairs per connector
- SFP+ 10Gb transceiver for data transmission to L2
- SFP+ transceiver for TSS (White Rabbit)

Concentrator tasks:

- Collecting data from the front-end boards
- Distribution of clock and commands from TSS
- Data integrity and timestamp control
- Slow control for FEB (thresholds, etc.)
- Reconfiguring front-end boards (firmware)

A new prototype is planned for creation by autumn.



PANGOMICRO (option for L1)

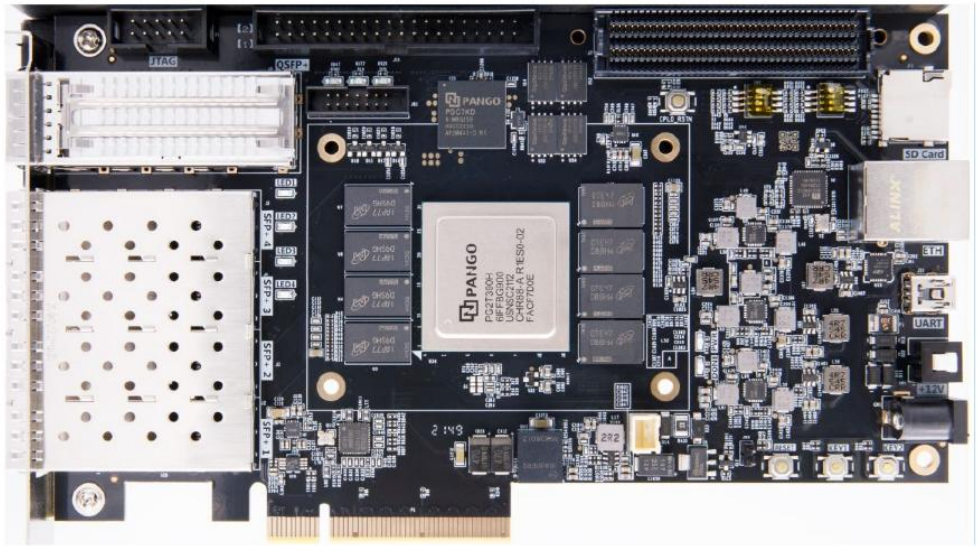
Pangomicro TITAN 2 (*Chinese FPGA*)

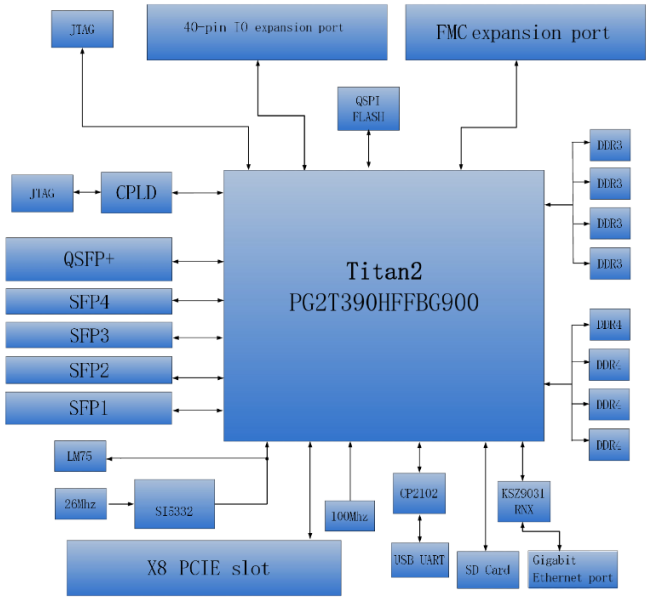
- Available for us *(without sanctions)* cost 220$ per chip
- Pin2pin compatible Xilinx Kintex 7 (*differences in architecture*)
- More resources compared to Cyclone 10GX
- Not detailed documentation
- There are a lot of problems with the IDE *(at the moment)*

Resource name		PG2T390H
CLM	LUT6	243600
	logical unit	389760
	FF	487200
	Distributed ram (Kb)	4712
DRM (36Kbits/ pc)		480
APM(units)		840
PLLs	GPLLs	10
	PPLLs	10
ADC (dual core)	Dedicated analog channel (differential input pair)	1
	Multiplexed analog channels (differential input pair)	11
SERDES LANE [1]		16
PCIE GEN2×8 CORE		1

ALINX APX390 *(Current available development board for TITAN 2)*

- Good documentation and reference designs for work
- Today:
  - ✓ Ready 10G link
  - ✓ SerDes IP is study (Need hardware test with FMC board)
  - ✓ CDR (clock data recovery) mode is not available (by default).
- We need to explore White Rabbit integration *(Together with SPbPU group)*.





E-Link *port*

Dedicated line for:

- Start of slice
- Start of frame
- Set Next Frame
- Global clock from L1 to Front-End

- Data line (Max 1250 Mbps) & CLK line
- Data line for FEB firmware reconfiguration / slow control (Thresholds, etc.) & CLK line

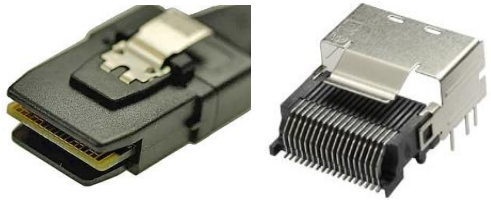
- 8 Unipolar lines for slow interface and different signals

Electrical standard:

- LVDS for differential signals (Data/CLK/TSS)
- LVTTL (3.3 V) for unipolar signals

Line on FEB	Signal description	Line on L1	Comments
TX0	Data line from FEB	RX0	
TX1	Clock line from FEB	RX1	
TX2	Data line from L1	RX2	Data line for slow control and reconfig
TX3	Clock line from L1	RX3	Synchronization Clock for data line from L1
RX0	Clock TSS from L1	TX0	Global clock from TSS
RX1	Start of Slice (SNF)	TX1	
RX2	Start of Frame (SOS)	TX2	
RX3	Set Next Frame (SOF)	TX3	Frame number (32 bit data)
Unipolar 0	Reset (HARD)	Unipolar 7	Hard reset of FEB (active hight)
Unipolar 1	SCL (SCLK)	Unipolar 3	I2C CLK / SPI CLK
Unipolar 2	SDA (CS_1)	Unipolar 4	Data I2C/ CS SPI
Unipolar 6	NC /(CS_2)	Unipolar 5	NC /CS SPI
Unipolar 7	NC /(MOSI_L1)	Unipolar 0	NC/Data from L1
Unipolar 3	NC /(MISO_L1)	Unipolar 1	NC/Data from FEB
Unipolar 4	Ready (From FEB)	Unipolar 2	Handshake for SerDes lines
Unipolar 5	Ready (From L1)	Unipolar 6	Handshake for SerDes lines

MiniSAS



Pin function	Side B Pin	Side A Pin	Pin function
GND	B1	A1	GND
Tx0+	B2	A2	Rx0+
Tx0-	B3	A3	Rx0-
GND	B4	A4	GND
Tx1+	B5	A5	Rx1+
Tx1-	B6	A6	Rx1-
GND	B7	A7	GND
Unipolar 0	B8	A8	Unipolar 7
Unipolar 1	B9	A9	Unipolar 3
Unipolar 2	B10	A10	Unipolar 4
Unipolar 6	B11	A11	Unipolar 5
GND	B12	A12	GND
Tx2+	B13	A13	Rx2+
Tx2-	B14	A14	Rx2-
GND	B15	A15	GND
Tx3+	B16	A16	Rx3+
Tx3-	B17	A17	Rx3-
GND	B18	A18	GND

FEB-L1 test

Now:

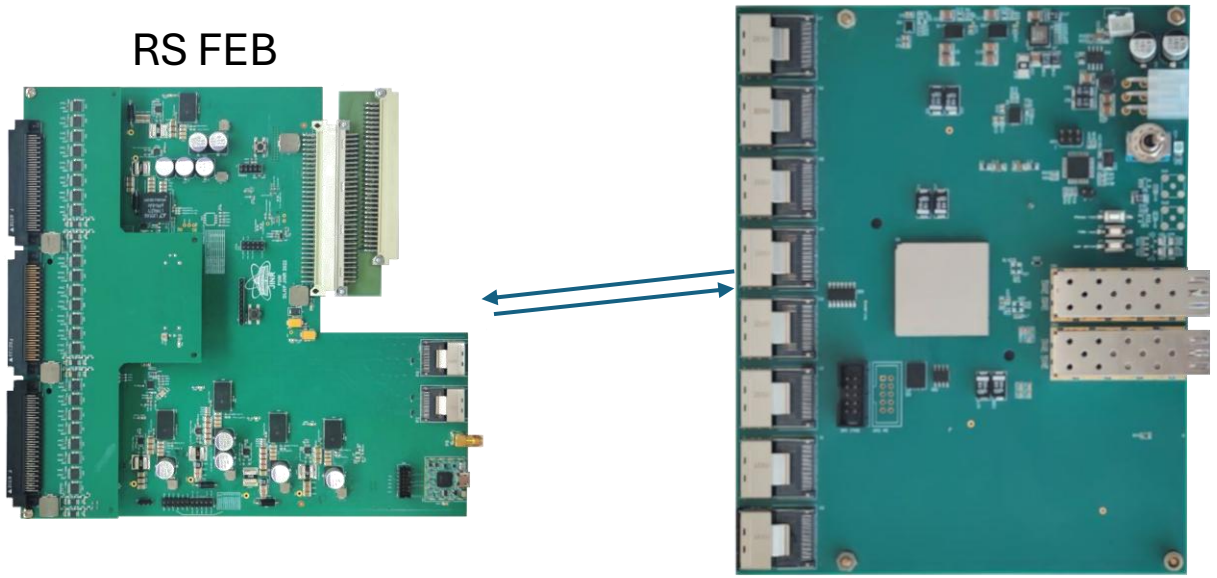
- Base clk for SerDes (L1-FEB-L1): 100Mhz
- Only 8b10b tested without packet structure

Plans:

- Up base clk for SerDes (L1-FEB-L1): 125Mhz
- Define a packet structure for RS-FEB
- Start of development procedure for reconfiguration RS-FEB via L1

RS FEB

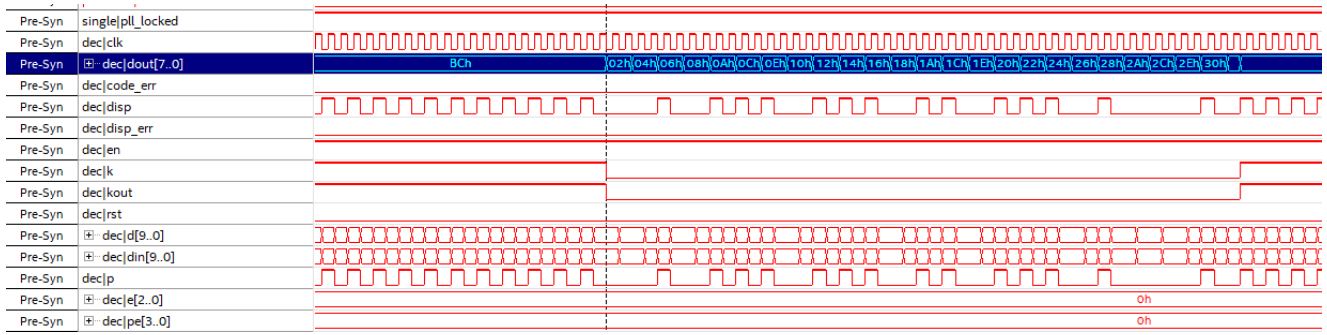
L1 prototype



Example FEB Packet (Green frame)

L2 Header	L2 Port 4 Bit				L2 ID 8bit	Reserved	
L1 Header	L1 Port 4 Bit				MSB of Frame Number 12bit		MSB of Slice Number 16 bit
FEB DATA BLOCK	1	0	X	X	Format ID 4 bit	LSB of Frame Number 8bit	LSB of Slice Number 16 bit
	0	0	X	X	FEB DATA #0		
	0	0	X	X	FEB DATA #1		
	...						
	0	0	X	X	FEB DATA #255		
	1	1	X	X	ERROR CODE 8 bit	TOTAL WORDS 20 BIT	

RS-FEB Test packet waveform (24 bytes)



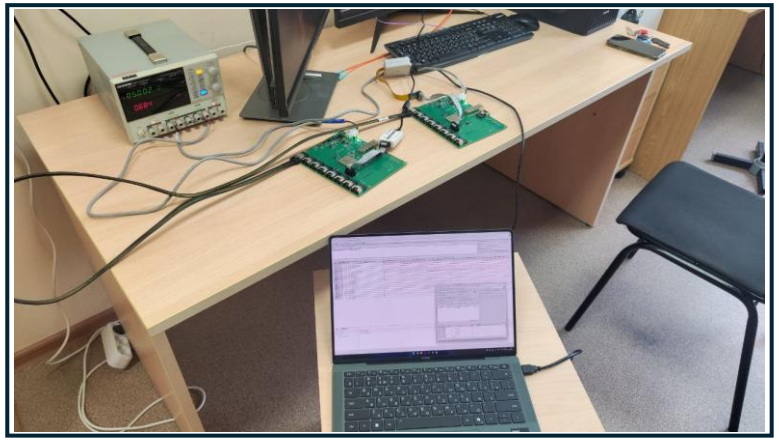
E-Link bandwidth test

DAQ Group Setup

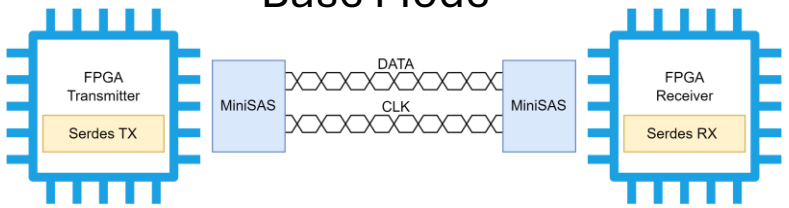
1. Two boards (Cyclone 10GX based)
2. MiniSAS cable 1.5 m
3. Only 8b10b tested

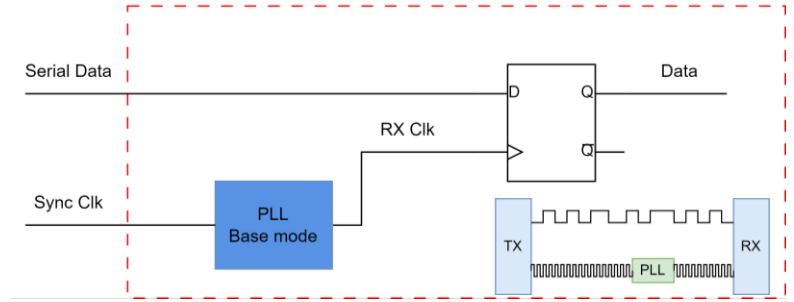
Monitoring and control via JTAG

Plans: Test with RS-FEB



Base Mode

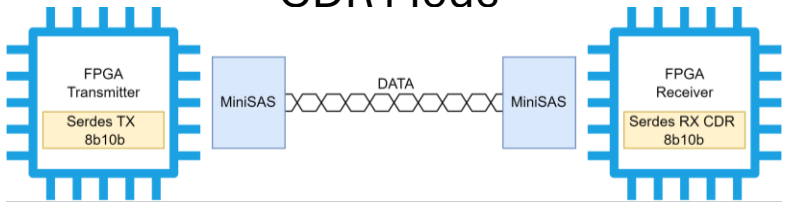


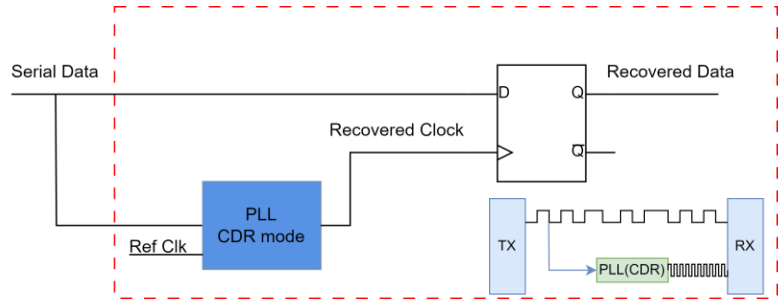


Link bandwidth per line:

150 Mbps – OK
500 Mbps – OK
750 Mbps – OK
1000 Mbps – OK
1250 Mbps – OK

CDR Mode





Link bandwidth per line:

150 Mbps – OK
500 Mbps – OK

NEW RESULTS

750 Mbps – OK
1000 Mbps – OK
1250 Mbps – OK

E-Link & WR refactor for next L1 prototype

Cyclone 10GX require strict definition of signal lines.

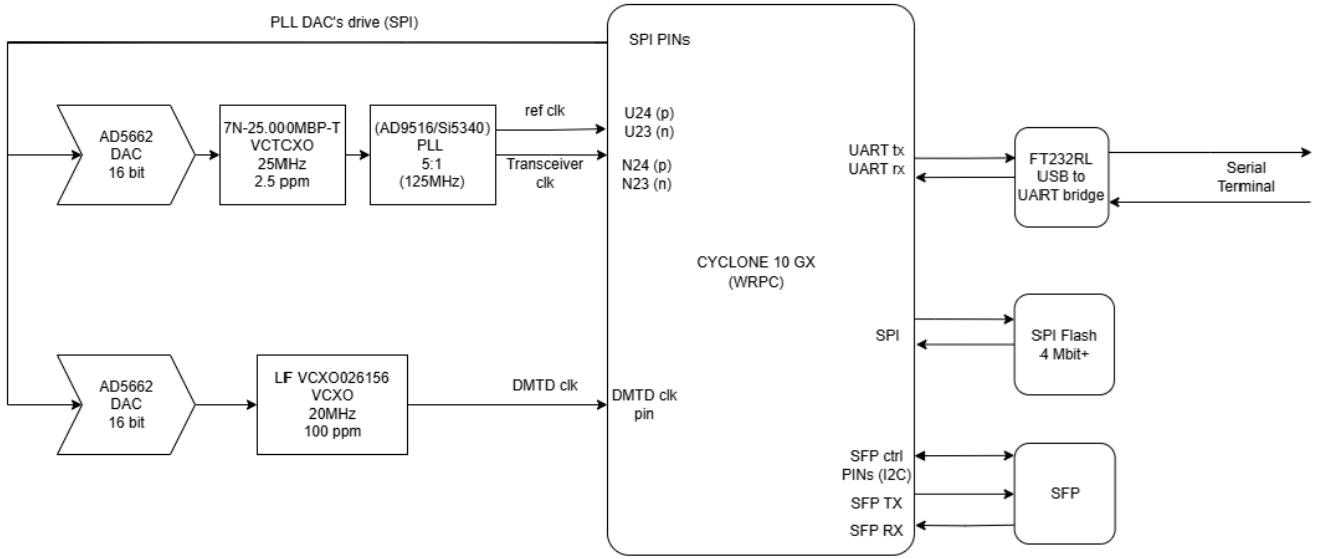
E-LINK requirements:

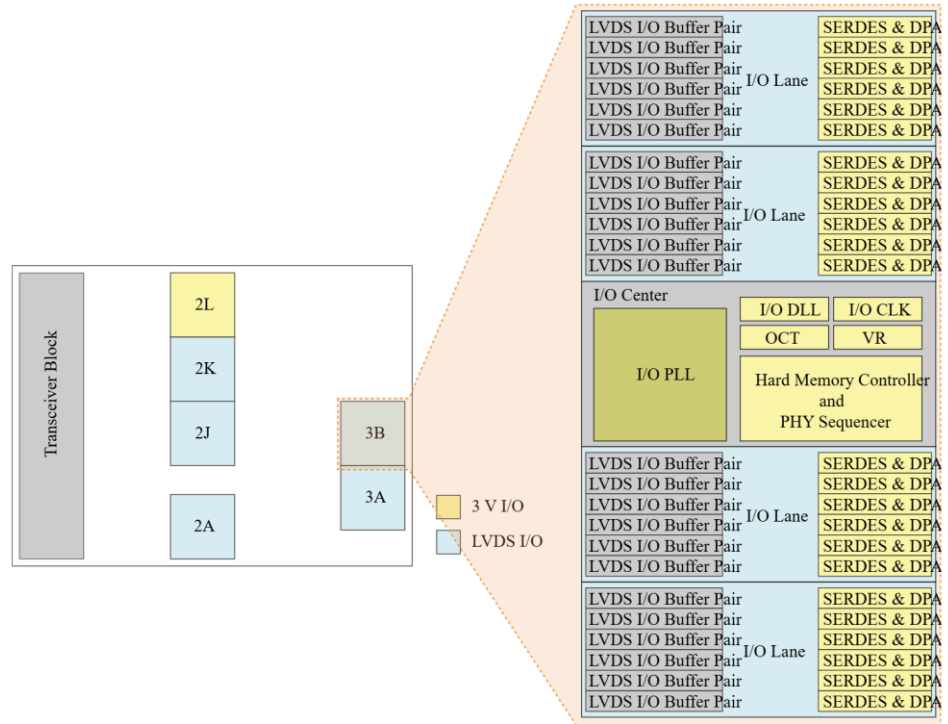
- Dedicated FPGA Bank's for RX signals
- Dedicated FPGA Bank's for TSS & TX signals

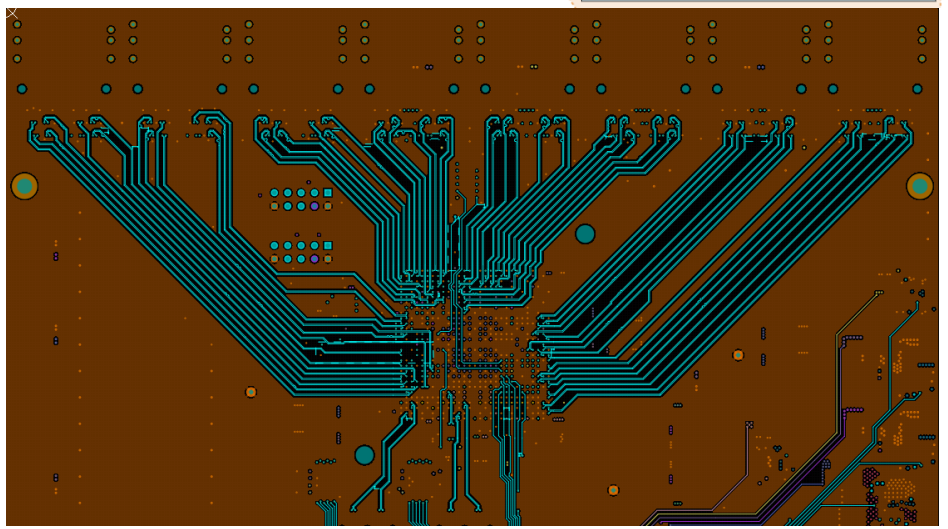
WR requirements:

- DAC 16 bit (x2) *for refClk phase adjustment*
- VCO-oscillators (25/125 MHz 2.5ppm) (x2)
- External memory for settings
- UART – for test's

(Provided SPbPU group)





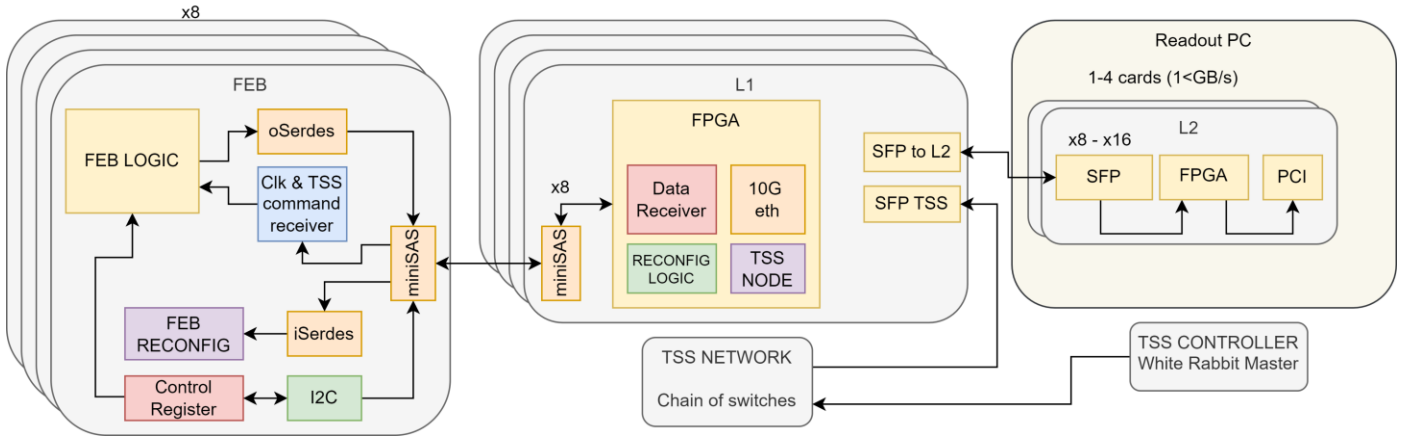


Remote stand

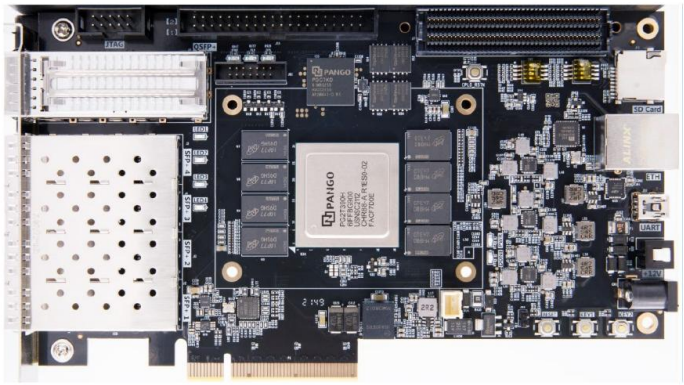
Plans on July – August (together TSU-group):

- Prepare a remote stand:
  - Hardware server
  - FEB-emulator & L1 & L2
  - USB hub for JTAG (remote control)
  - Power supply (remote control)
  - White Rabbit network (one switchboard)

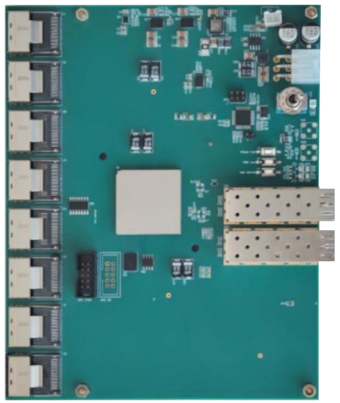
- Prepare Dockers with Vivado/Quartus + QuestaSim
- Setting up a dedicated PC to run long simulations, build projects and storage of Docker's (Each docker size 50-120 GB)



FEB Emulator (Need FMC with MiniSAS)



L1



L2

Conclusion

- It is planned to create a new prototype with:
  - White Rabbit Core (endpoint)
  - Correct E-LINK assignments
- Work continues to explore an alternative platform for L1.
- Work has begun on testing the integration between L1 and FEB
- It is planned to deploy remote stands for collective development

Thanks for your attention

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