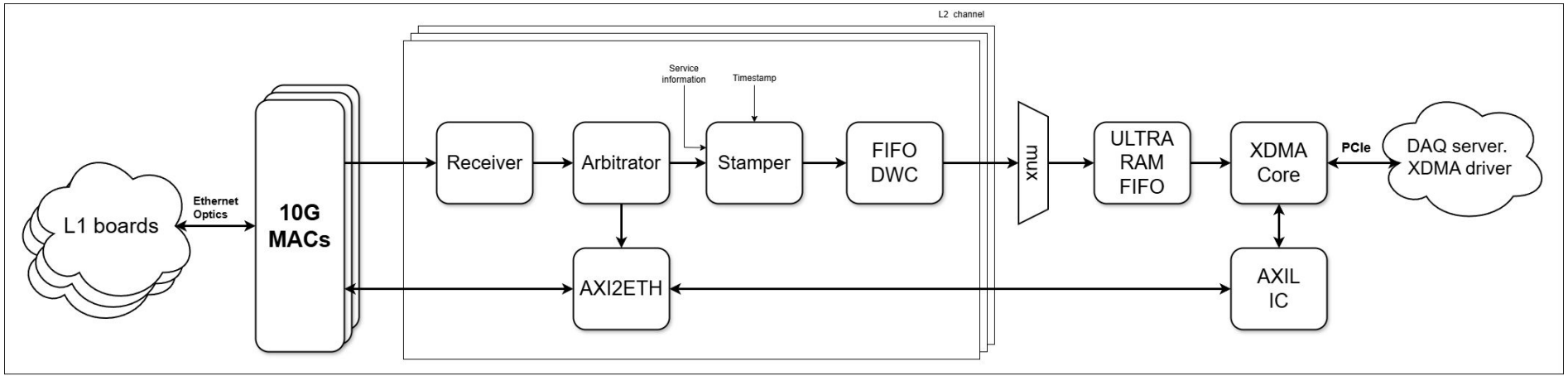
National Research Tomsk State University

Laboratory of High Energy Physics Data Analysis
Tomsk State University

Current status of the L2 concentrator development.

Andrei Berngardt, Vladislav Borshch, Dmitriy Erofeev, Kirill Zhidkov, Olga Petrova, Irina Shreyber, Sergei Filimonov.

L2 FPGA architecture



Full readout pipeline is completed. Testing and integration is ongoing

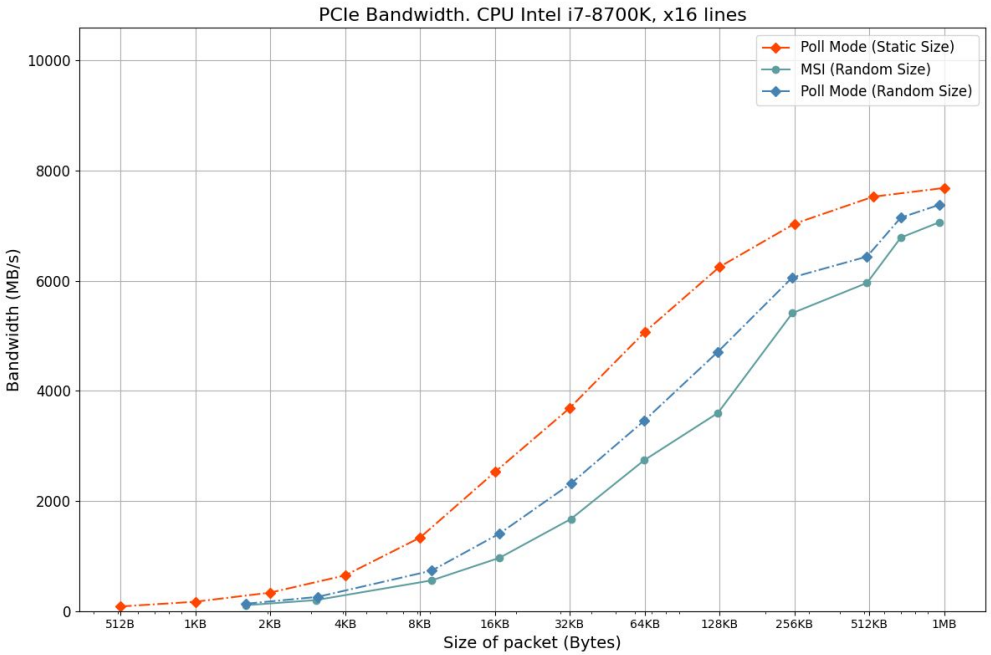
Ethernet channels

The number of sfp channels in the design is now controlled by a parameter.

We decided to switch to open-source Ethernet cores to achieve better resources utilization.

8 optical 10G Ethernet channels are under tests.

DMA Core



We tested XDMA performance with static and random sized packets.

Current performance of PCIe 3.0 x16 interface with XDMA core is acceptable for the prototyping and future developments.

The possible improvements: switch from XDMA to QDMA - improve performance for short packets; improve performance and algorithms of API

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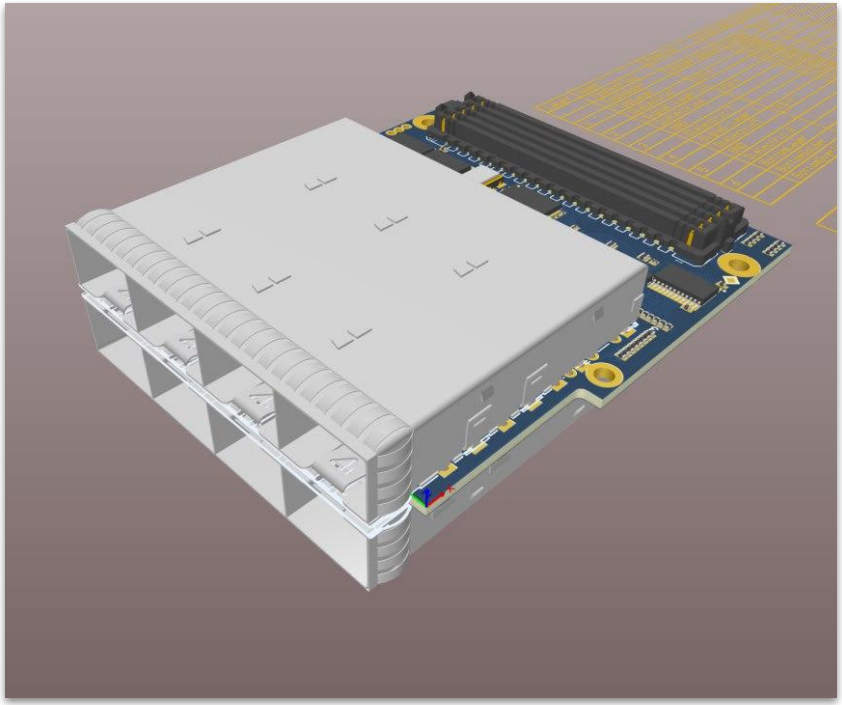
New mezzanine card development



Design for 8 SFP channels mezzanine card has been developed.

Two prototypes are planned to be purchased by JINR

Ongoing work

1) Transition to open-source ethernet cores and also testing them.
2) Enhancing algorithms and the DMA’s API
3) Optimization of new mezzanine card (we want to make them cheaper).
4) Development of tests using UVM.
5) JINR “START” program participation (integration of L2 with L1 and DAQ software).

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Thank you!

Laboratory
of High Energy Physics
Data Analysis

Tomsk
State
University

National Research
Tomsk State
University
36, Lenina Avenue, Tomsk, 634050, Russia
Tel.: +7 (3822) 529 852, fax: +7 (3822) 529 585
E-mail: rector@tsu.ru

www.tsu.ru