Передовые инженерные школы

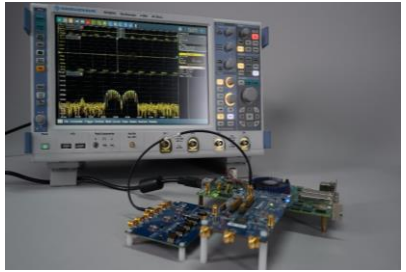
POLYTECH
Peter the Great St.Petersburg Polytechnic University

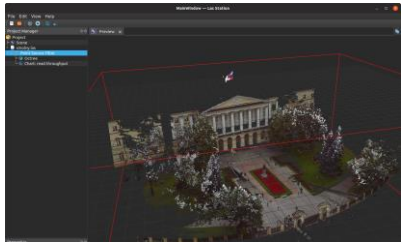
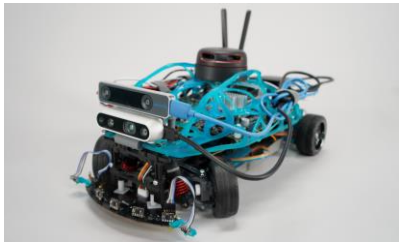
ЦИФРОВОЙ ИНЖИНИРИНГ
ПИШ СПбПУ

WCRC
ADVANCED DIGITAL TECHNOLOGIES

POLYTECH
Advanced Manufacturing Technologies Center
National Technology Initiative

POLYTECH
Laboratory
Industrial Systems for Streaming Data Processing



SPD-meeting

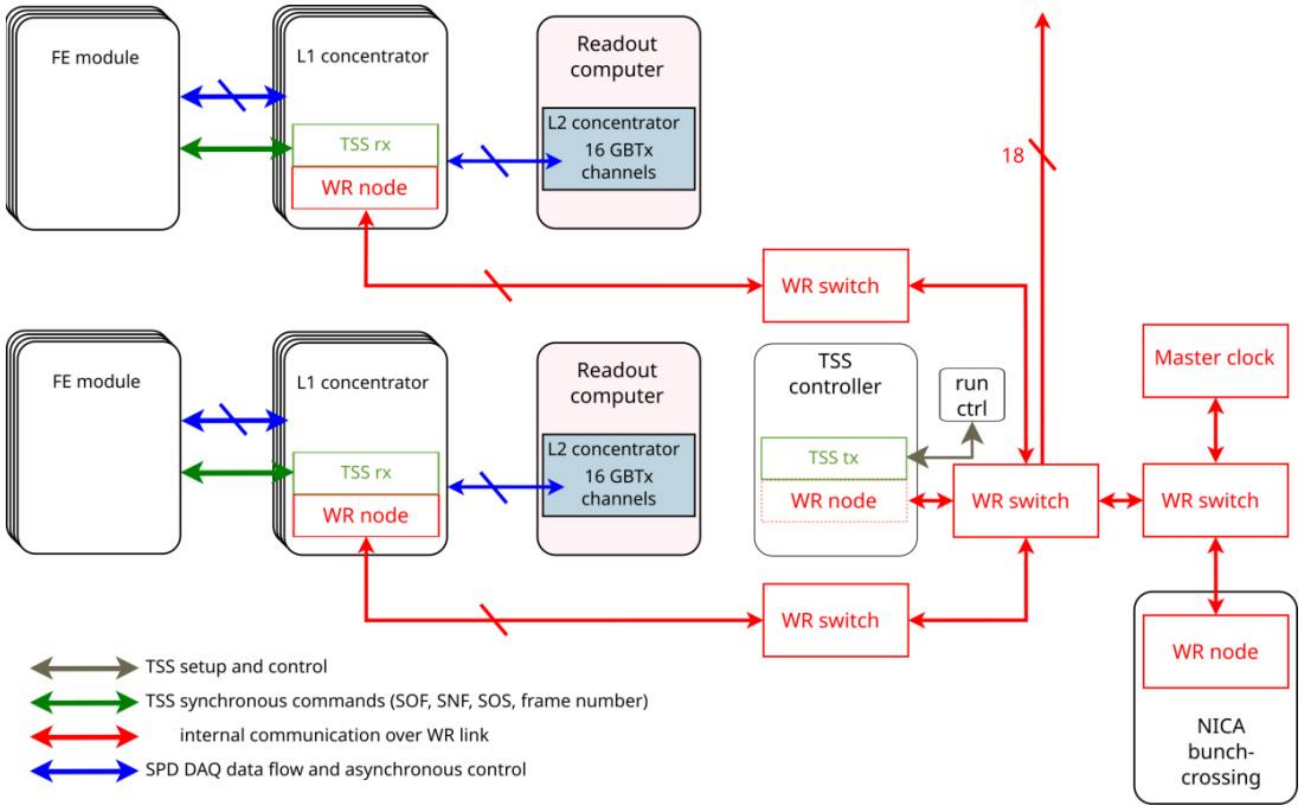
May 12th, 2025

Status of TSS development. TSS control protocol v2. First test runs.

Kirill Kotov, Technician

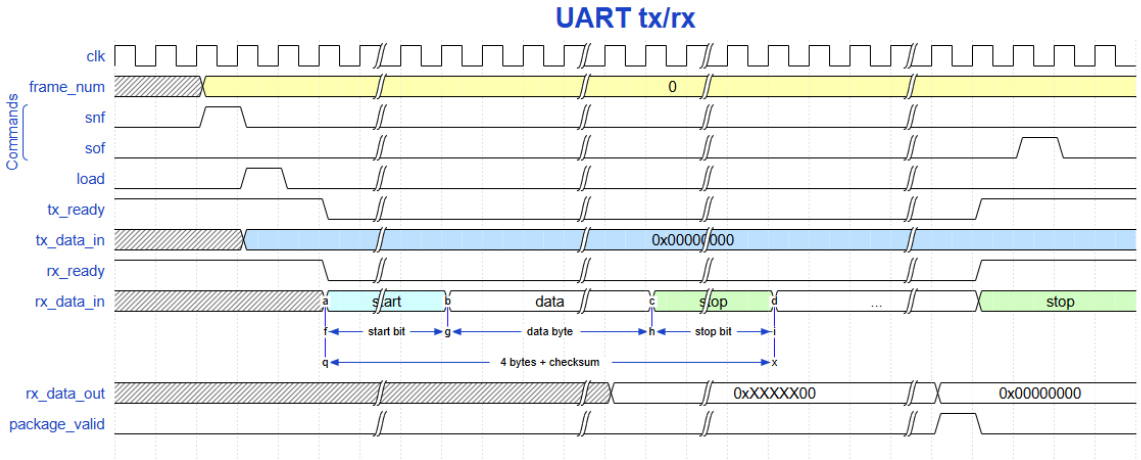
Industrial Systems for Streaming Data Processing Laboratory,
Peter the Great St. Peterburg Polytechnic University

TSS Architecture

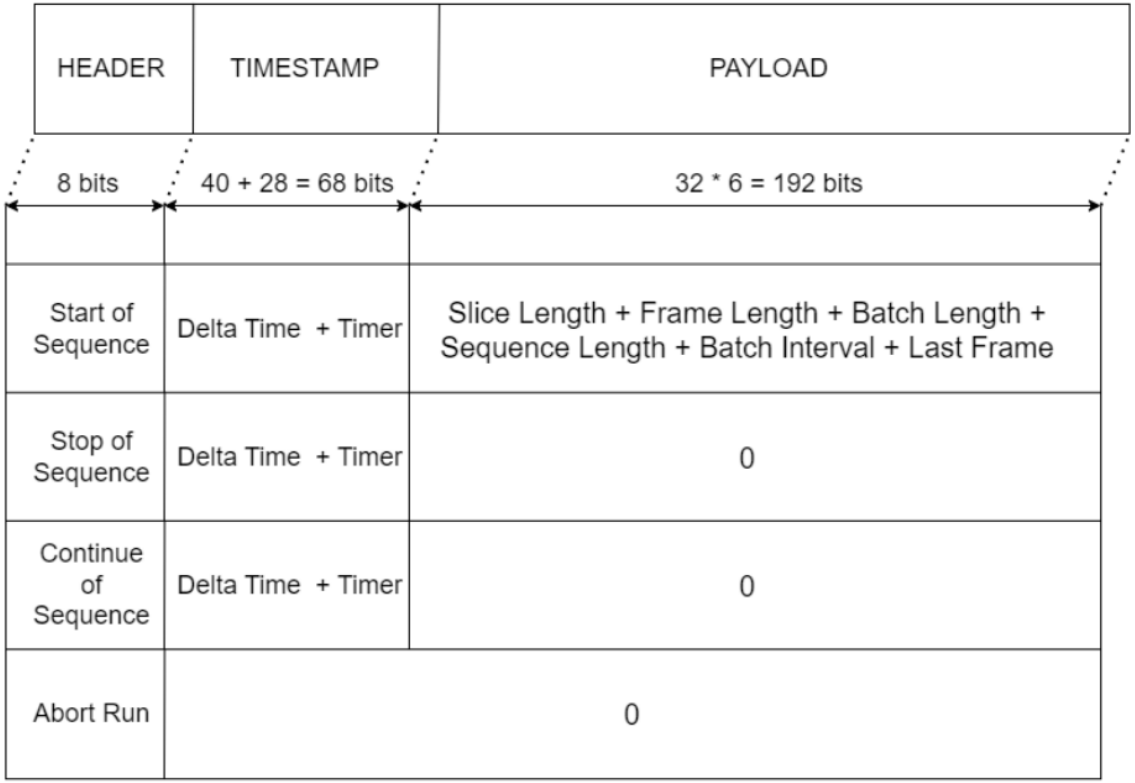


TSS v2 Features

1. Added support for 2 new commands:
   - Continue Sequence
   - Abort Sequence
2. Added Serial Interface for transfer of Current frame number
   - UART as an output from TSS Node to L1 instead of Parallel.

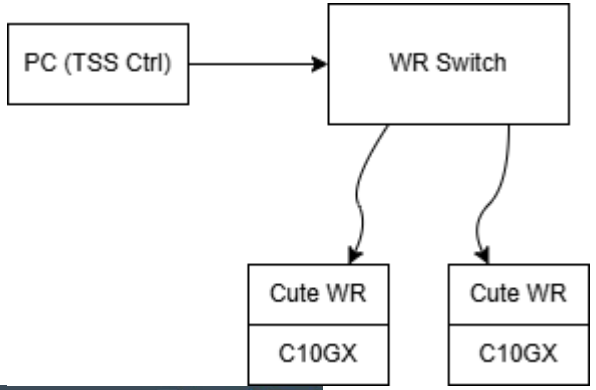


TSS Controller Command Format

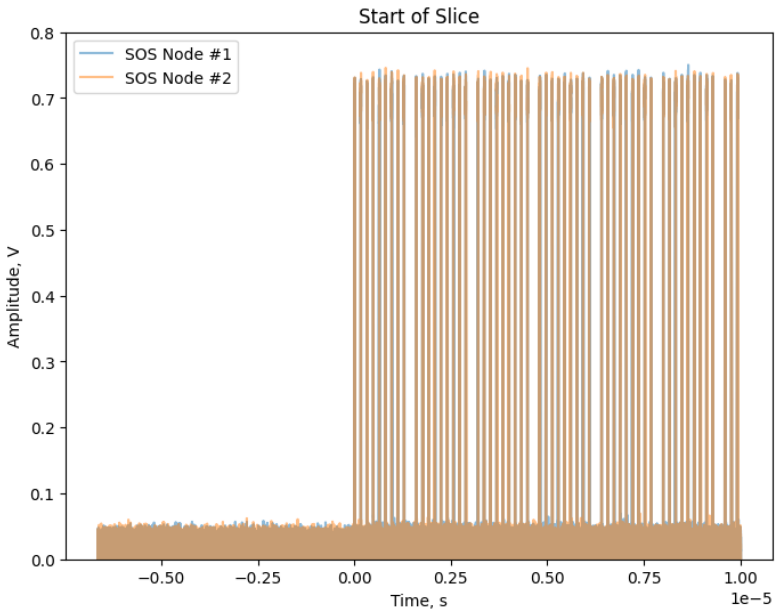


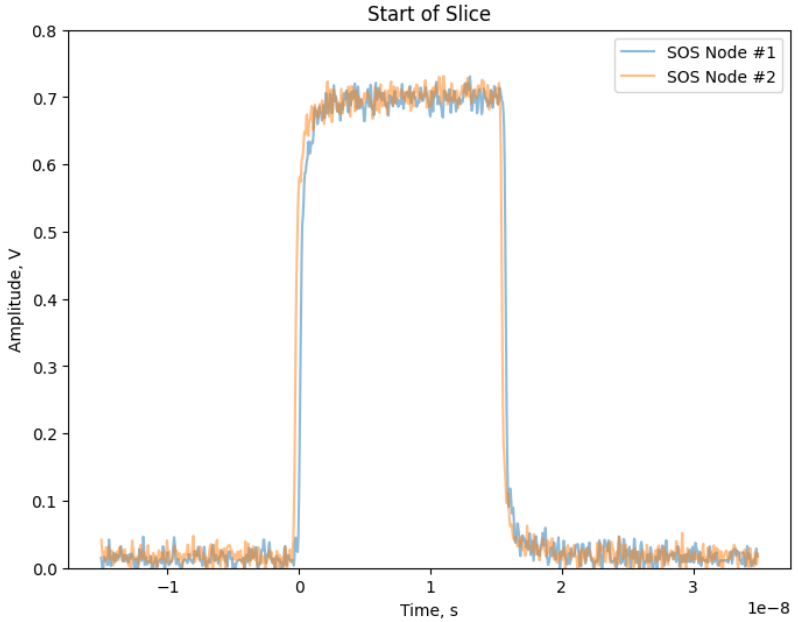
First Test Runs

- TSS Nodes were running on Cyclone 10 GX FPGA connected to White Rabbit Nodes from SyncTechnology in cascade mode to transfer network data via SFP and via FMC to transfer synchronization data.
- WR Nodes were connected to WR Switch by SyncTechnology.
- All WR devices were previously synchronized
- PC as a TSS controller is connected to the same WR Network



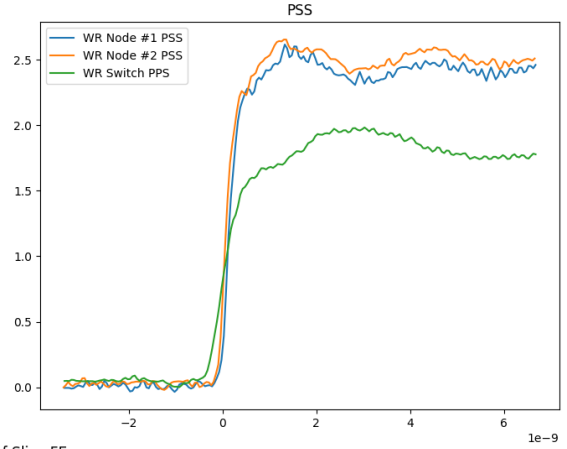
Test Results

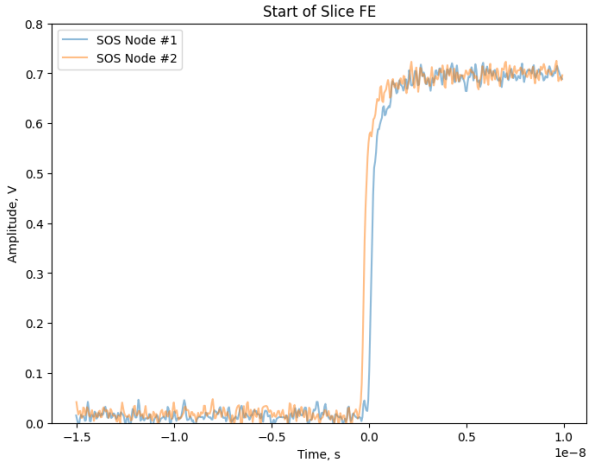




More Test Results

- Measured PPS and Start of Slice (synchronous command).
- Average PPS Delay – 16 ps;
- PPS Jitter – 13 ps;
- Average SoS impulse length – 15.8 ns;
- Average SoS Delay – 279 ps;
- St Deviation of SoS Delay – 190 ps.





Planned work

In next version of TSS we plan to add new functions:

- Diagnostics of possible errors when generating synchronous commands:
  - Lost connection to TSS Controller;
  - Incorrect generation of schedule by TSS controller;
  - Desynchronization between TSS node and WR Master clock;
- Porting TSS controller and node to other hardware platforms (PangoMicro, Xilinx)

iW-RainboW-G30D

- Zynq UltraScale+ FPGA

ALINX AXP390

- Pango Titan2 FPGA