ZOOM

04.12.2024

Дубна

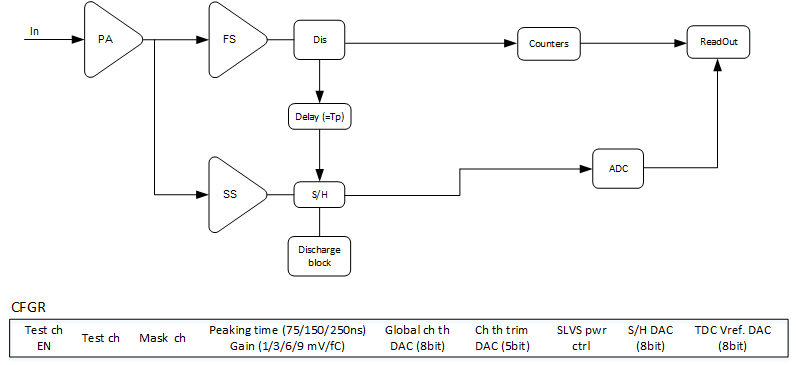
Разработка ИС для straw and micromegas детекторов NICA-SPD

Солин Александр , НИИ ЯП БГУ, Минск

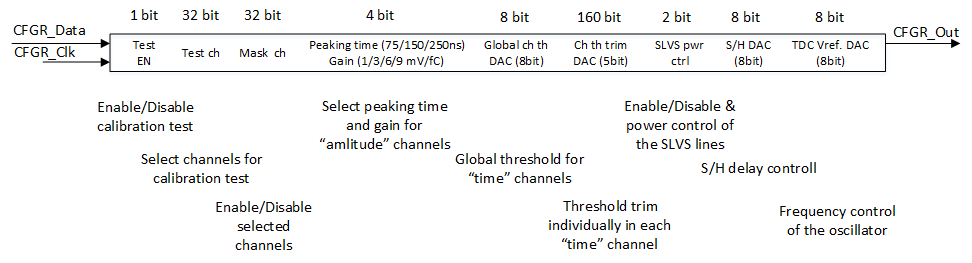
**AST-SPD main specification**

|  |  |
| --- | --- |
| Detector parameters | |
| Negative input charge, fC | 1000 |
| Detector channel capacitance, pF | 20÷100 |
| Loading per channel, kHz | up to 200 |
| Working mode | triggerless |
| Common chip parameters | |
| Technology | CMOS, 180 nm |
| Number of channels | 32 |
| Supply voltage, V | 1.8 |
| Power dissipation, mW/ch | 10 |
| Fast shaper, time channel | |
| Shaping time, ns | 6÷10 |
| Time channel resolution, ns | 1 |
| ENC (r.m.s.), e @ Cd=60pF | <1000 |
| Slow shaper, amplitude channel | |
| Shaping time, ns | 75/150/250 |
| Shaper order | 4 |
| Gain, mV/fC | 1/3/6/9 |
| ENC (r.m.s.), e @ Cd=60pF | <1000 |
| ADC, bit | 10 |

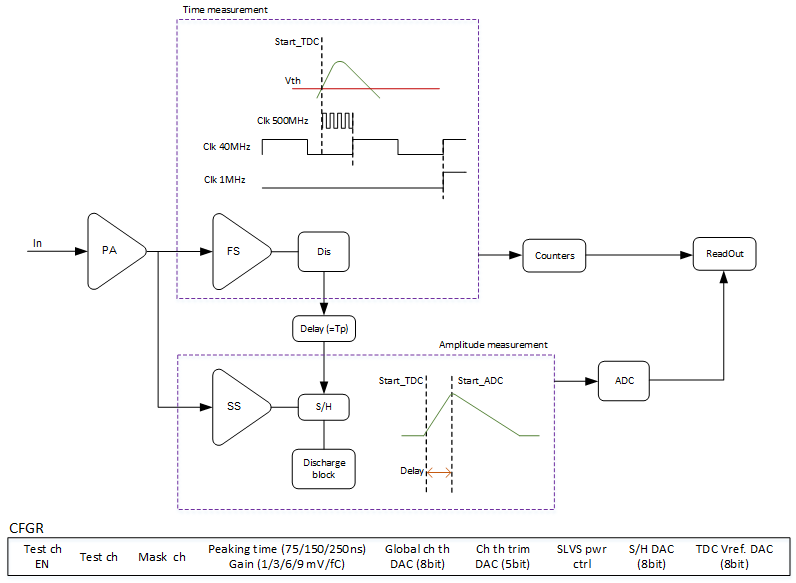
**APD-SPD channel architecture**



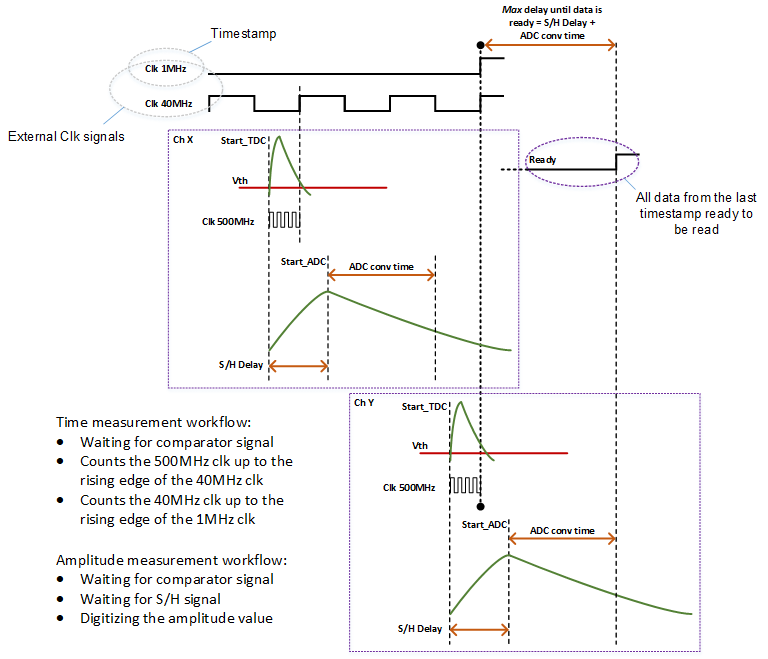
**Configuration register**



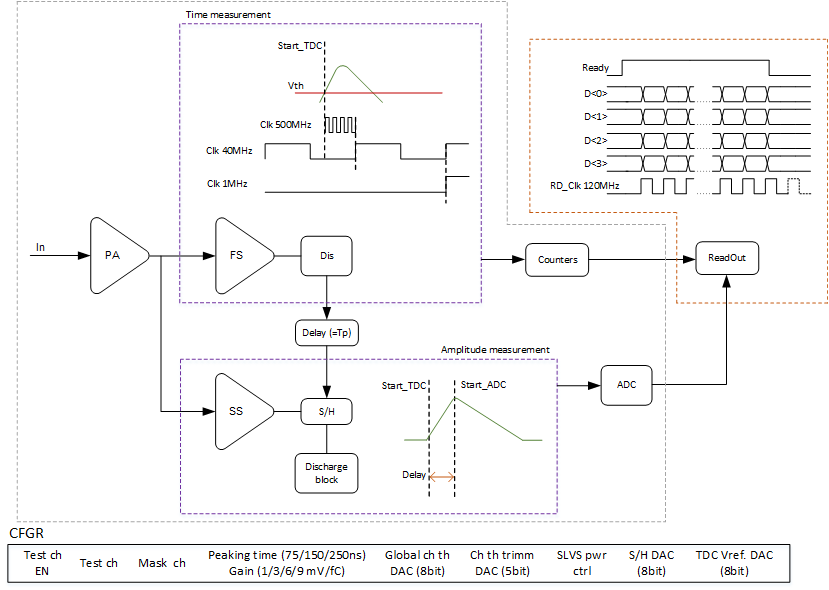
**TDC @ ADC**



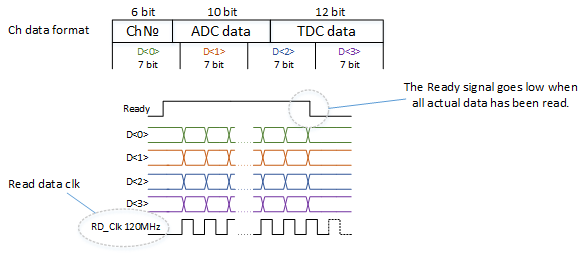
**TDC @ ADC details**



**TDC @ ADC readout**



**AST-SPD data format**



**Pin Assignment/Function**

|  |  |  |
| --- | --- | --- |
| **Pin name** | **Number of pins** | **Description&Comments** |
| **Analog pins** | | |
| **Inputs** | | |
| In | 32 | Analog input, ESD |
| **Test channel** | | |
| In\_test | 1 | Test input, ESD |
| Out\_fs | 2 | Differential output of fast shaper |
| Out\_ss | 2 | Differential output of slow shaper |
| Out\_S/H | 2 | Differential output of S/H |
| **Calibration** | | |
| vdc\_cal | 1 | Calibration voltage |
| **Digital pins** | | |
| **Reset** | | |
| RS | 1 | Set to default state (reset data register, current trigger states), 1.8V CMOS |
| **Configuration register** | | |
| CFGR\_Data | 1 | Configuration register input, 1.8V CMOS |
| CFGR\_Out | 1 | Configuration register output, 1.8V CMOS |
| CFGR\_Clk | 1 | Configuration Register clock, 1.8V CMOS |
| CFGR\_Rst | 1 | Configuration register reset, 1.8V CMOS |
| **Data output** | | |
| Ready | 2 | Data output request, SLVS |
| Data\_Out<1:4> | 8 | Data output, four buses, SLVS |
| **External clock signals** | | |
| Clk\_1MGz | 2 | Time stamp, SLVS |
| Clk\_40MGz | 2 | TDC counter, SLVS |
|  | | |
|  | | |
| **Pin Assignment/Function** | | |
| **Pin name** | **Number of pins** | **Description&Comments** |
| RD\_Clk | 2 | Read data, SLVS |
| **OR circuit** | | |
| OR | 2 | OR output, SLVS |
| **Calibration** | | |
| tinj | 2 | Charge injection into selected channels, SLVS |
| **Analog power supplies** | | |
| VDD1, VSS1 | 12 | Power and ground CSP, FS, SS, six through buses |
| VDD2, VSS2 | 8 | Power and ground Dis, four through buses |
| VDD3, VSS3 | 8 | Power and ground S/H, ADC, four through buses |
| VRP | 2 | ADC reference voltage, 1.4 V, two through bus |
| VCM | 2 | ADC reference voltage, 0.9 V, two through bus |
| VRN | 2 | ADC reference voltage, 0.4 V, two through bus |
| **Digital power supplies** | | |
| VDD4, VSS4 | 8 | Power supply for digital part, four through buses |
| VDD5, VSS5 | 8 | Power supply for SLVS receivers and transmitters, four through buses |
| VDD6, VSS6 | 8 | ESD power supply, four through buses |
| VOSC | 2 | TDC reference voltage, (0.9÷1.6) V, through bus |
| Total | 123 |  |

**Configuration register**

|  |  |
| --- | --- |
| **Description&Comments** | **Number of bits** |
| **Global bits (defaults are 0)** |  |
| Shaping time: 75, 150, 250 ns | 2 |
| Gain: 1, 3, 6, 9 mV/fC | 2 |
| Channels threshold DAC | 8 |
| S/H DAC | 8 |
| TDC reference voltage DAC | 8 |
| SLVS power control | 2 |
| **Channel bits (defaults are 0)** |  |
| Channel threshold trimming DAC | 5 |
| Channels calibration | 32 |
| Channels mask | 32 |
| Test channel enable | 1 |

**Прототип**

Статус работ: контракт на изготовление первого прототипа чипа AST-SPD заключен

Планируемый срок поставки: 31.08.2025

AST-SPD-8\_v1rev01 specification

|  |  |
| --- | --- |
| **Detector parameters** | |
| Negative input charge, fC | 2000 |
| Detector channel capacitance, pF | 20÷100 |
| Detector occupancy, kHz | up to 200 |
| Working mode | triggerless |
| **Common chip parameters** | |
| Technology | CMOS, 180 nm |
| Number of channels | 8 |
| Supply voltage, V | 1.8 |
| Power dissipation, mW/ch | 10 |
| Channel optimization criteria:  1) Maximum occupancy  2) Minimum dead time  3) Power dissipation  4) Chip area | |  |  |  |  | | --- | --- | --- | --- | | **CSP** | **FS** | **Dis** | **TDC** | | **SS** | | **SAR ADC** |   TDC per time channel  SAR ADC per amplitude channel |
| Additional functions | OR output  Individual channels testing  Noisy channels masking |
|  |  |
| Data output | Serial channel, 120 MHz  (option: 4 parallel channels,120 MHz) |
| Digital signals | sLVDS |
| Control | Configuration register |
| Test channel | Shape and gain control of analog signals: differential outputs of fast and slow shapers  Discriminator test: differential outputs |
| **Fast shaper, time channel** | |
| Shaping time, ns | 6÷10 |
| Time resolution, ns | 1 |
| ENC (r.m.s.), e @ Cd=60pF | <1000 |
| **Slow shaper, amplitude channel** | |
| Shaping time, ns | 75/150/250 |
| Shaper order | 4 |
| Gain, mV/fC | 1/3/6/9 |
| ENC (r.m.s.), e @ Cd=60pF | <1000 |
| ADC, bit | 10 |
| Time conversion, ns | 100 |

**Рабочий план**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Этапы разработки | Сервис | Сроки | | Число  каналов | Количество  микросхем |
| **2024-2025** | | | | | |
| Первая итерация  AST-SPD-8\_v1rev01 | MPW | 01.12.2024 | 31.08.2025 | 8 | до 5 |
| Тестирование |  | 01.09.2025 | 30.11. 2025 |  |  |
| **2025-2026** | | | | | |
| Вторая итерация | MPW или MLM (по результатам первой итерации) | 01.12.2025 | 30.06.2026 | MPW:8  MLM: 32 | до 5  MLM: 1500 и более |
| Тестирование |  | 01.07.2026 | 31.10.2026 |  |  |
| **2026-2027** | | | | | |
| Установочная партия | MLM | 01.11.2026 | 31.03.2027 | 32 | 1500 и более |