Preparing for testing the active HGND module in the upcoming run.

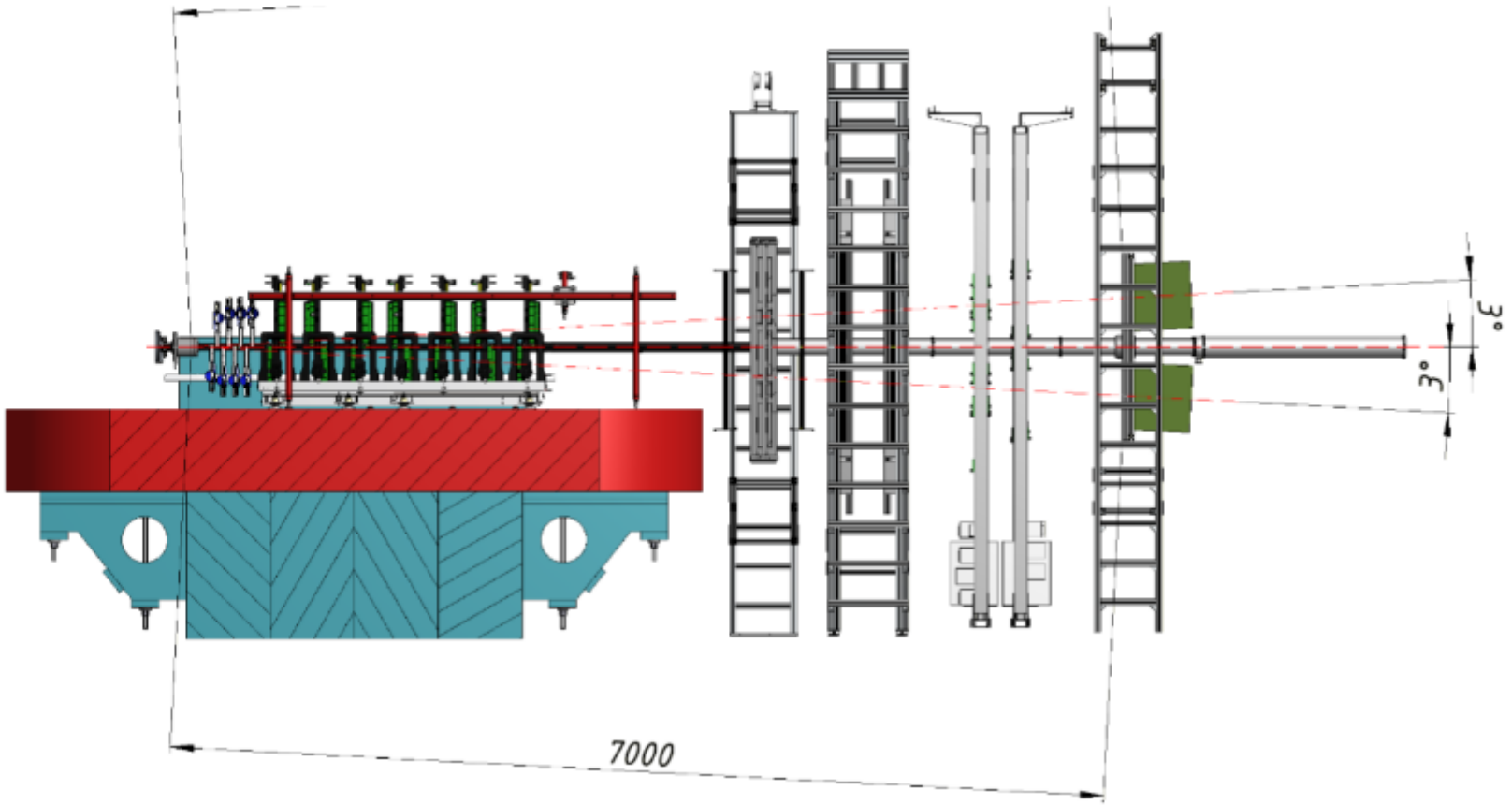
D. Finogeev, F. Guber, A. Izvetnyy, A. Makhnev S. Musin, D. Serebryakov
INR RAS, Moscow

Outline

- Updates on the FPGA design
- Updates on the software design
- The support structure assembling
- Status of the HW development
- Status and plans for the HGND prototype tests at INR
- HGND prototype setup at BM@N and integration tests

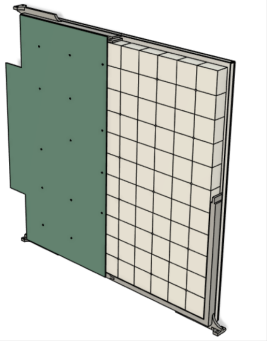
Detector arrangement

- Detector for high-energy neutron flow measurement
- ToF method with T0 as the “start” signal source
- 7m measurement distance
- Detector is split into 2 “blocks” for improved acceptance

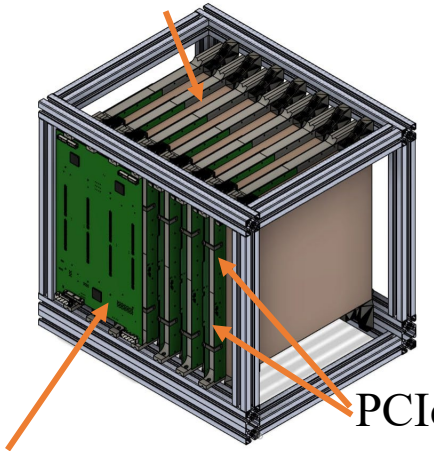


FEE & readout architecture

- 16 layers with scintillation matrix 11X11
- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total

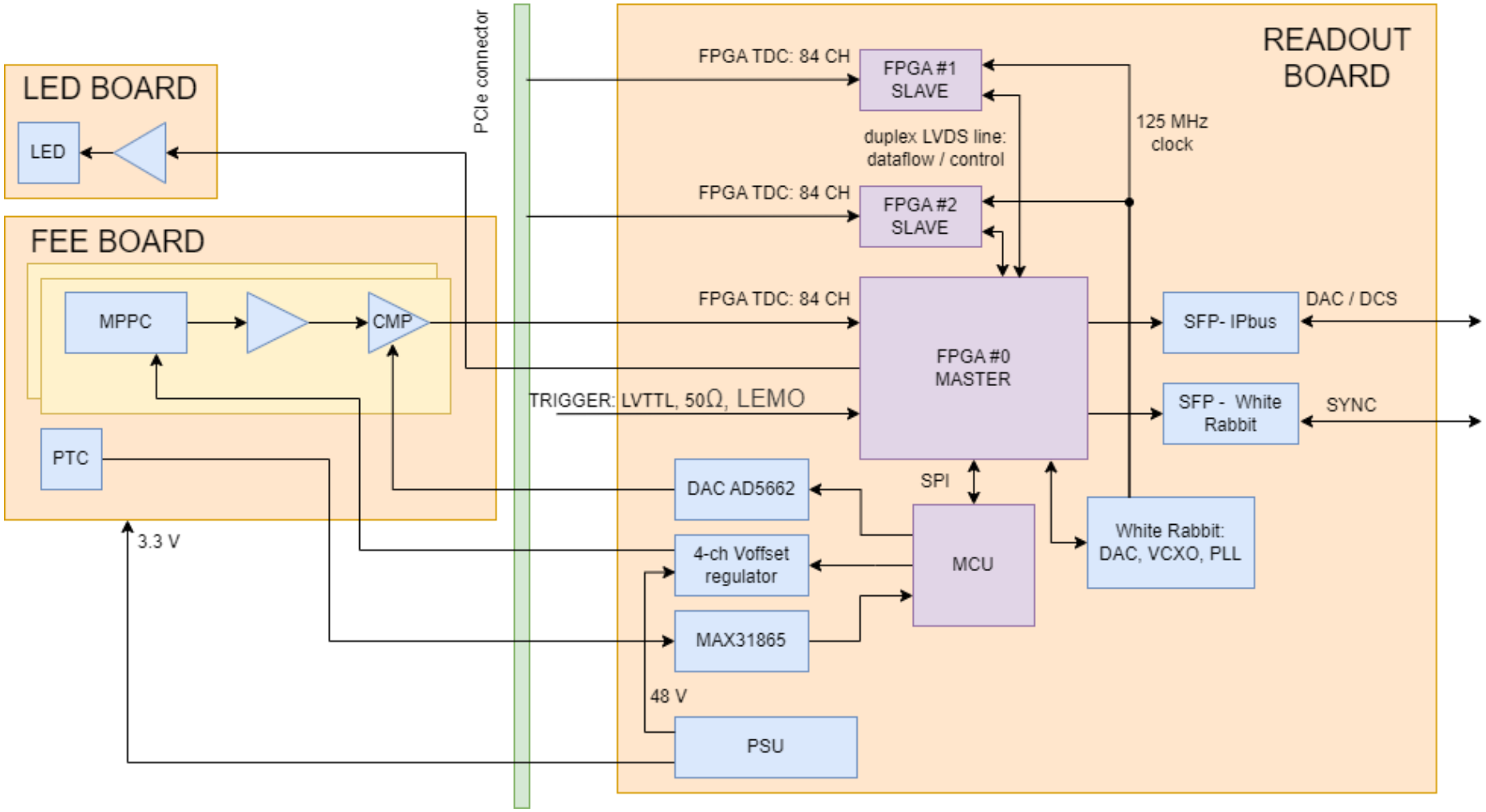


FEE board



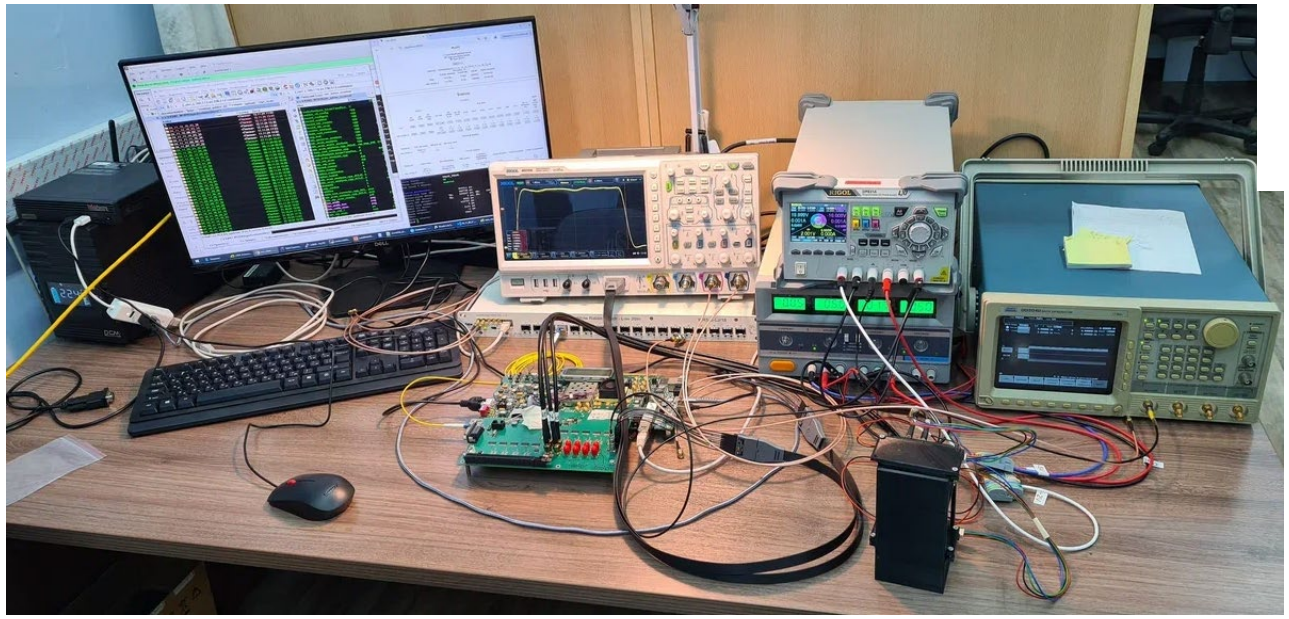
PCIe

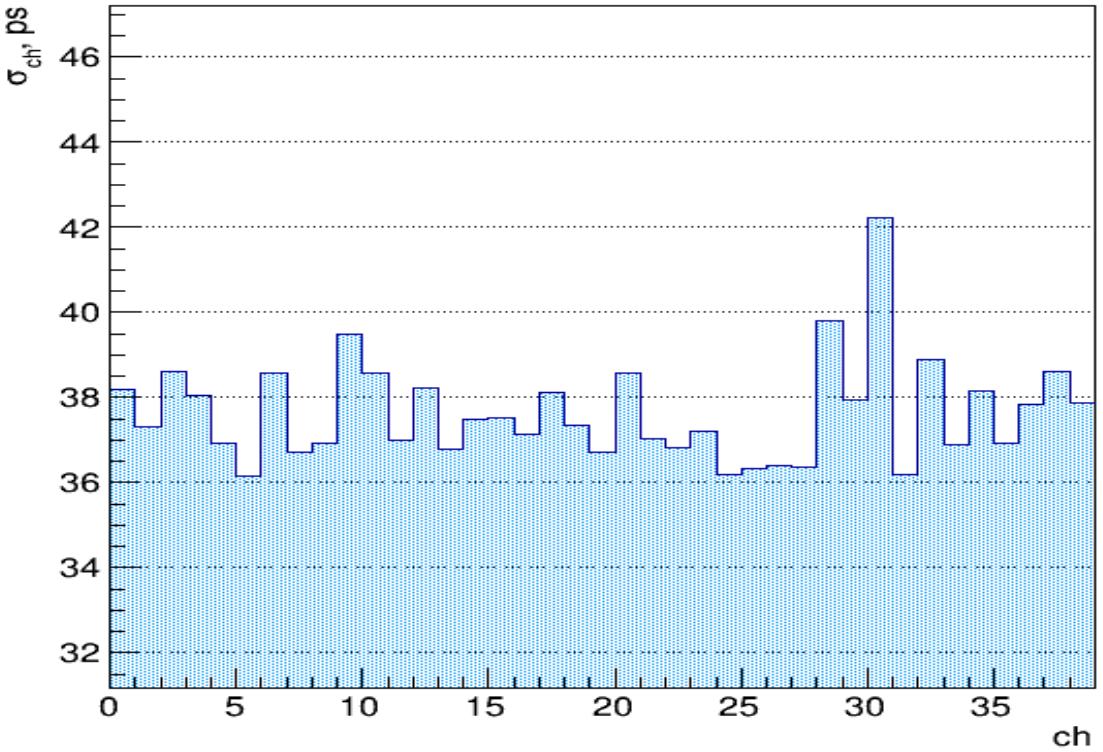
Readout board



Status of the FPGA&TDC design

- New version of TDC_v2 fabric calculation was developed: much easier, less requirements to FPGA resources. Tested on real data in software and on the VHDL simulation.
- The sequential TDC calibration was tested in software – not works, seems the calibration is NP-complete task.
- The full set delays enumeration TDC calibration was implemented in software and VHDL (TDC_v2).
- New pulse generator was implemented in FPGA for LED&LB: pulses in range from 2 ns to 8.16 us with step 13 ps
- FPGA project was optimized and cleaned up; timing constrains fixed.



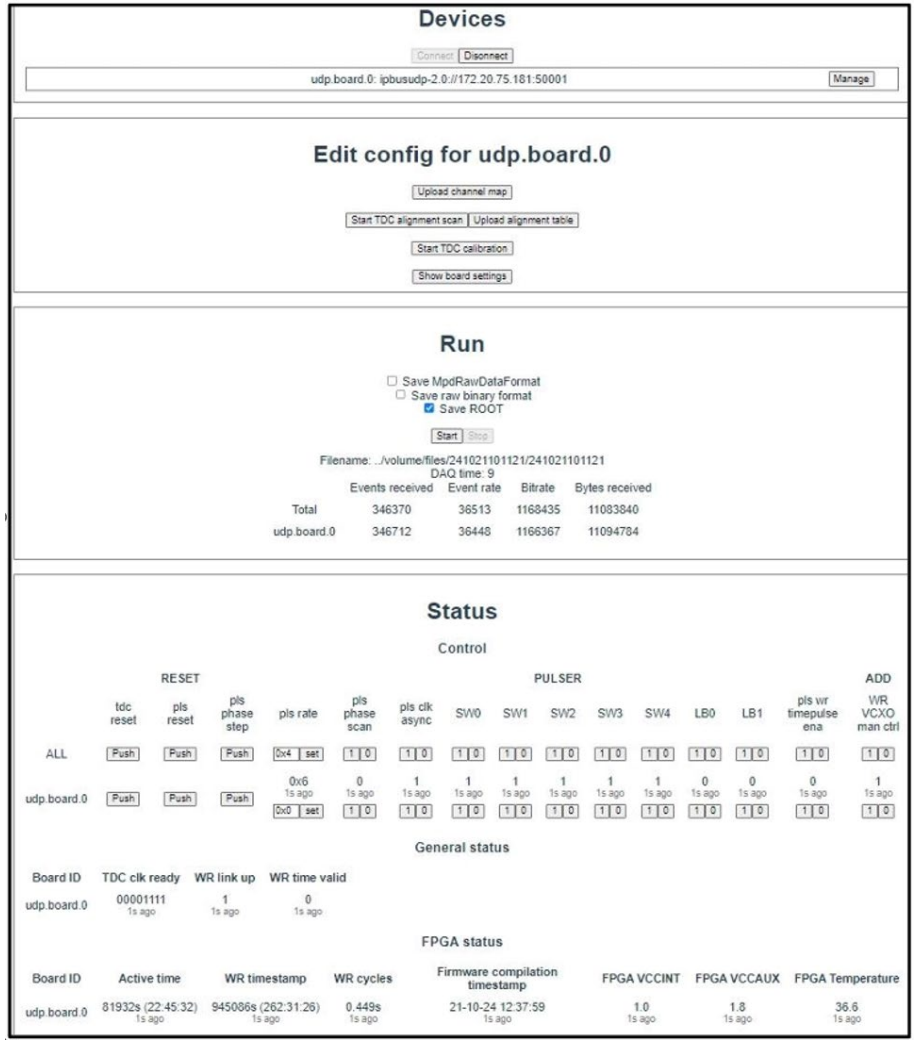


The TDC channel precision. Measured with the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).

The accurate TDC precision measurements:

- Pulses are asynchronous to TDC clock.
- Pulses length is various 9.8 .. 10.3 ns with step 50ps
- Source pulses jitter is 5ps

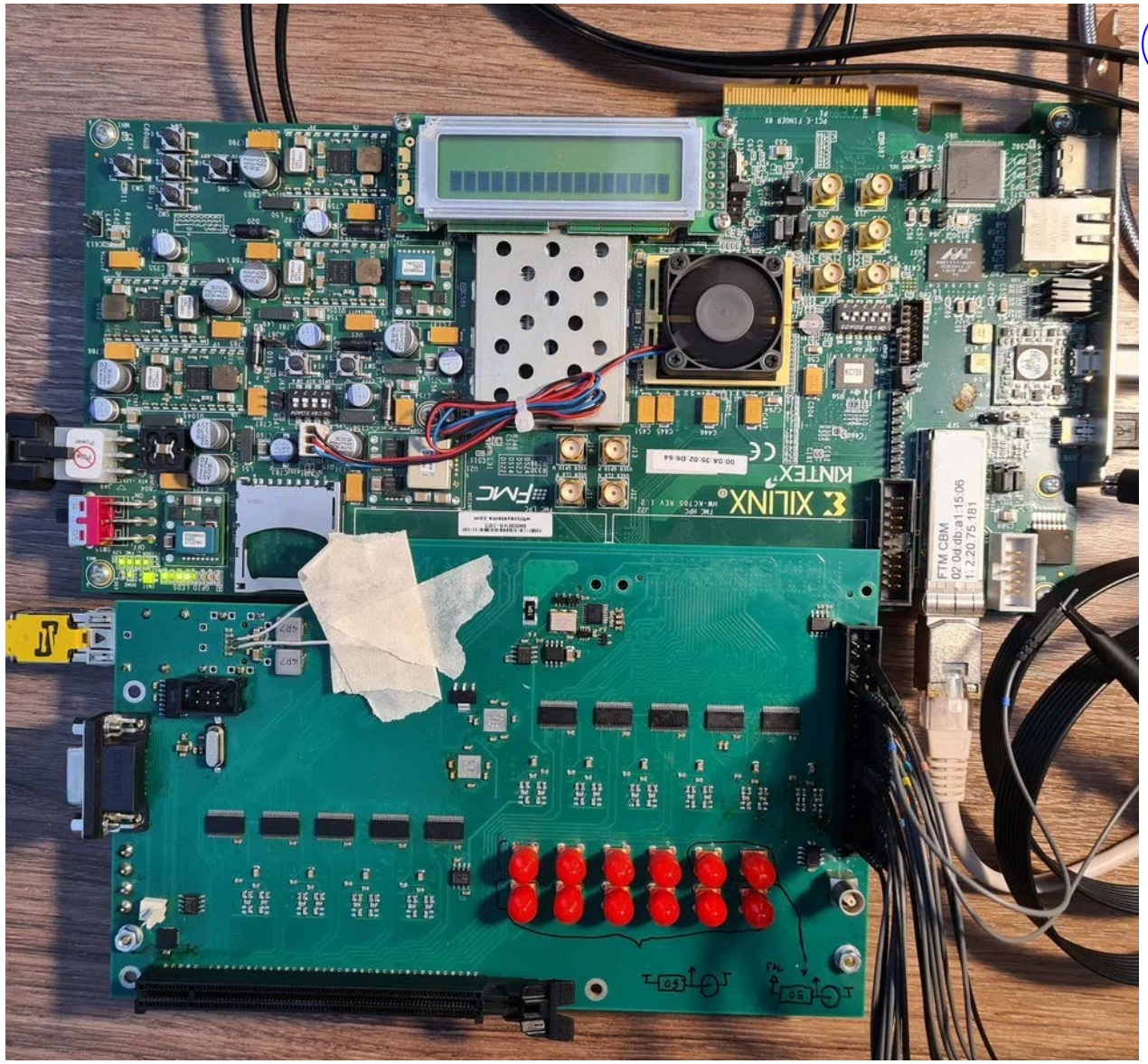
Server development status and preparation for integration into BM@N

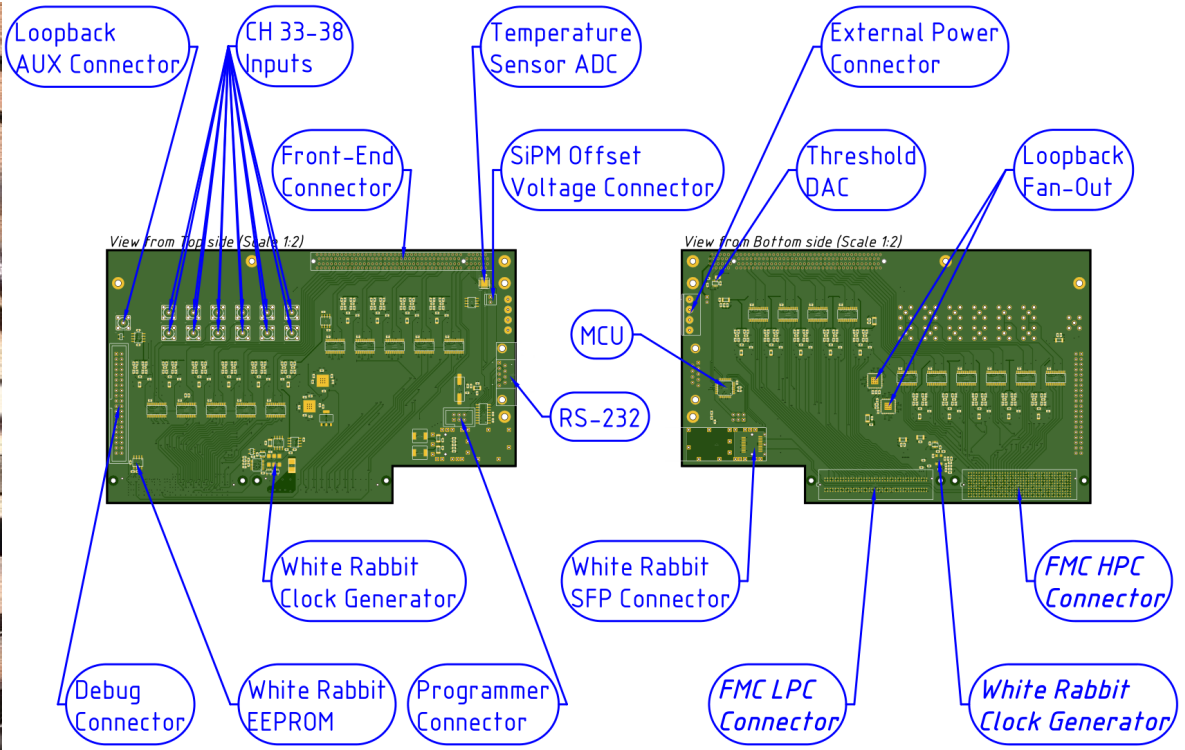


- Implemented FPGA control from the server graphical interface.
- Tested server fault tolerance during long-term data acquisition (from 3 days without intervention).
- Primary data processing and QA from the interface.
- Up to 500 Mbps when testing with 1 board; Up to 800 Mbps when testing with 2 boards.
- Online event sorting and data publishing via TCP: 2.6 MHz event rate with a trigger frequency of 10 kHz (local loopback).
- The server is ready for testing control from DCS BM@N with real equipment and recording data from space.
- Working on:
  - **<u>Multiple input trigger logic implementation</u>**

HGND readout v2 prototype (39 channels)

based on the Kintex 7 evaluation board (KC705)



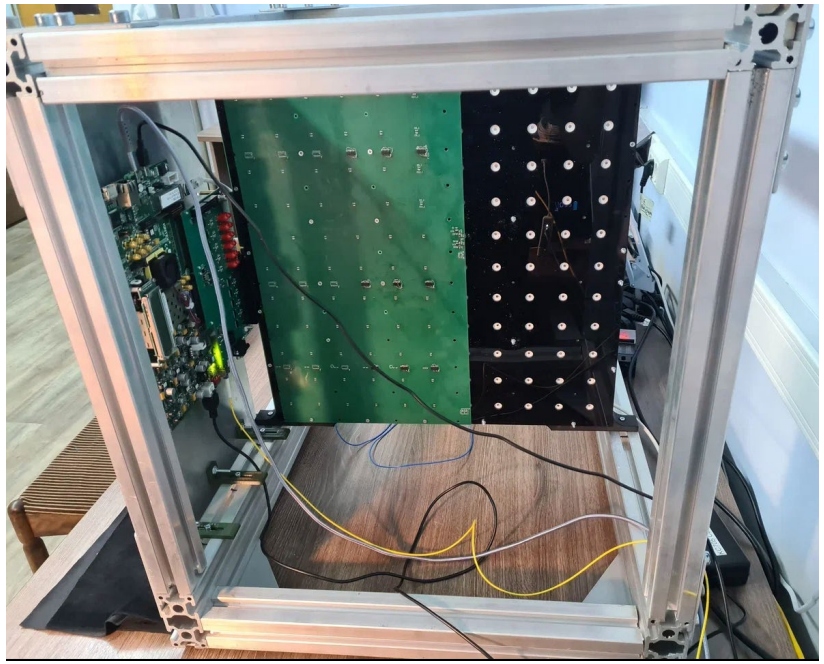


- Addon for Kintex 7 evaluation board
- 33 PCIe + 6 SMA TDC channels
- Ethernet readout
- White Rabbit synchronization
- FPGA loopback for TDC calibration
- Readout board functionality:
  - *PCIe connector for* scintillation matrix*, Temperature sensor, SiPM offset voltage control DAC threshold*

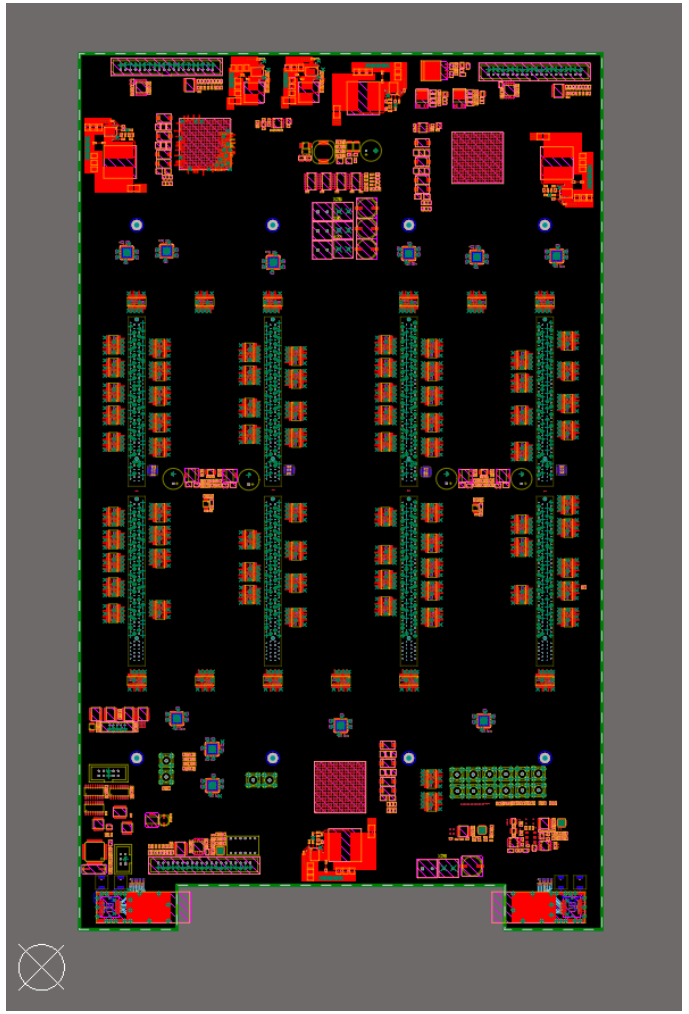
Status of the HW development

The full functional HGND prototype was assembled

- ¼ of matrix SiPM & LED channels
- Ethernet readout
- White Rabbit synchronization
- PCIe connector for scintillation matrix
- Temperature sensor
- SiPM threshold DAC control
- Match HGND geometry

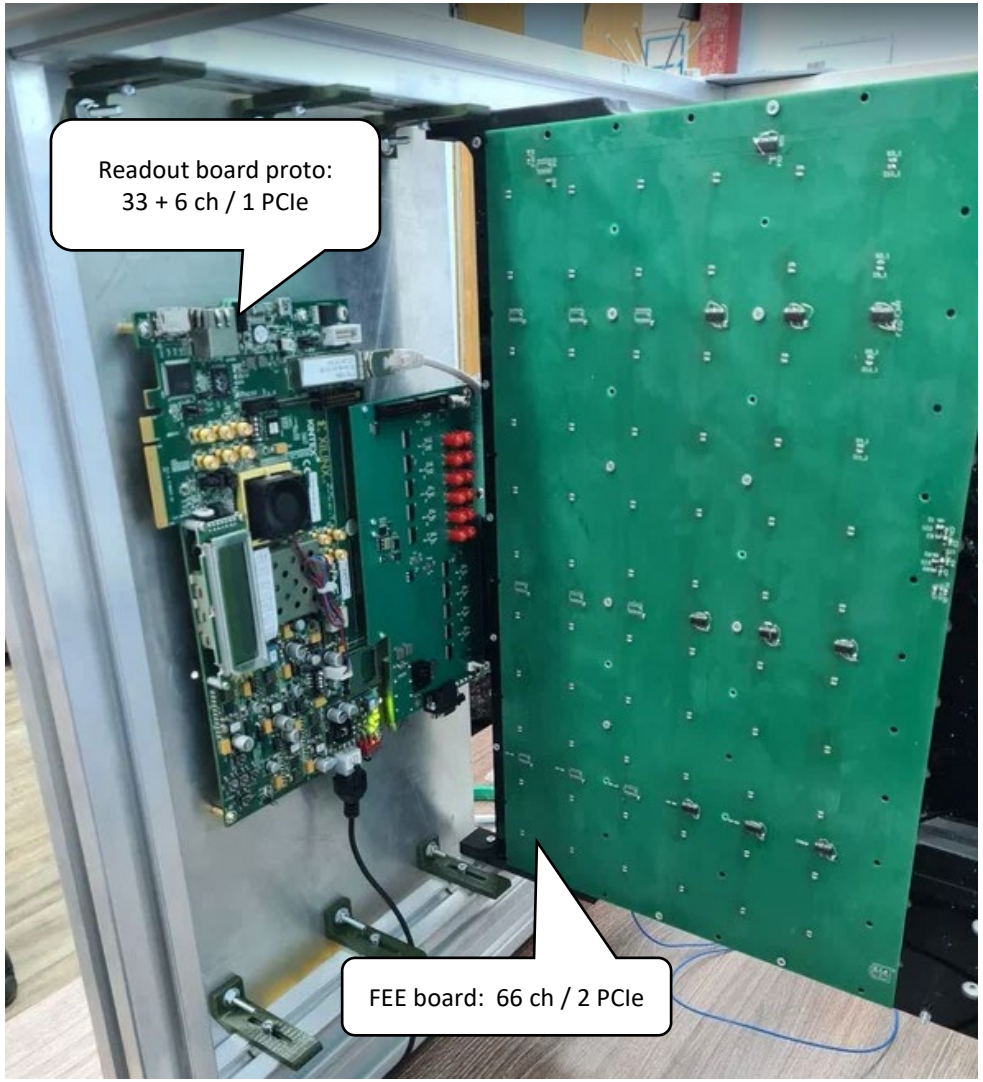


Readout board in under development: layout is finished; design routing

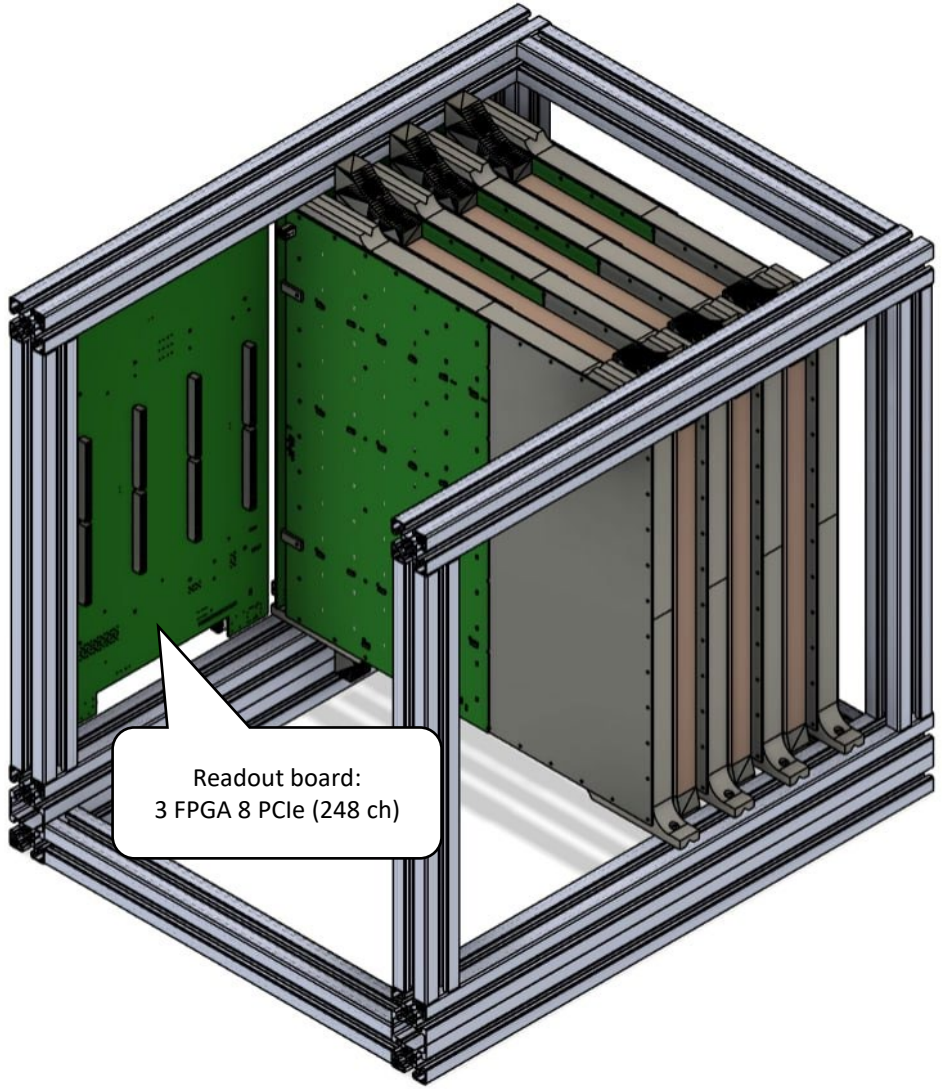


- Two new evaluation boards connected to server
- Two addons manufacturing estimation: end of March

HDND geometry

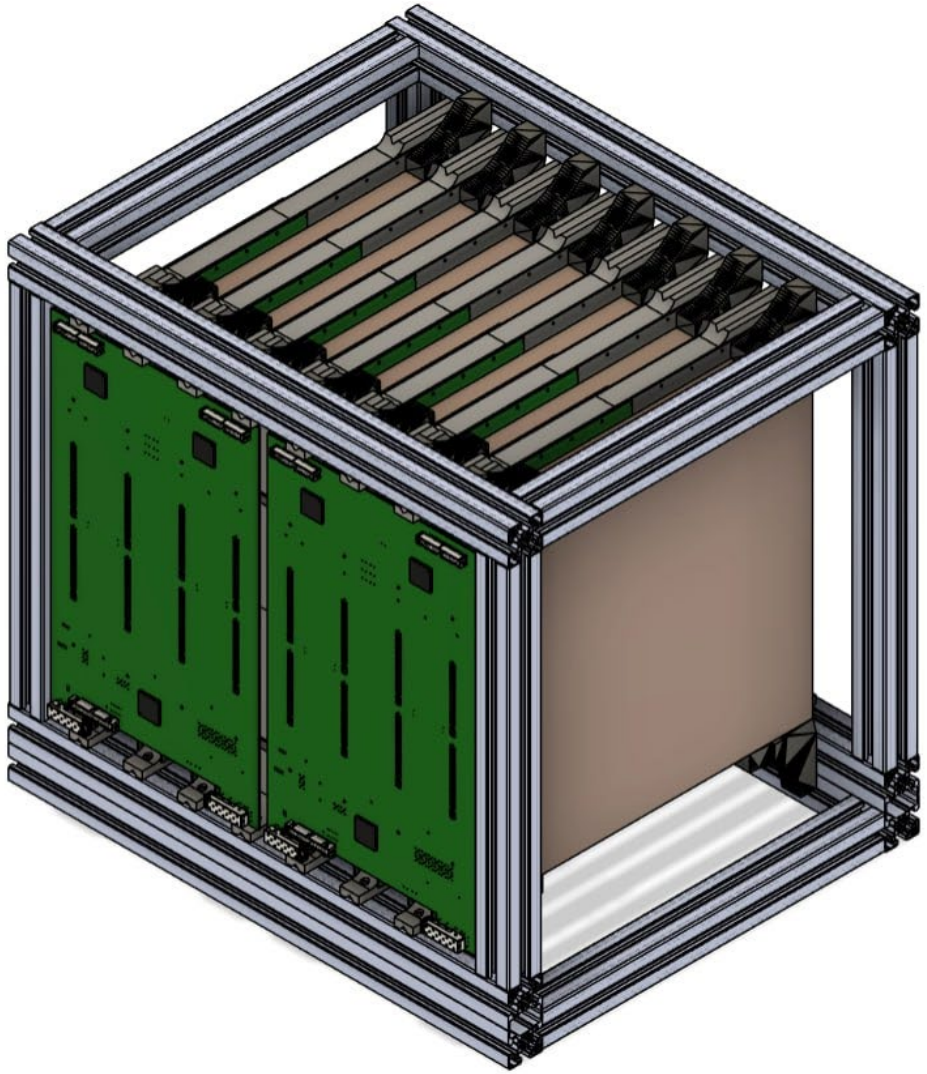


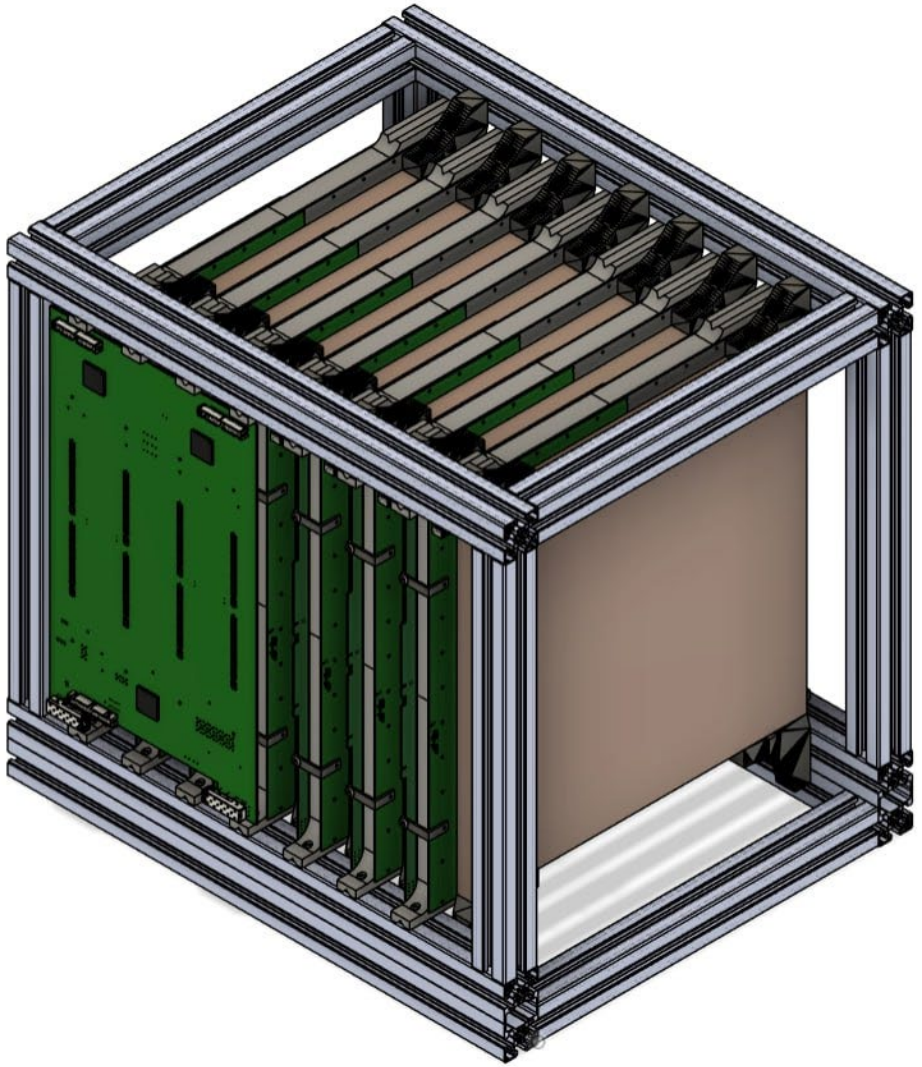
¼ matrix readout prototype



HGND geometry sketch

HDND geometry



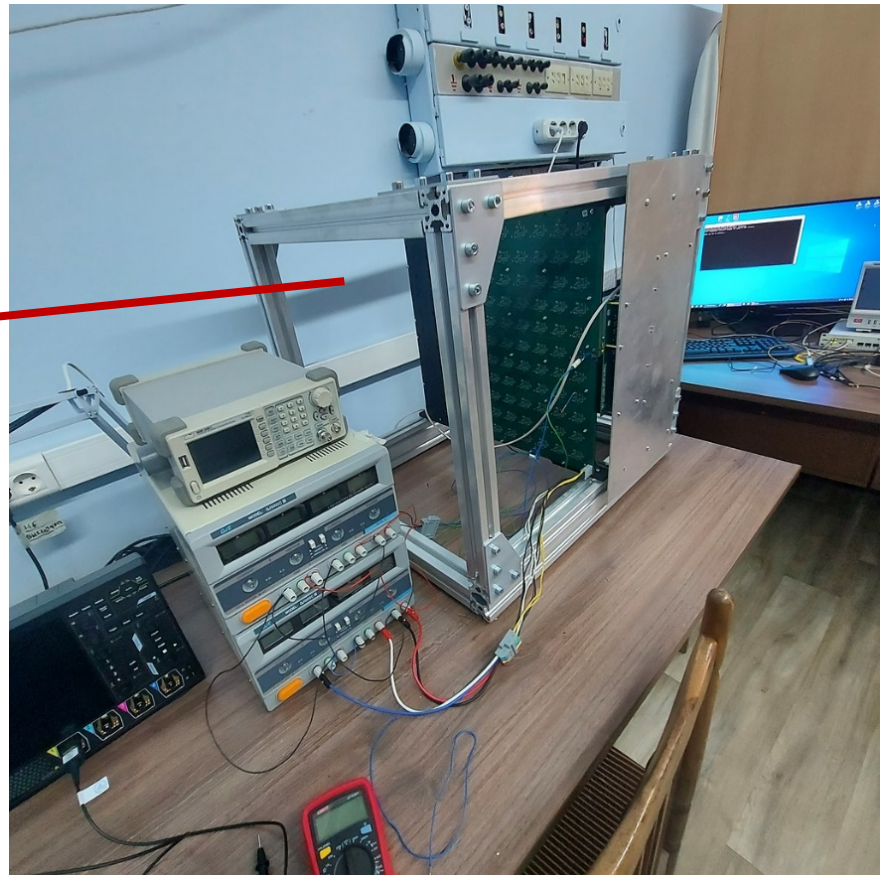


Mechanical support assembly progress

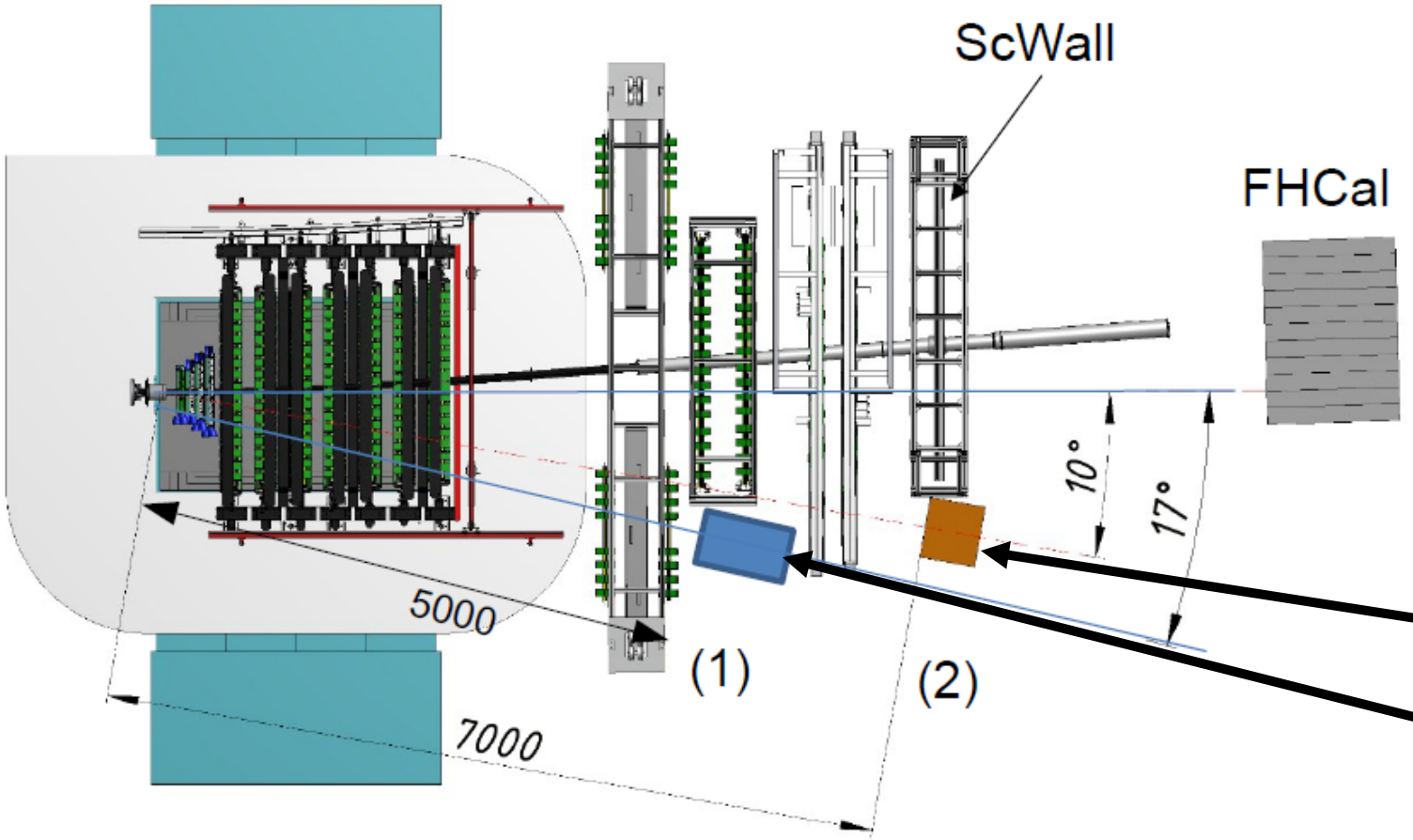
- 2 modules of the neutron detector with copper absorbers are assembled and installedon a movable stand
- Dimensions of the stand: 80x100x300 cm
- Total weight: ~ 1000 kg

Planned HGND assembly with one module at the next session on BM@N

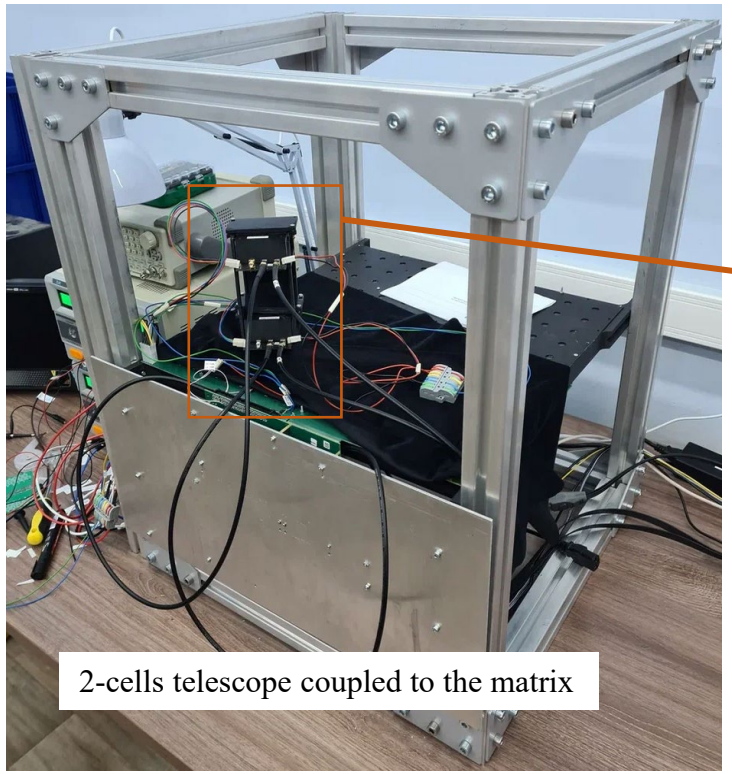
¼ matrix readout prototype (33 ch)

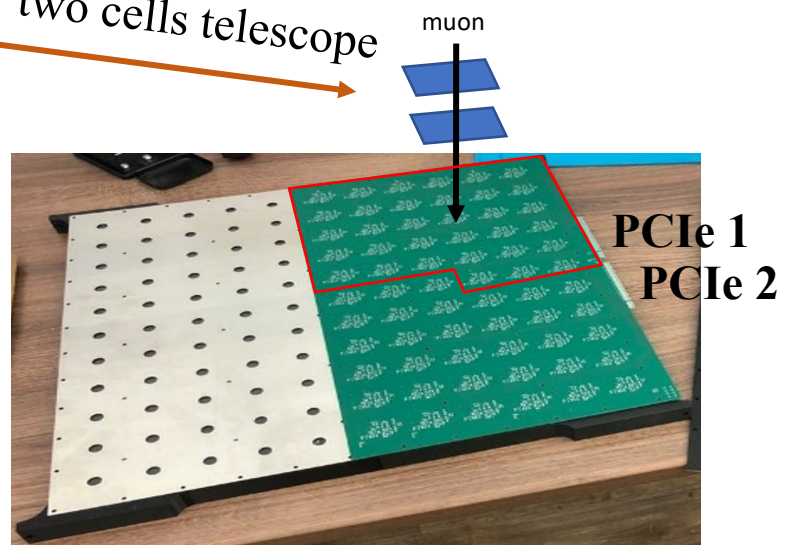


Planned location of the stand with 1 HGND module at the next session on BM@N

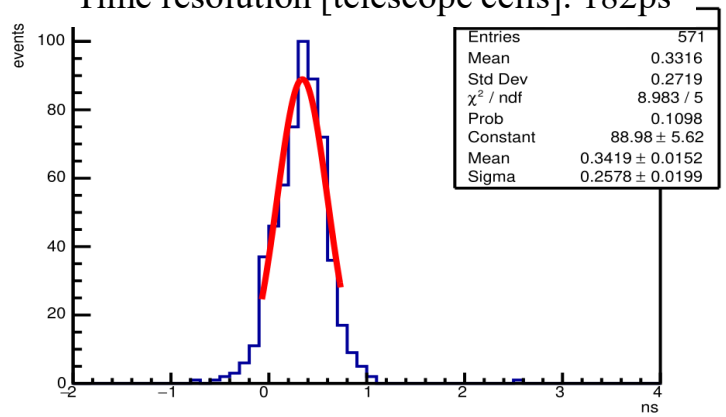


The HGND prototype tests with cosmic muons

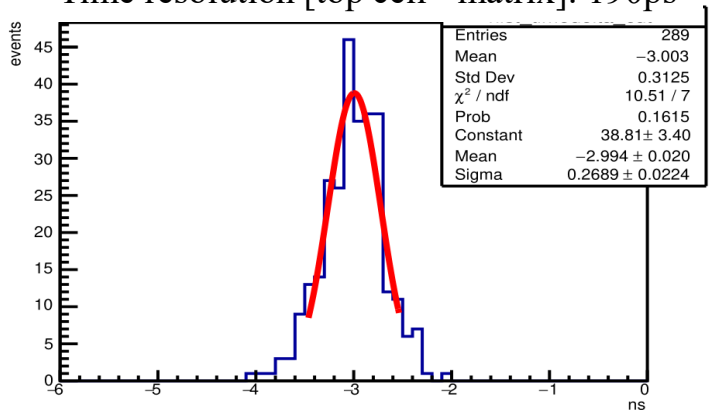




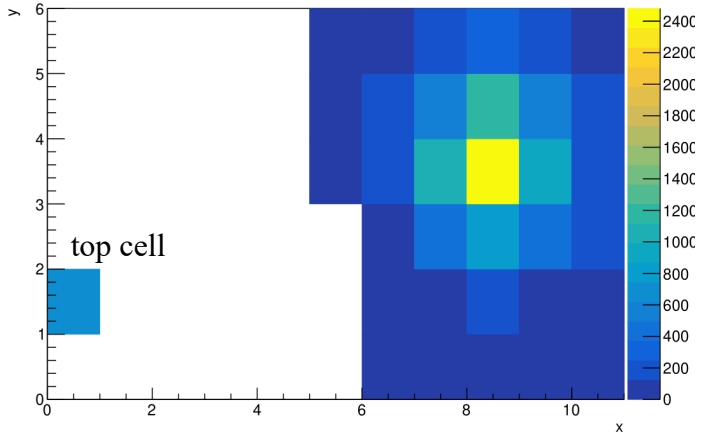
Time resolution [telescope cells]: 182ps



Time resolution [top cell - matrix]: 190ps



The time correlated events: bottom cell – matrix



Cosmic runs was collected in two configuration:

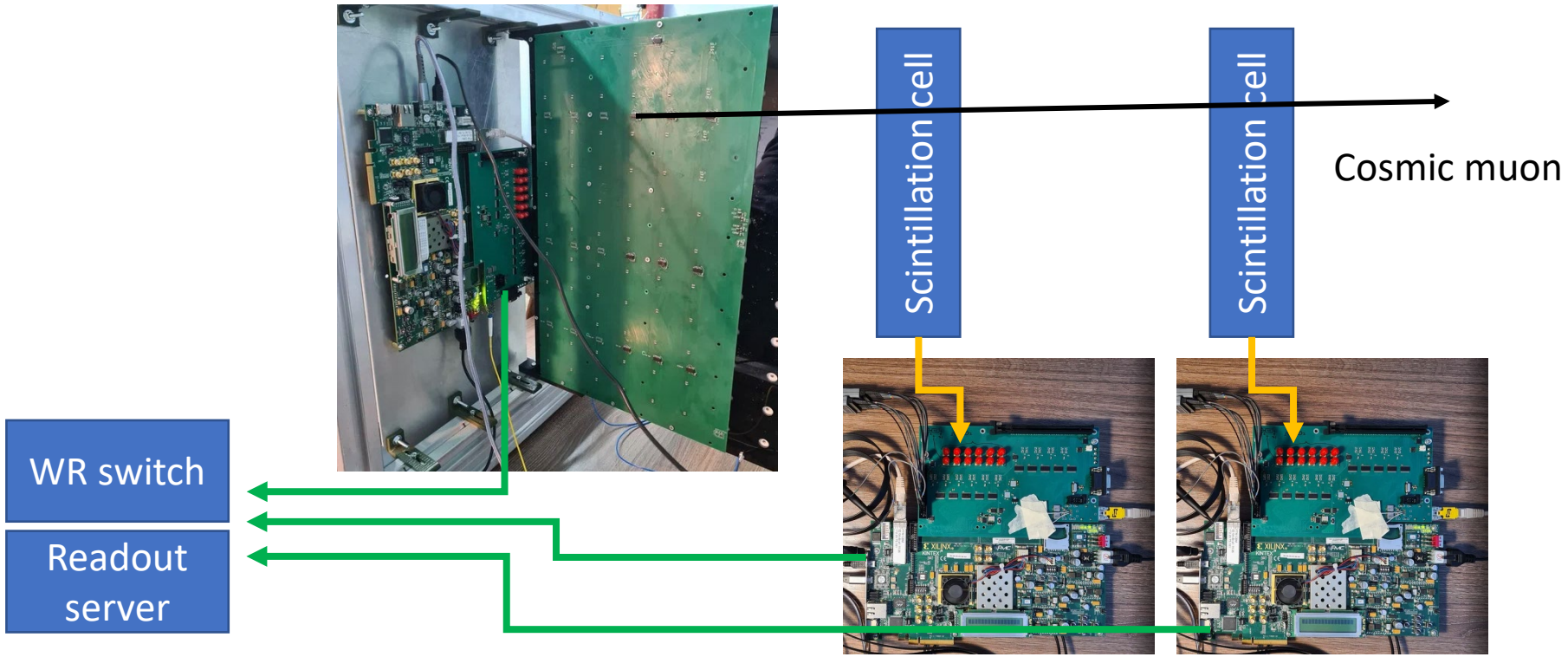
- Normal position (like placement on the BM@N)
- Horizontal position with 2 cells telescope

✓ Results shows the same time resolution between telescope connected via SMA and matrix connected via PCIe: 182 and 190 ps per channel.

➢ Testing all functionality: readout, LED calibration, temperature sensor, geometry, light-isolating

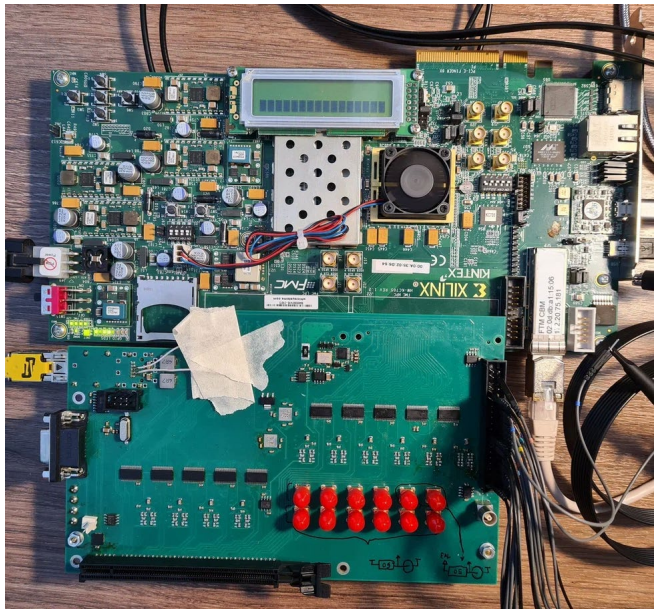
➢ FEE Mass-production

The test of time synchronization and multiple links readout is planned

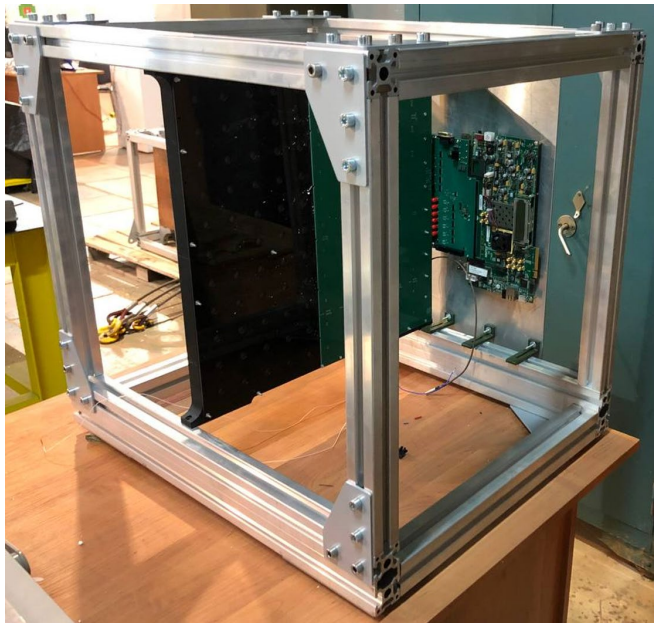


- Three board are connected to WR switch and readout server and detect same cosmic muon track
- Generated events are mixed in for emulation real event rate per link
- Will allow to test:
  - Time synchronization
  - Trigger selection
  - Data acquisition
  - DCS control

Planned setup at BM@N: two steps



HGND Proto assembly



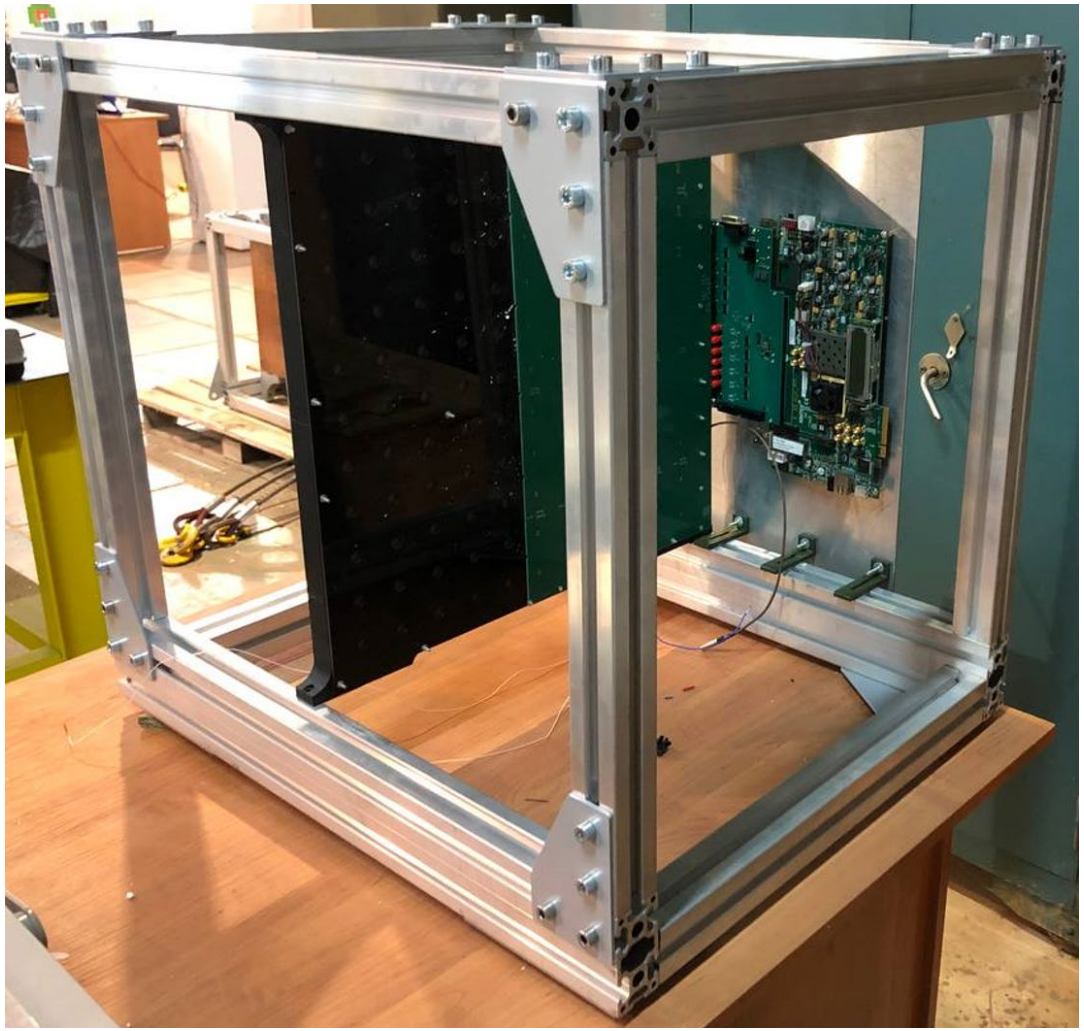
Step 1: the setup allows testing:

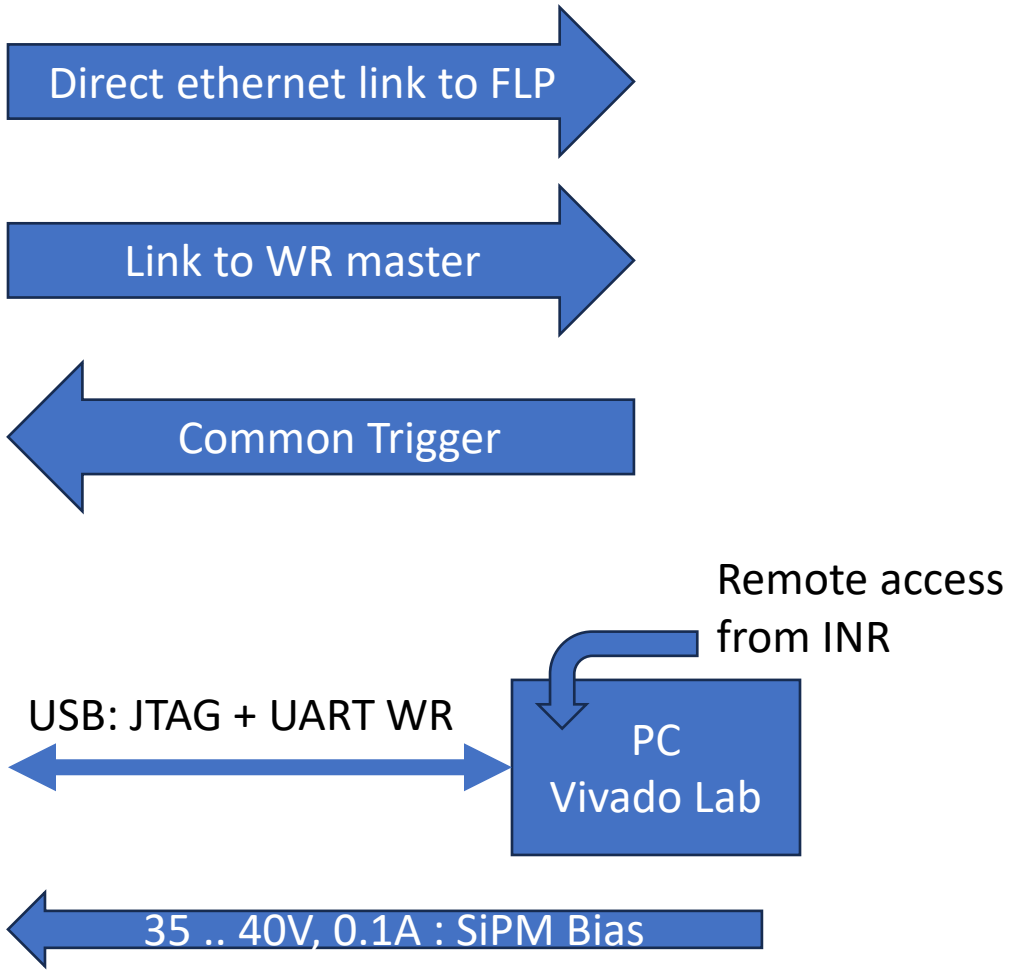
1. HGND control via common DCS
2. Data readout: rate + digitizing
3. White Rabbit events timestamps
4. Trigger selection & synchronization

Step 2: the setup allows testing (additionally) :

1. HGND real time resolution
2. Physics events time correlation
3. FEE behavior in real beam conditions
4. Detector events load

HGND proto setup at BM@N





Conclusions

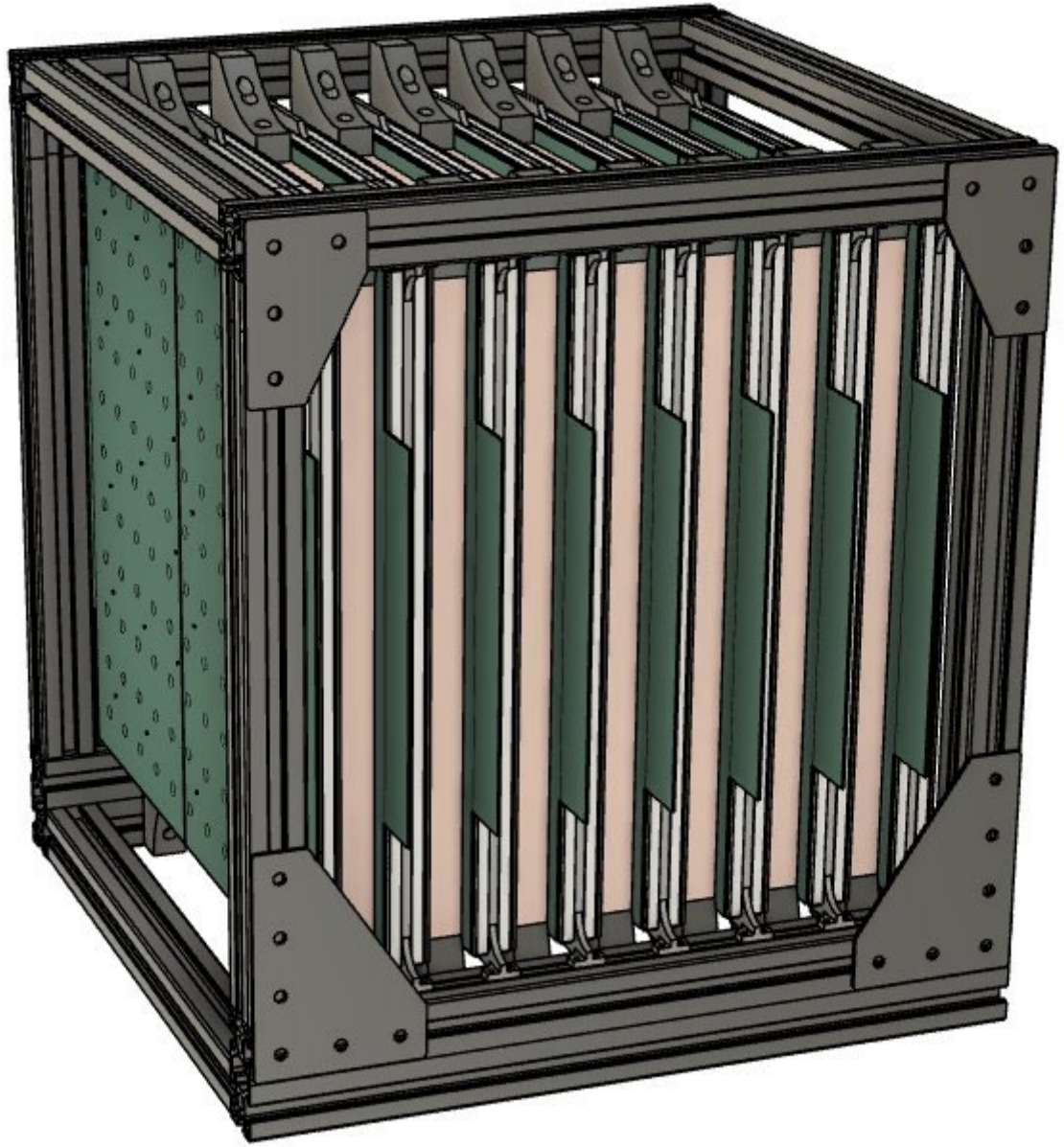
- Status of the HGND readout development:
  - ✓ Good progress on firmware and software
  - ✓ Routing the readout board is in progress
  - ✓ Doing final tests before FEE mass-production
  - ➢ Next steps:
    - multi-boards test
    - Integration prototype into BM@N

Thank you for your attention!

BACKUP

Detector “block”

- Each block consists of:
  - A VETO-layer
  - 8 Cu absorbers
  - 8 sensitive layers
    - 11x11 grid of scintillatiors each
- Assembly is light-tight and air-cooled
- Framing is built with light-weight Al profiles



Readout & trigger

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip (2000 total)
- ***White Rabbit*** (WR) is used for event's time synchronization (8 links total):
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events

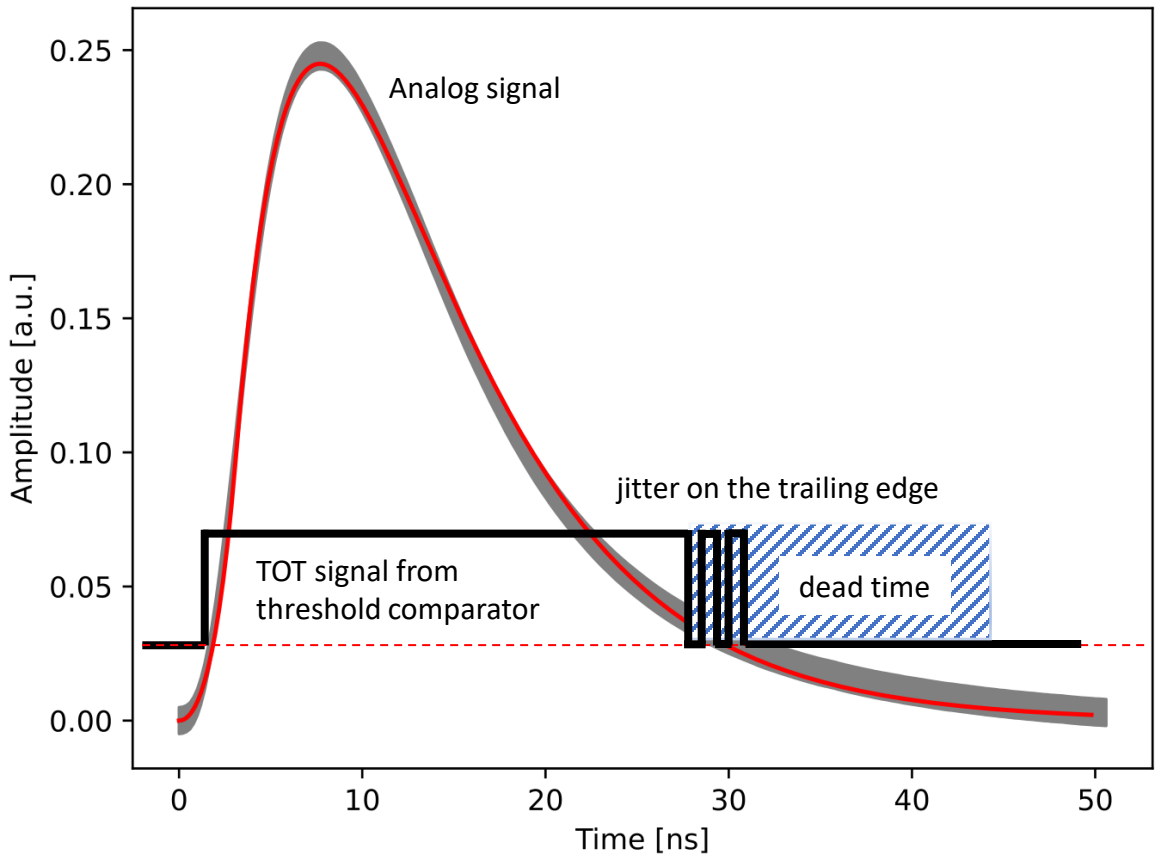
- Ethernet UDP protocol (***IPbus*** [1]) is used for data forwarding and board control
- Local network connect readout boards (8 ethernet links) with FLP

- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit per link is not exceed ***100 Mbit/s***. ***The continuous readout*** is implemented without busy signal.

- The trigger is processed on FLP site:
  - Trigger signal is connected to TDC channel and digitized with WR timestamp in FPGA
  - Message trigger accompanied by a timestamp is transmitted to FLP for event selection

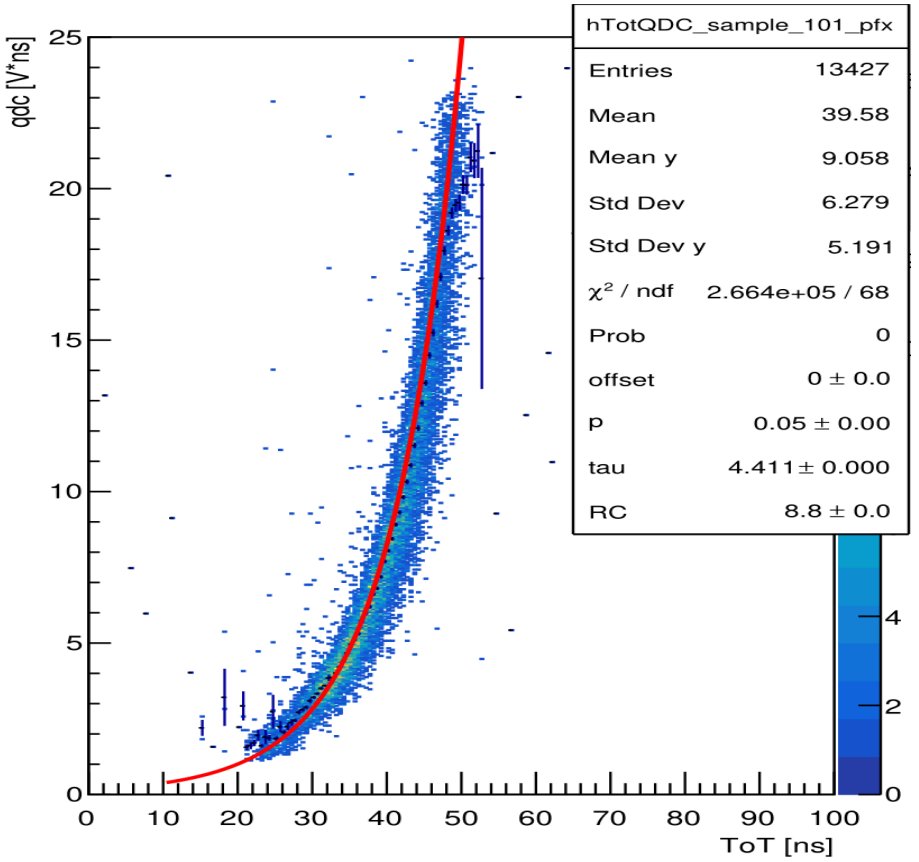
[1] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, ***IPbus: a flexible Ethernet-based control system for xTCA hardware***, *JINST 10 (2015) no.02, C02019.*

TDC Time Over Threshold (TOT)



- The threshold is tunable around 20 mV
- Signals length range is 20 – 60 ns
- Signals less than 6.4 ns are rejected for noise reduction
- Dead time is tunable in range 30 – 200 ns for comparator jitter filtering
- Minimum TOT time and dead time available in FPGA TDC are 3.2 ns

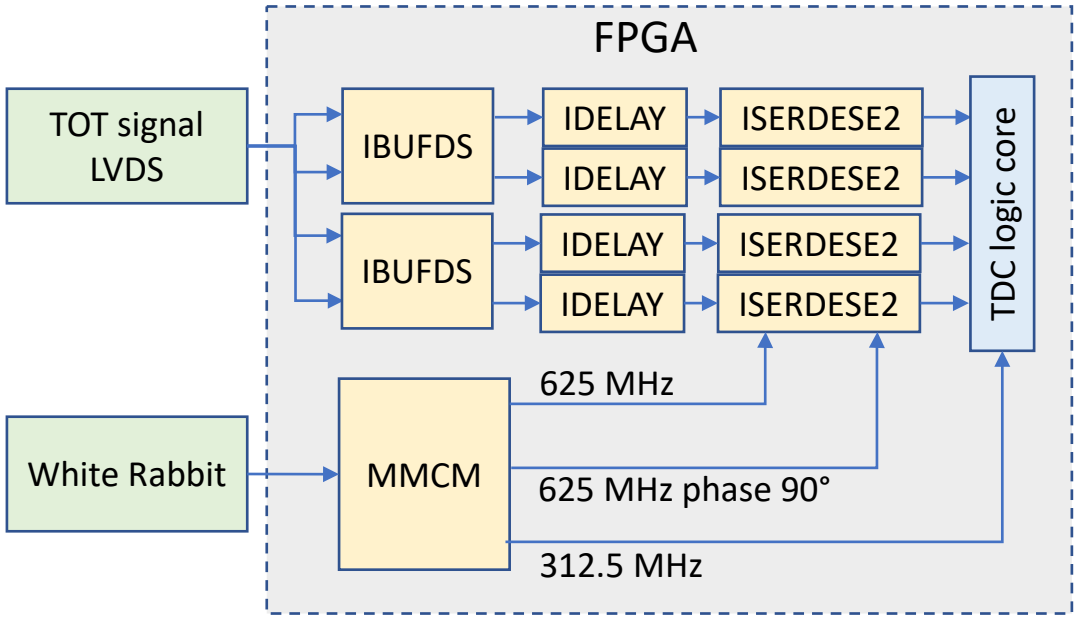
Amplitudes vs TOT time with analytical forecast

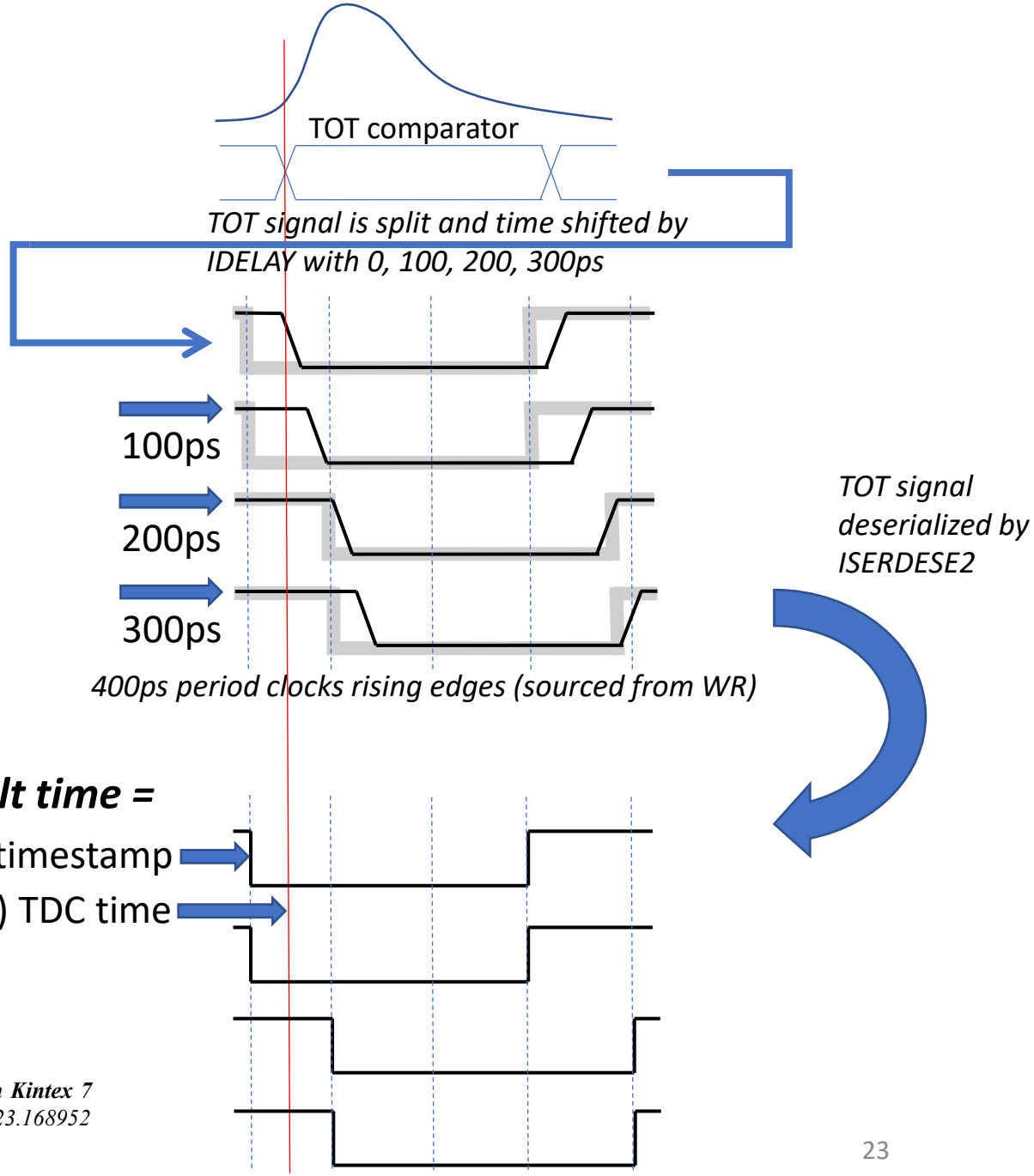


- TOT amplitude resolution is in range 14 - 22%
- Is used for time slewing correction

[2] N. Karpushkin, D. Finogeev, F. Guber, D. Lyapin, A. Makhnev et al., ***Analytical description of the time-over-threshold method based on time properties of plastic scintillators equipped with silicon photomultipliers,*** *DOI: 10.1016/j.nima.2024.169739*

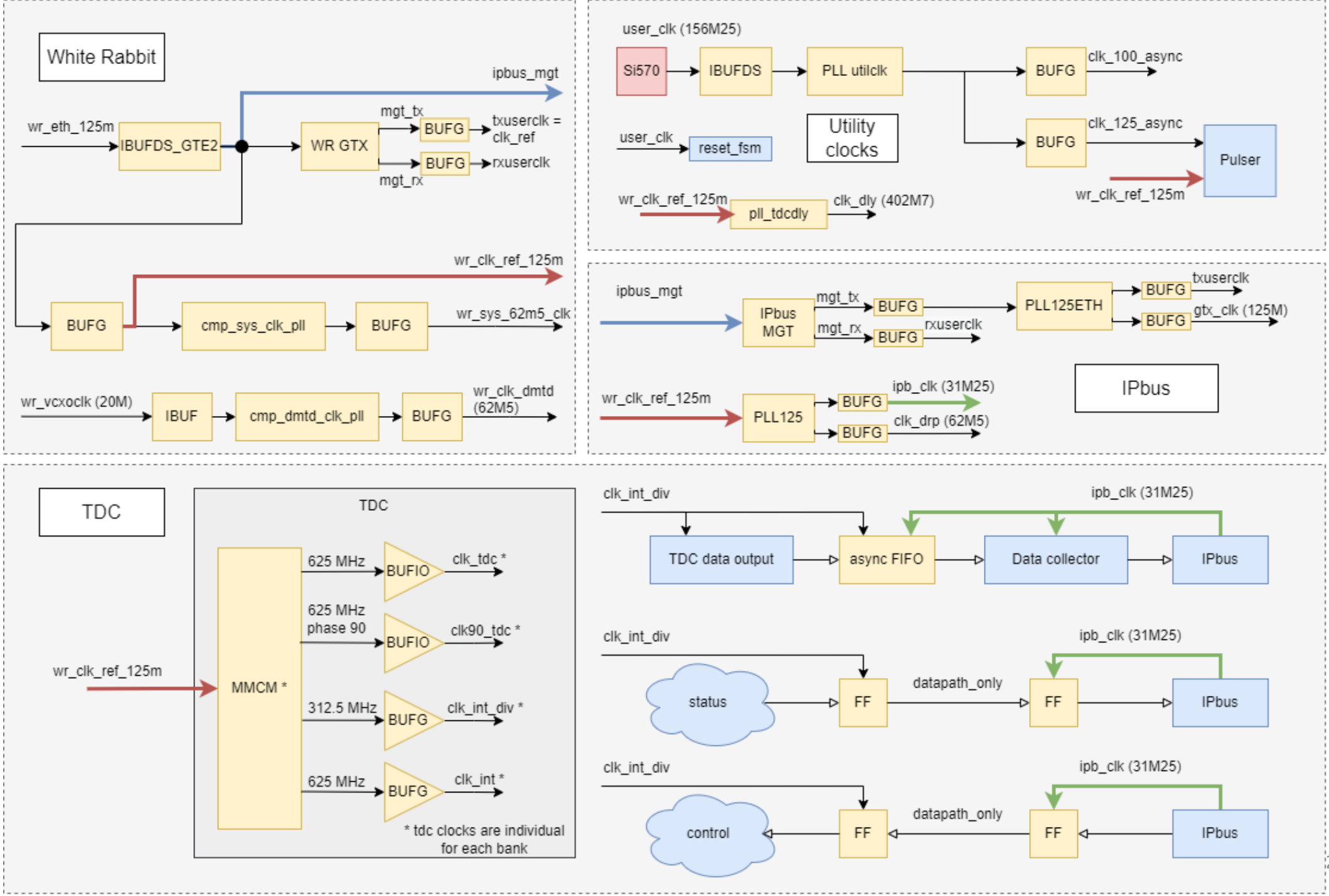
The 100ps FPGA TDC principle of operation



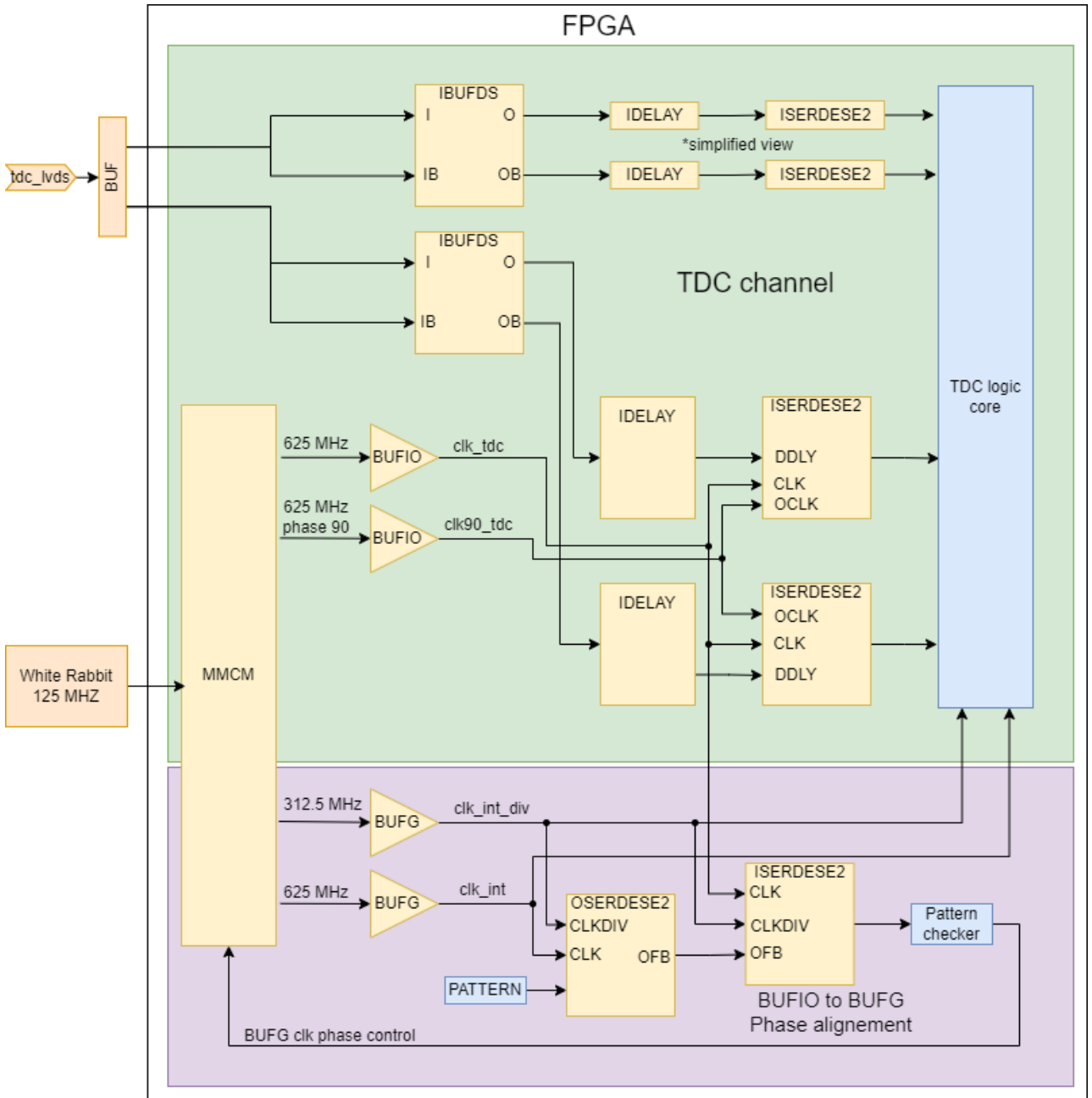


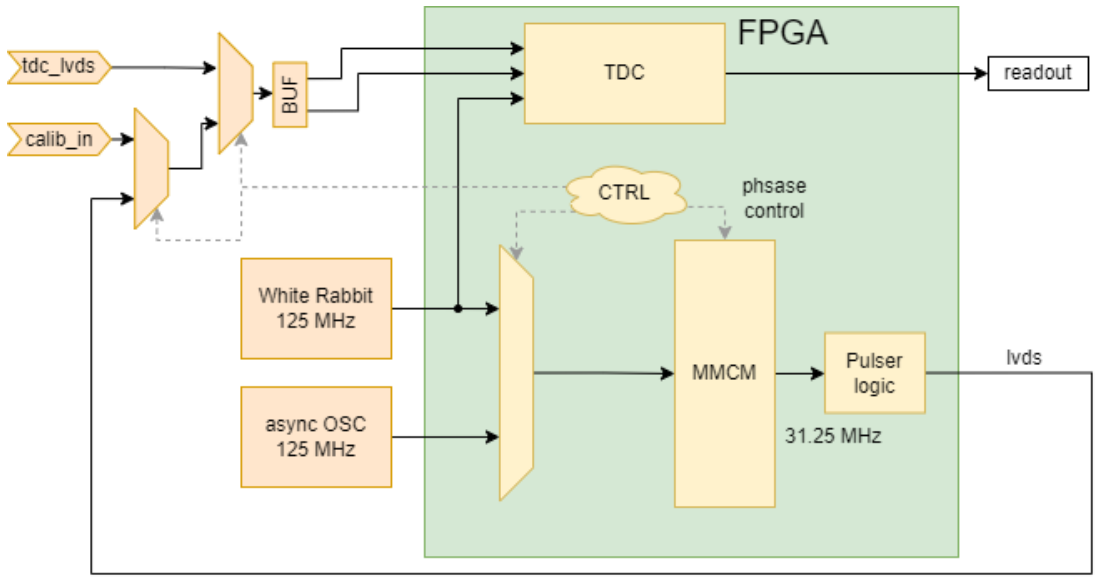
The TDC is **based on the Kintex-7** input serial-to-parallel converter with oversampling capability and programmable delay. The design is **based on Xilinx recommendations**, and uses **only documented features** of the FPGA within its specifications.

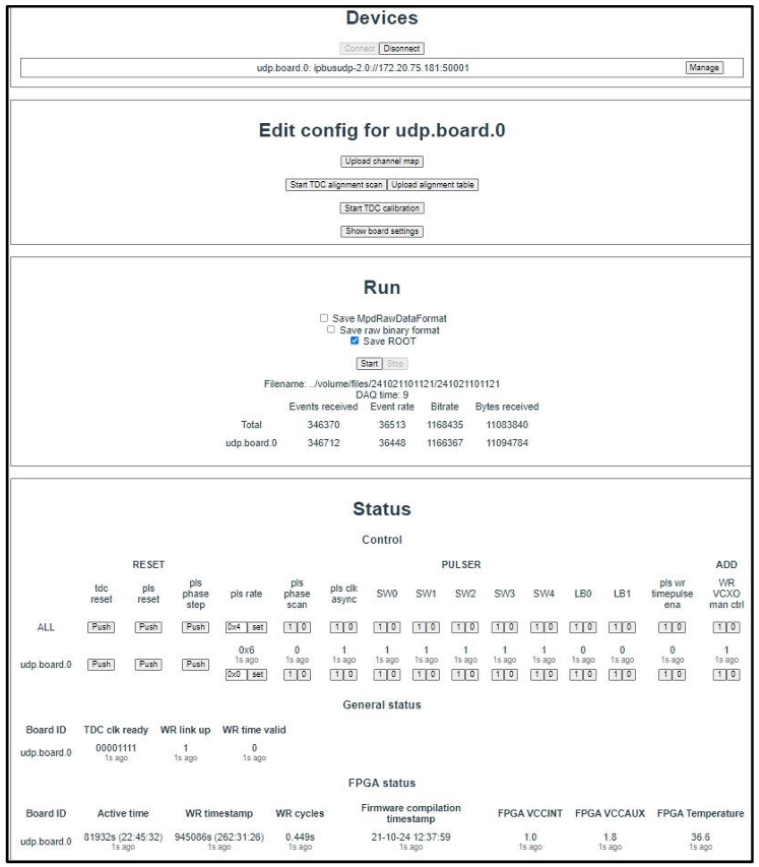
[3] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

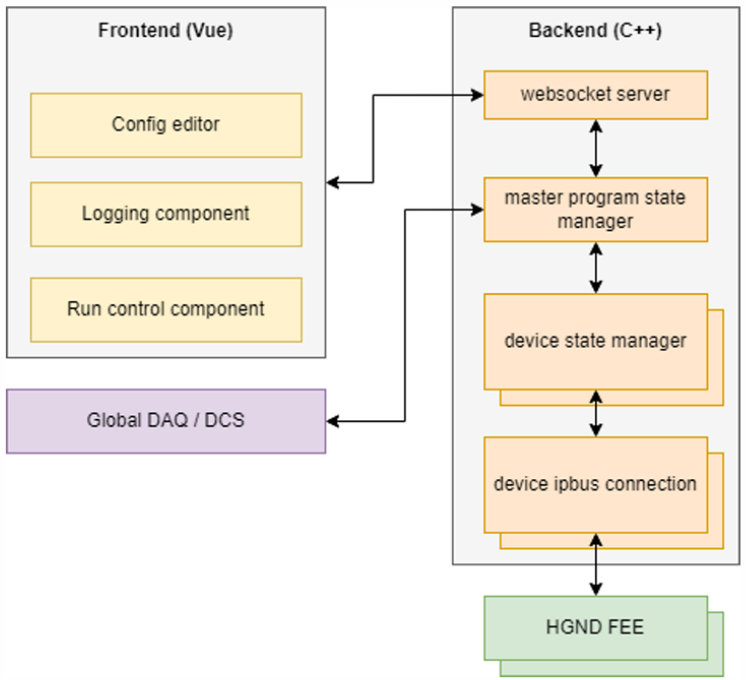

White Rabbit
ipbus_mgt
wr_eth_125m
IBUFDS_GTE2
WR GTX
mgt_tx
BUFG
txuserclk = clk_ref
BUFG
rxuserclk
mgt_rx
wr_clk_ref_125m
BUFG
cmp_sys_clk_pll
BUFG
wr_sys_62m5_clk
wr_vcxoclk (20M)
IBUF
cmp_dmtd_clk_pll
BUFG
wr_clk_dmtd (62M5)
user_clk (156M25)
Si570
IBUFDS
PLL utilclk
BUFG
clk_100_async
user_clk
reset_fsm
Utility clocks
BUFG
clk_125_async
Pulser
wr_clk_ref_125m
wr_clk_ref_125m
pll_tdcdly
clk_dly (402M7)
ipbus_mgt
IPbus MGT
mgt_tx
BUFG
mgt_rx
BUFG
rxuserclk
PLL125ETH
BUFG
txuserclk
BUFG
gtx_clk (125M)
IPbus
wr_clk_ref_125m
PLL125
BUFG
ipb_clk (31M25)
BUFG
clk_drp (62M5)
TDC
TDC
wr_clk_ref_125m
MMCM *
625 MHz
BUFIO
clk_tdc *
625 MHz phase 90
BUFIO
clk90_tdc *
312.5 MHz
BUFG
clk_int_div *
625 MHz
BUFG
clk_int *
* tdc clocks are individual for each bank
clk_int_div
ipb_clk (31M25)
TDC data output
async FIFO
Data collector
IPbus
clk_int_div
ipb_clk (31M25)
status
FF
datapath_only
FF
IPbus
clk_int_div
ipb_clk (31M25)
control
FF
datapath_only
FF
IPbus

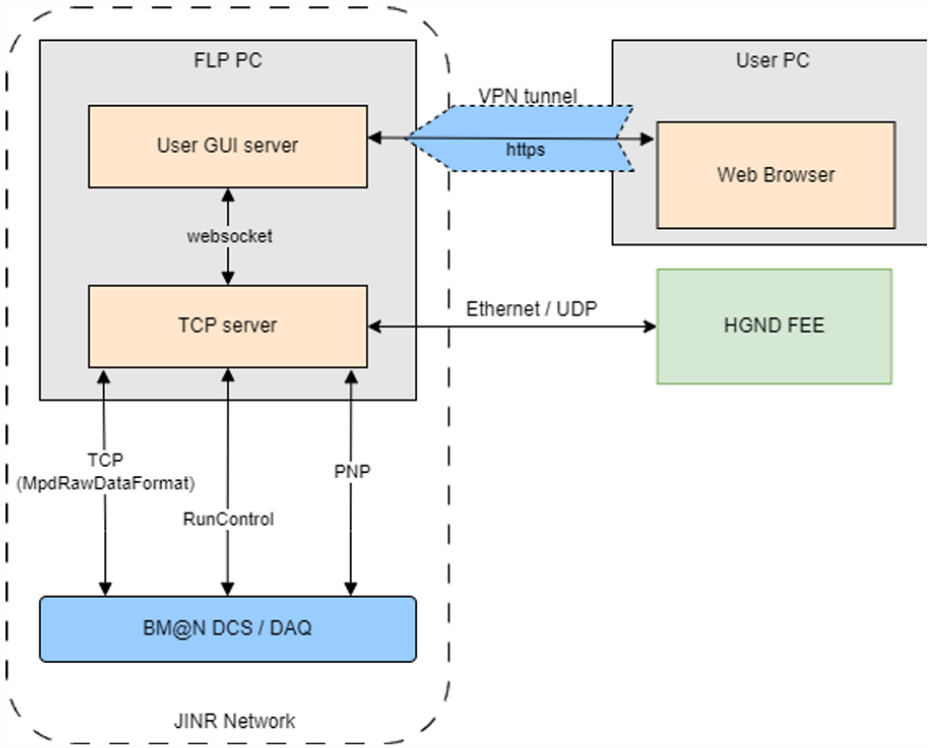
FPGA TDC and calibration pulser clocks layout






Devices
Connect
Disconnect
udp.board.0: ipbusudp-2.0:///172.20.75.181:50001
Manage
Edit config for udp.board.0
Upload channel map
Start TDC alignment scan
Upload alignment table
Start TDC calibration
Show board settings
Run
Save MpdRawDataFormat
Save raw binary format
Save ROOT
Start
Stop
Filename: .../volume/files/241021101121/241021101121
DAQ time: 9
Events received
Event rate
Bitrate
Bytes received
Total
346370
36513
1168435
11083840
udp.board.0
346712
36448
1166367
11094784
Status
Control
RESET
PULSER
ADD
tdc reset
pls reset
pls phase step
pls rate
pls phase scan
pls clk async
SW0
SW1
SW2
SW3
SW4
LB0
LB1
pls wr timepulse ena
WR VCXO man ctrl
ALL
Push
set
udp.board.0
0x6
1s ago
General status
Board ID
TDC clk ready
WR link up
WR time valid
udp.board.0
00001111
FPGA status
Board ID
Active time
WR timestamp
WR cycles
Firmware compilation timestamp
FPGA VCCINT
FPGA VCCAUX
FPGA Temperature
udp.board.0
81932s (22:45:32)
945086s (262:31:26)
0.449s
21-10-24 12:37:59
1.0
1.8
36.6


Frontend (Vue)
Config editor
Logging component
Run control component
Global DAQ / DCS
Backend (C++)
websocket server
master program state manager
device state manager
device ipbus connection
HGND FEE


FLP PC
User GUI server
websocket
TCP server
TCP
(MpdRawDataFormat)
RunControl
PNP
BM@N DCS / DAQ
JINR Network
VPN tunnel
https
User PC
Web Browser
Ethernet / UDP
HGND FEE