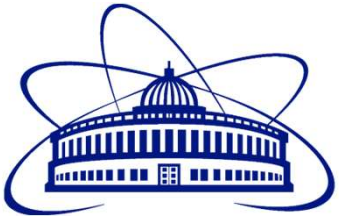
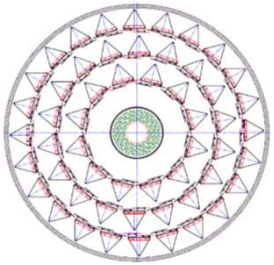




MPD ITS Status and Perspectives

Yuri Murin (LHEP JINR) for the MPD ITS Consortium

XV MPD Collaboration Meeting,

Dubna, 15-17 Aril 2025



Outline

“ Roughly 95% of events generated in relativistic heavy ions collisions do not carry information of interest w.r.t. announced goals of the up-to-date experiment “ – *the CBM reminder*

- The MPD tracking system as a backbone of the MPD and the role of ITS
- The MPD ITS layout with description of its basic components
- Status of the ITS mechanics and leakless water&dry gas cooling systems
- Status of the MICA chip R@D effort at CCNU (Wuhan)
- Status of the RU and PU R@D at USTC (Hefei)
- Preparations for the in-beam tests of the MAPS sensors/module and its readout system with protons in Protvino (150-300 MeV) and Gatchina (1000 MeV)
- Conclusions and outlook.

NICA MPD-Inner Tracking System based on ALICE ITS-2 technology

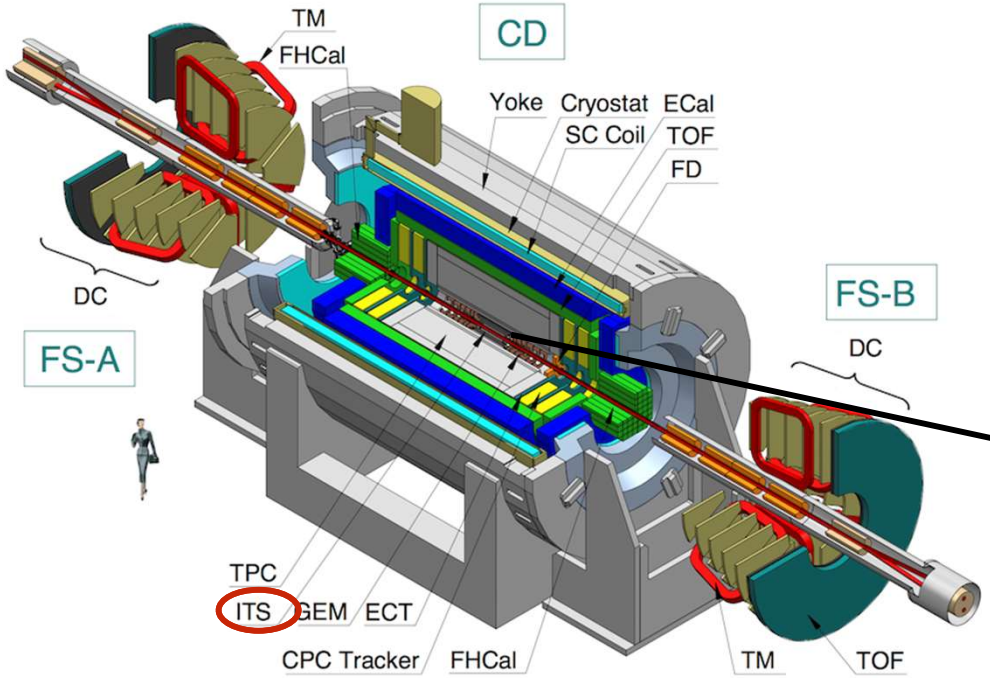
MPD-ITS structure: 3-layers Inner Barrel + 3-layers Outer Barrel .

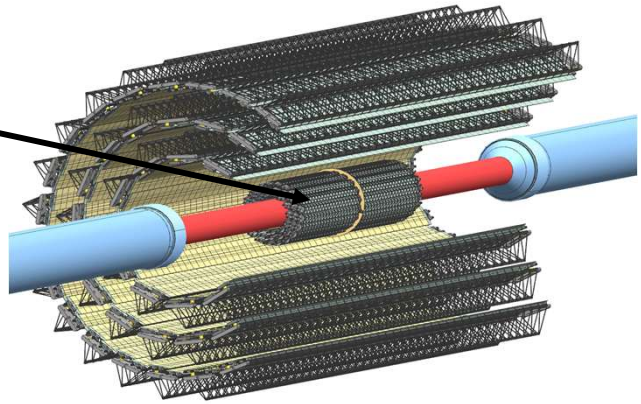
Looking for needle in a haystack

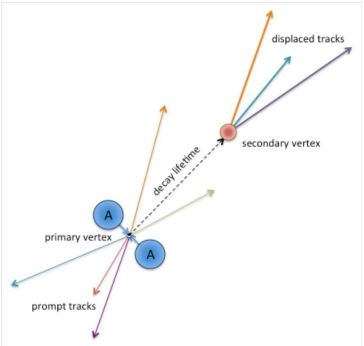
It will supplement the TPC for the precise tracking, momentum determination and vertex reconstruction for **low Pt momenta hyperons** (Λ, Ξ, Ω) and identification of **D-mesons.**

Some of the MPD-ITS requirements:

- **Fast, high granularity CMOS pixel sensors with low noise level.**
- **Spatial resolution of track coordinate registration at the level of ~5–10 μm.**
- **Material budget as low as possible.**
- **Positioned as close as possible to the interaction diamond**

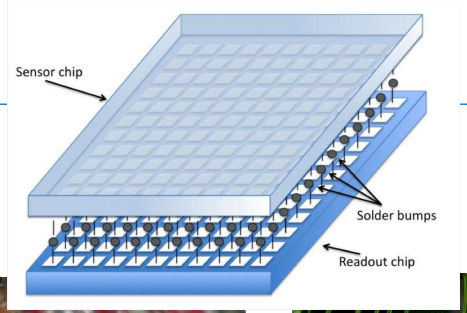


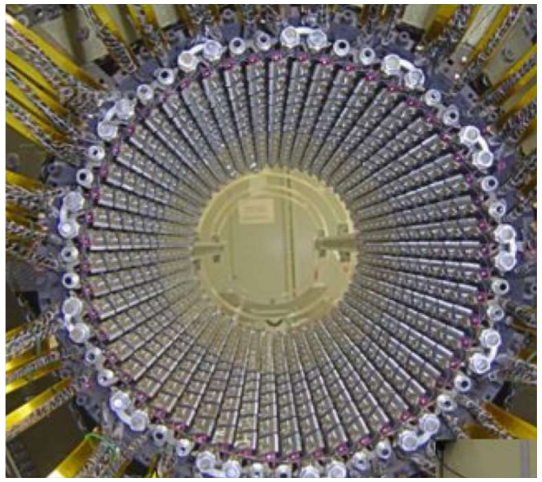
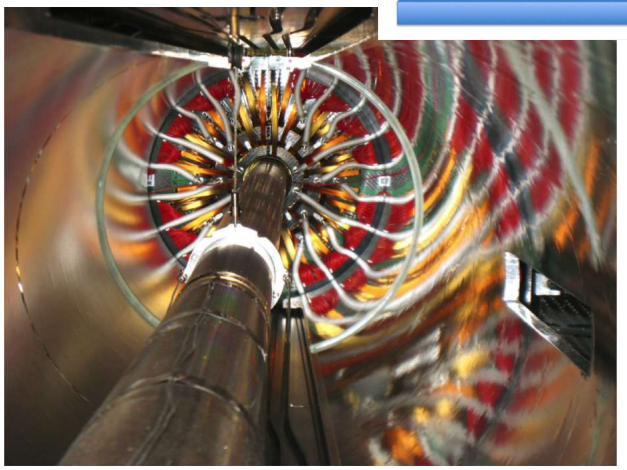
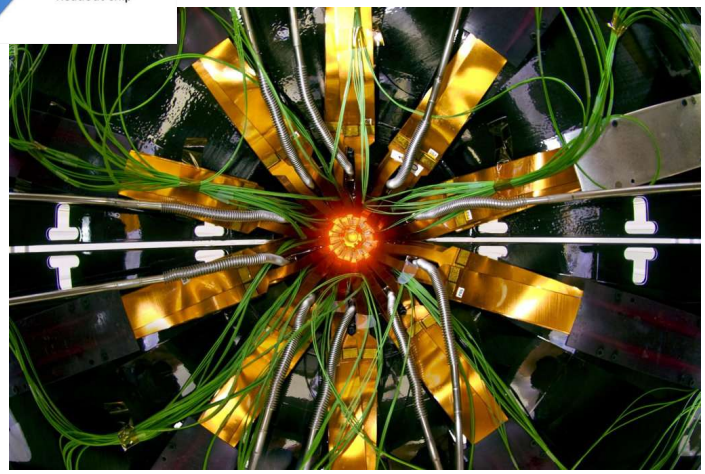




Yu. A. Murin and C. Ceballos, *"The Inner Tracking System for the MPD Setup of the NICA Collider"*, Phys. Part. Nuclei 52, 742–751 (2021).

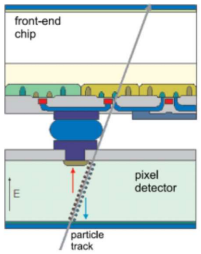
Пиксельные системы LHC Run#1

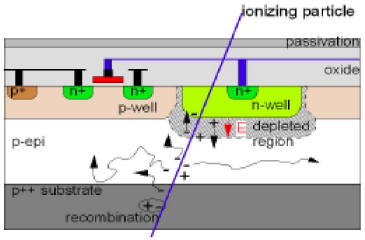


	ATLAS	CMS	ALICE
			
Число слоёв:	2	3	3
Число пикселей:	9.8M	80M	66M
Площадь, м²:	0.21	1.17	1.0
Размер пикселя, мкм²	50x425	50x400	100x150
Толщина (Si+ASIC), X/Xo [%]	0.21+0.16	0.27+0.19	0.30+0.19

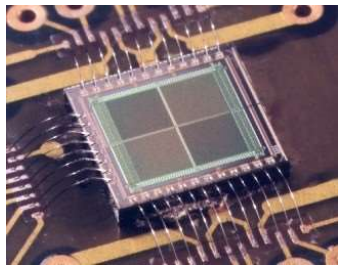
Mimosa series – IPHC Strasbourg - Move to standard CMOS

NIM A 458 (2001) 677-689





Mimosa1 – 1999
AMS 0.6 µm

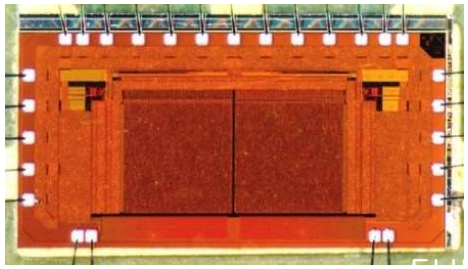


20um pixel

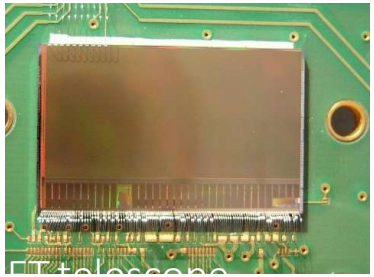
Mimosa2 – 2000
MIETEC 0.35 µm

20um pixel

Mimosa3 – 2001
IBM 0.25 µm



Mimosa26 – 2008
AMS 0.35 µm



Full detector Jan 2014

Physics Runs in 2015-2016

- 2 layers (2.8 and 8 cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector
- Radiation length (1st layer)
- x/X0 = 0.39% (Al conductor flex)

MIMOSA28 (ULTIMATE) – 2011

First MAPS system in HEP

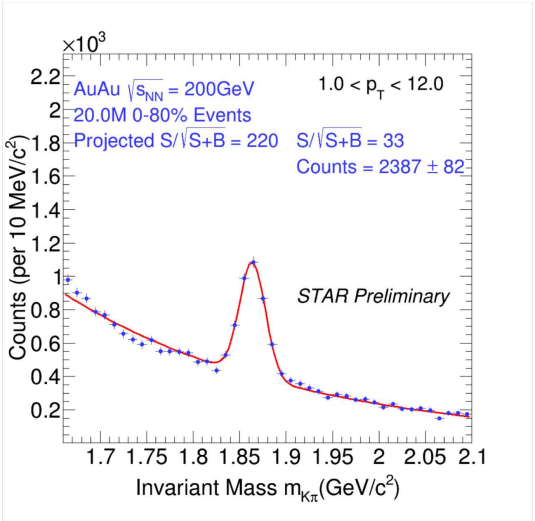
Twin well 0.35 µm CMOS (AMS)

- 18.4 µm pitch
- 576x1152 pixels, 20.2 x 22.7 mm^2
- Integration time 190 µs
- No reverse bias -> NIEL ~ 10^{12} n_{eq}/cm^2
- Rolling shutter readout

12 years from idea to first results STAR !

....

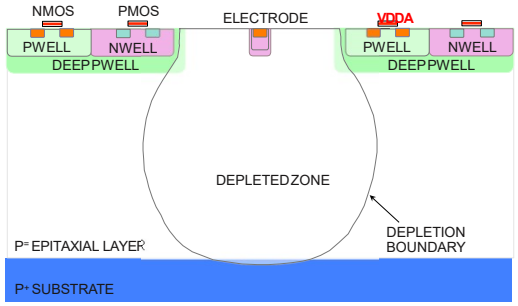
....

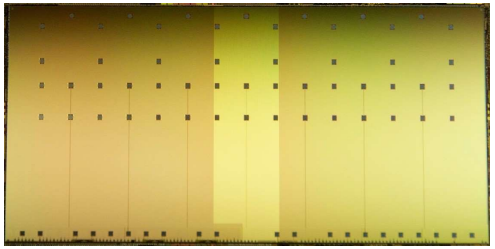


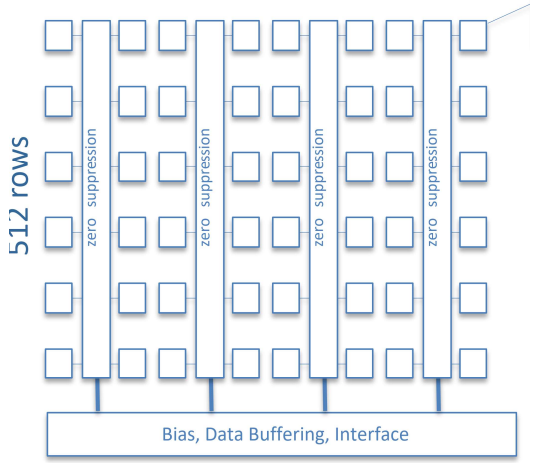
ALPIDE

Zero-suppressed readout, no hits no digital power

G. Aglieri et al. NIM A 845 (2017) 583-587







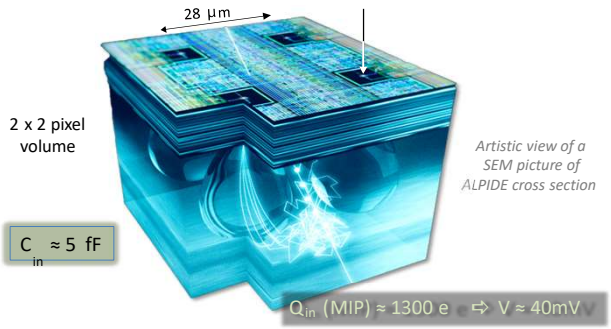
130,000 pixels / cm^2 27x29x25 µm^3

charge collection time <30ns (V_{bb} = -3V)

Max particle rate: 100 MHz/cm^2

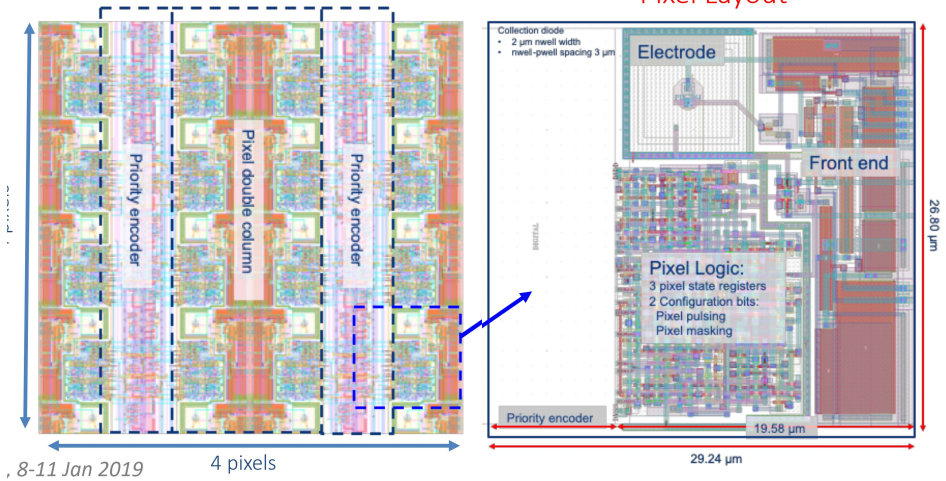
fake-hit rate: < 1 Hz/ cm^2

power : ≈300 nW /pixel (<40mW/cm^2)



Matrix Layout

Pixel Layout



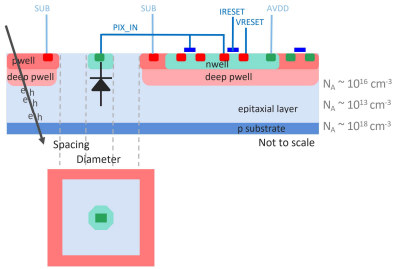
, 8-11 Jan 2019

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

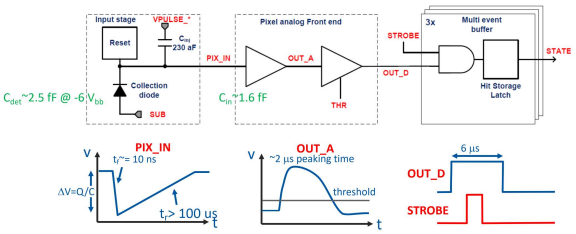
1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

Basic ALPIDE signal processing and data management features

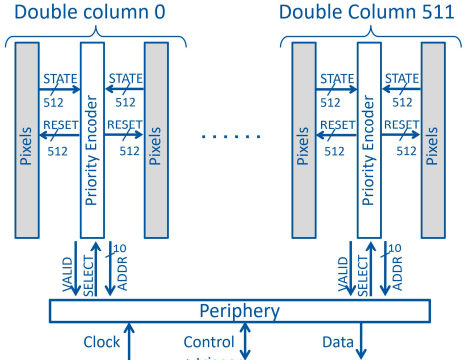
Extremely high sensitivity



Analogue delay memory



Clockless priority encoding



Analog front-end and discriminator continuously active

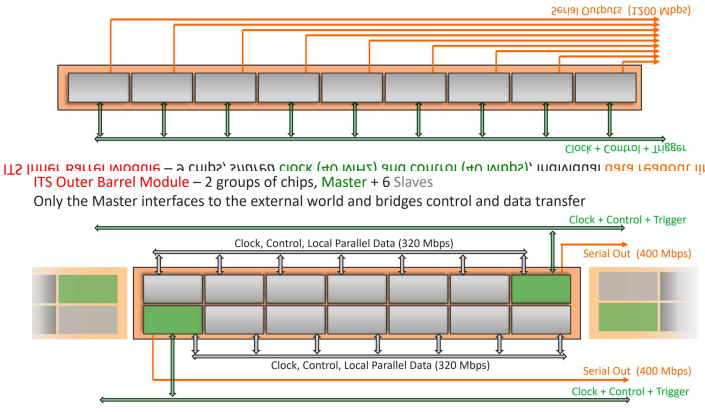
- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

Front End Characteristics	
Gain (small signal) [mV/e]	4
ENC [e]	3.9
Threshold [e]	92 ± 2

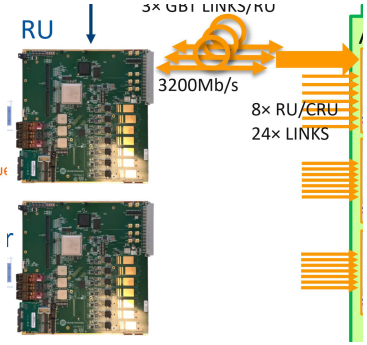
The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

- Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

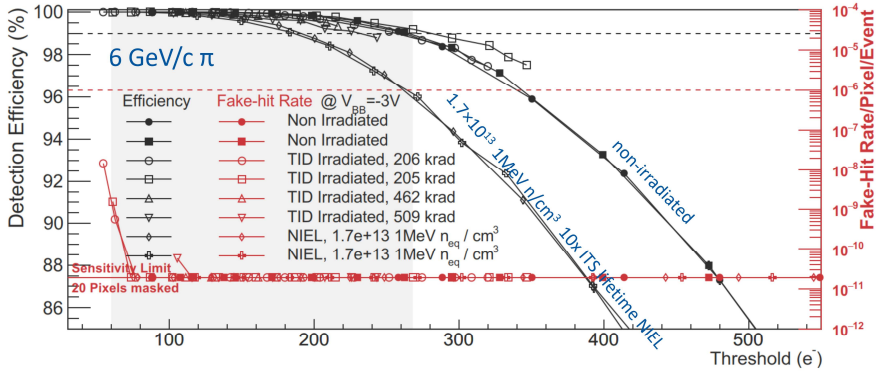
Smart data management and Control



GBT interface



Sufficient adiation hardness with reverse bias -> NIEL ~ 3 ·10¹³ n_{eq}/cm^2



Components for building ITS by - OB:2028 & OB+IB:2029/30

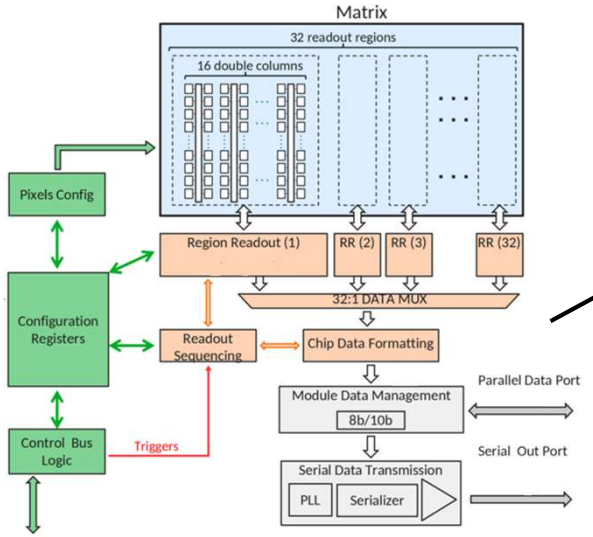
The MAPS chip - MICA

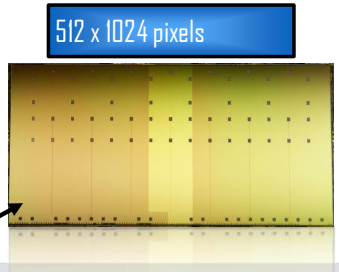
PRC FAB 0.13 μm CMOS pixel sensor first prototype

» High-resistivity (> 1kΩ cm) p-type substrate (500μm thick later to be thinned)

» Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance.

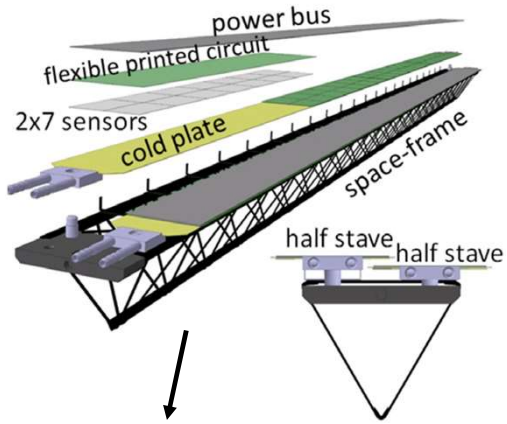
» Deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area.

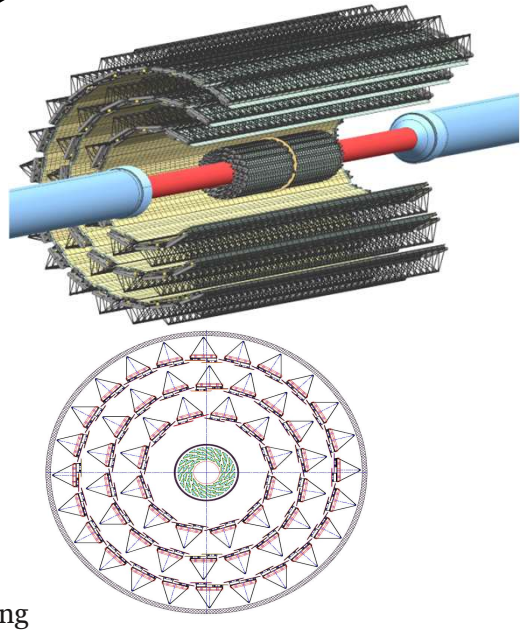




Sensor architecture

Size: 15mm x 30mm
Pixel pitch: 30.53μm x 26.8μm
Peaking time: < 1μs
Integral time: 5-10 μs
Power consumption: 30.5nA/pixel
Dead area 1.1mm x 30mm





OB = 54 Staves

Total number chips

10584 pcs

IB = 2x 48 Staves

Total number chips

864 pcs

Total number pixels

5,724 10^9

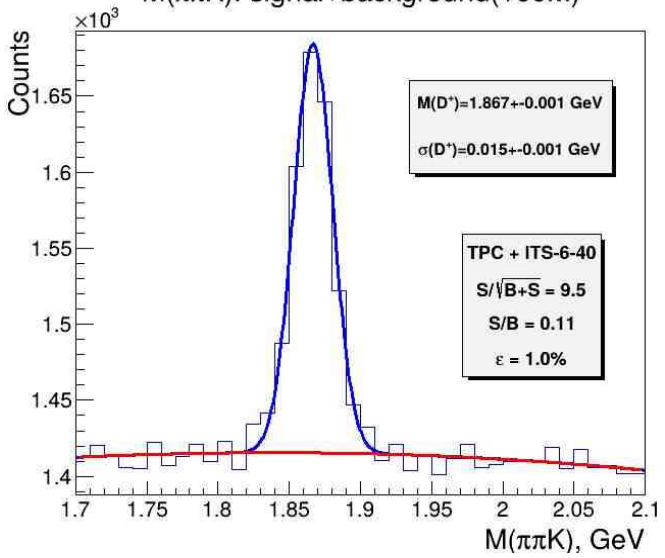
MPD ITS computer simulations predictions for open charm identification

MPD - ITS

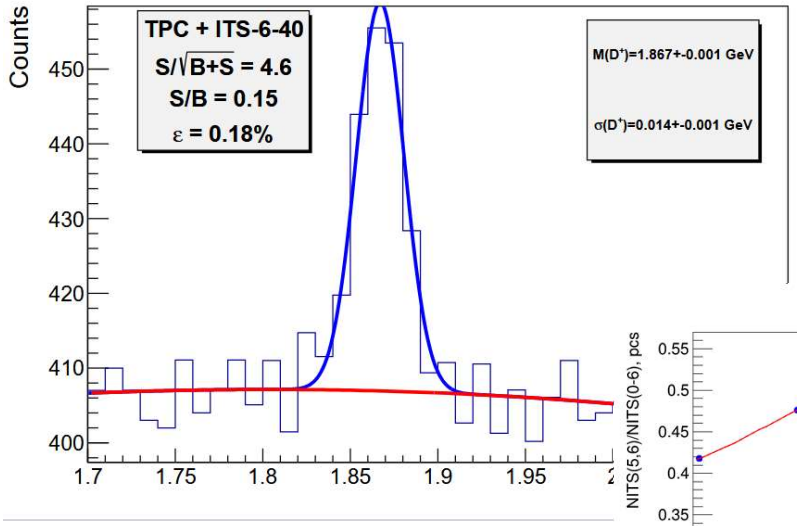
10,8 GeV Bi+Bi: D⁺ and D⁰ reconstruction using KF with TPC-TOF PID

$$D^+ \rightarrow K^- + \pi^+ + \pi^+$$

M(ππK): signal+background(100M)



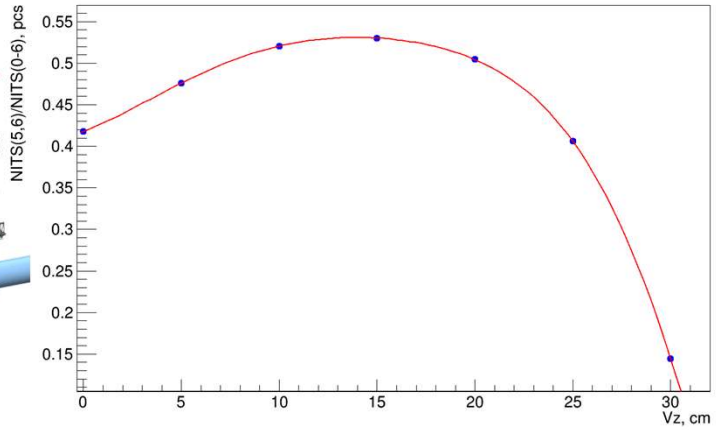
M(ππK): signal+background(100M)



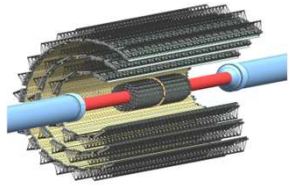
Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

Efficiency vs shift of vertex along Z-axis

Number of ITS(5,6)/ITS(0-6) from Vz



N_D = 19 000 mesons/month
for D^+ before IB design finalized and .....after



Using the optimal BDT cut allows to reconstruct D^+ and D^0 with an efficiency of **1.0%** and **0.4%** respectively.

Reduction efficiency by factor 5! for realistic length of IB

E.Tsapulina, V.Kondratiev, Y.Murin

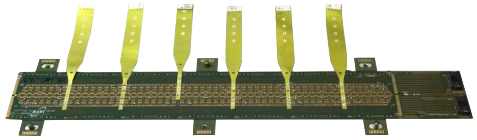
Module (HIC) and Supermodule(Staves) Assembly Readiness

Full technological transfer from ALICE to MPD

- Complete KnowHow
- Detector assembly and testing hardware/software
- Supervision and support from ALICE specialists

} Setup at JINR of the full detector assembly line from chips to detector layers

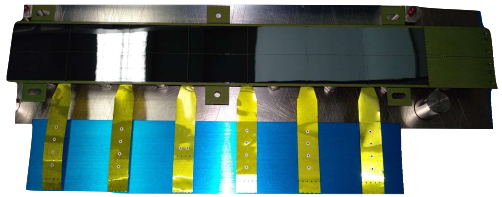
FPC

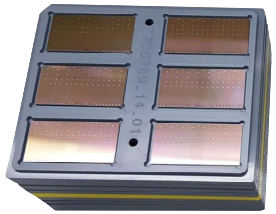


+

MAPS

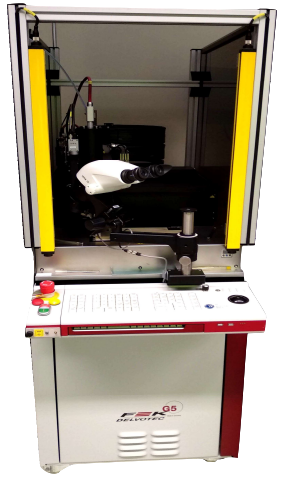
HIC



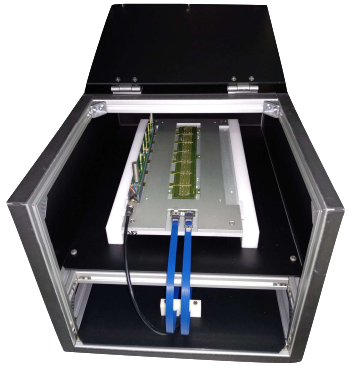


Chips selection

Chips alignment and gluing



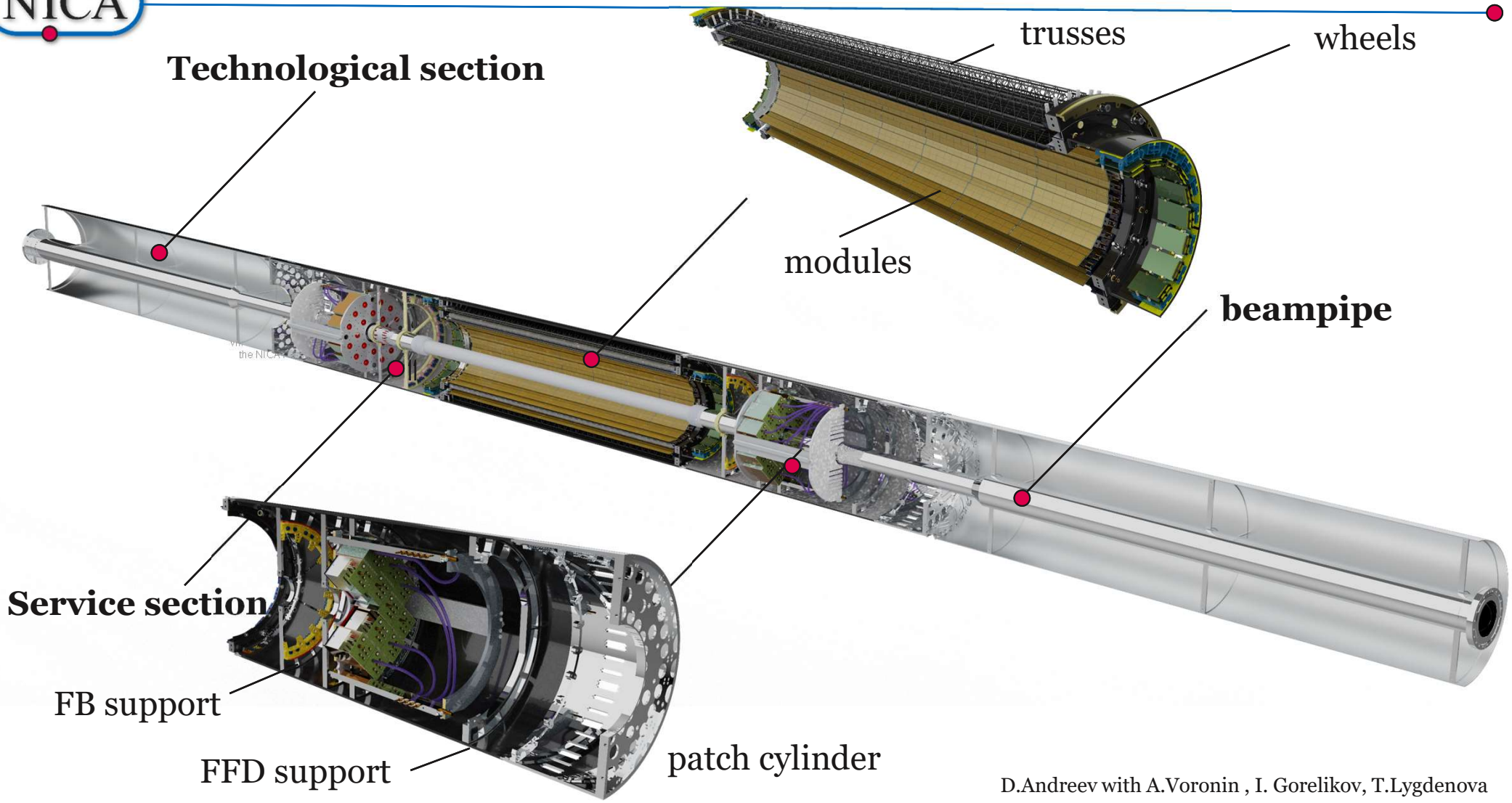
Ultrasonic bonding Chips - FPC



HIC testing

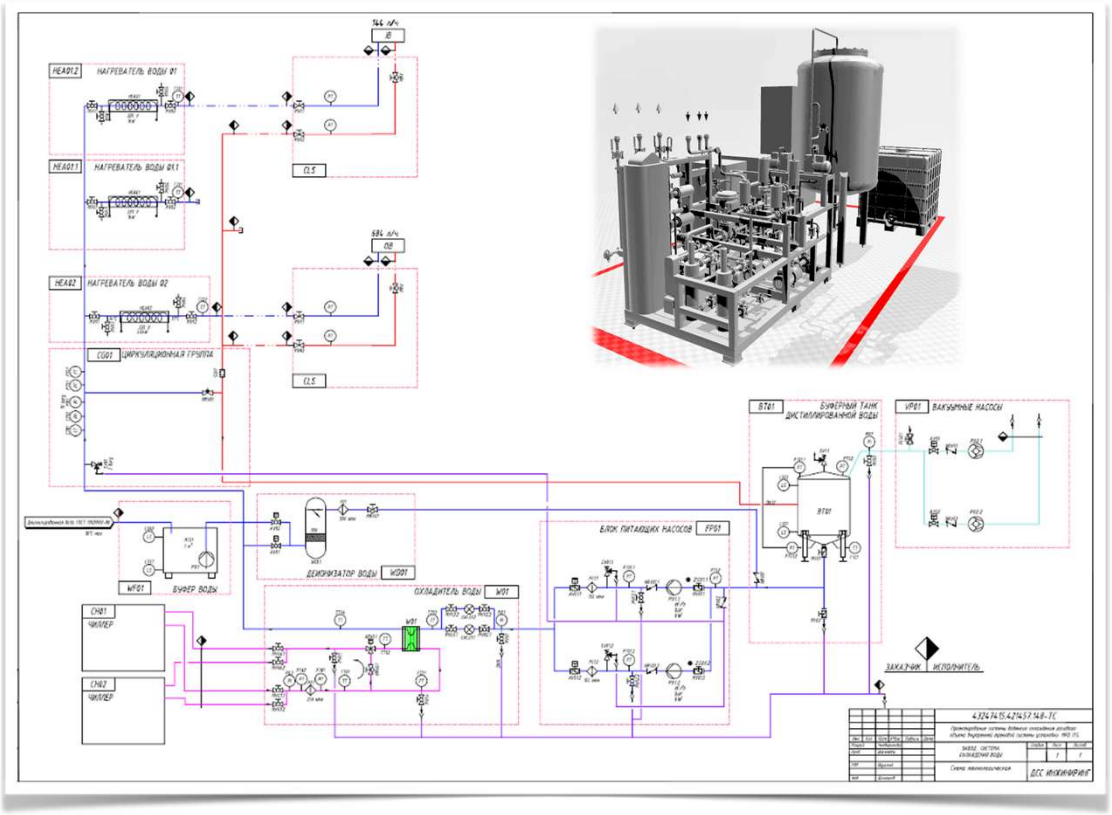
A.Sheremetiev with T.Andreeva, S.Patronova,T.Semchukova and C/Ceballos

MPD ITS mechanical structure



D.Andreev with A.Voronin , I. Gorelikov, T.Lygdenova

Cooling Plant by DSSE for leakless water cooling system



Barrel type	No. of Staves	No. of Panels	No. of Circuits	Power in the circuit [W]	Flow [l/h]
IB	96	96	24	240	288
OB	54	108	9	2187	684
Total ITS	150	204	33	2427	972

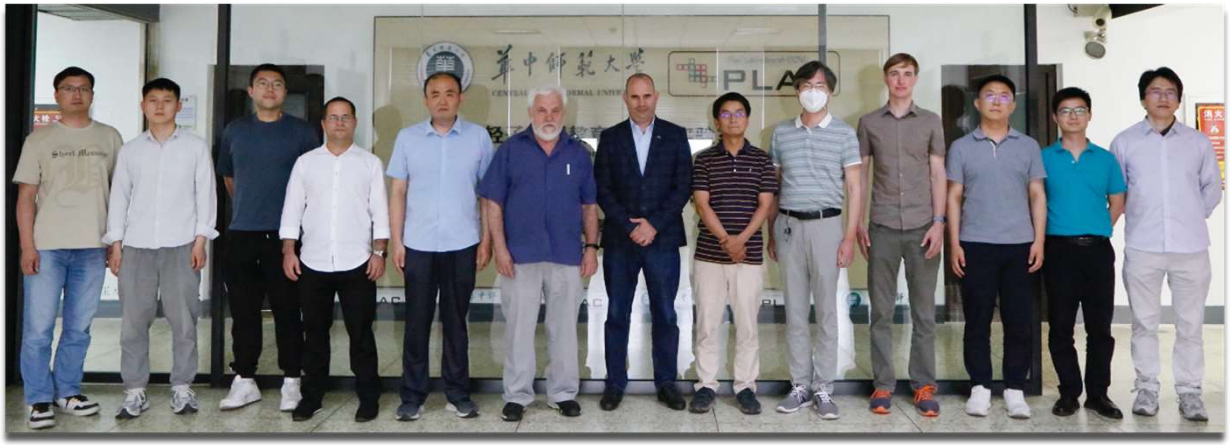
- Delivery of instrumentation and control equipment (Dec. 2024).
- Production and tests (May. 2025).

V.Elsha and T.Lygdenova

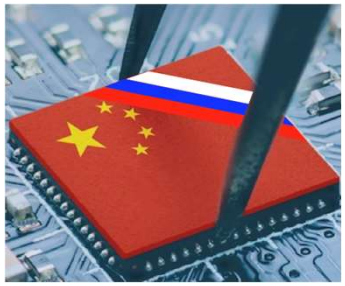
Electronics Challenge

The long-term sustainable proposal

NICA-MPD/ITS Seminar on China-Russia Cooperation, Wuhan, 2023.06.15-16



2023



MICA

Participants: JINR, CCNU, USTC, IHEP and IMP.

It was agreed: A joint development and construction of Monolithic Active Pixel Sensors **(MAPS)** for fundamental and applied science experiments **including front-end electronics** to make this technology **freely accessible** to China and Russia.

Yu. A. Murin, C. Ceballos Sanchez for the MPD-ITS Collaboration, *"Modern Microelectronics for MPD-ITS. Monolithic Active Pixel Sensors and Readout System"*, accepted for publication in the 4th issue of Phys. Part. and Nucl. in 2024

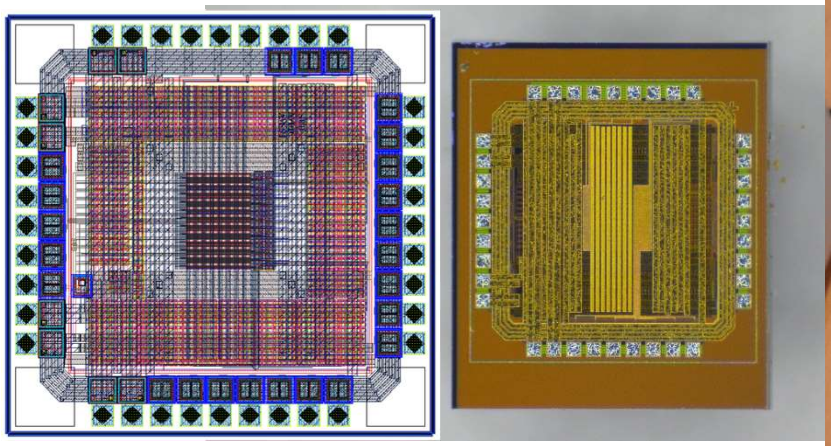
MICA: MPW scouting pixel technology with different processes

^{90}Sr test	55 nm CIS technology	180 nm High Voltage technology 0V bias	180 nm High Voltage technology -9V bias	130 nm Bulk CMOS process Low resistance substrate	130 nm Bulk CMOS process High resistance substrate 0V bias	130 nm Bulk CMOS process High resistance substrate -9V bias
MPV (ADC Value)	10(178e$^-$)	10 (462e$^-$)	To be tested	6.5	8.5	12
Case rate (per hour)	4100	1440	To be tested	840	2760	11700
Pixel size	24u×24u	30u x 30u		40u x 40u		

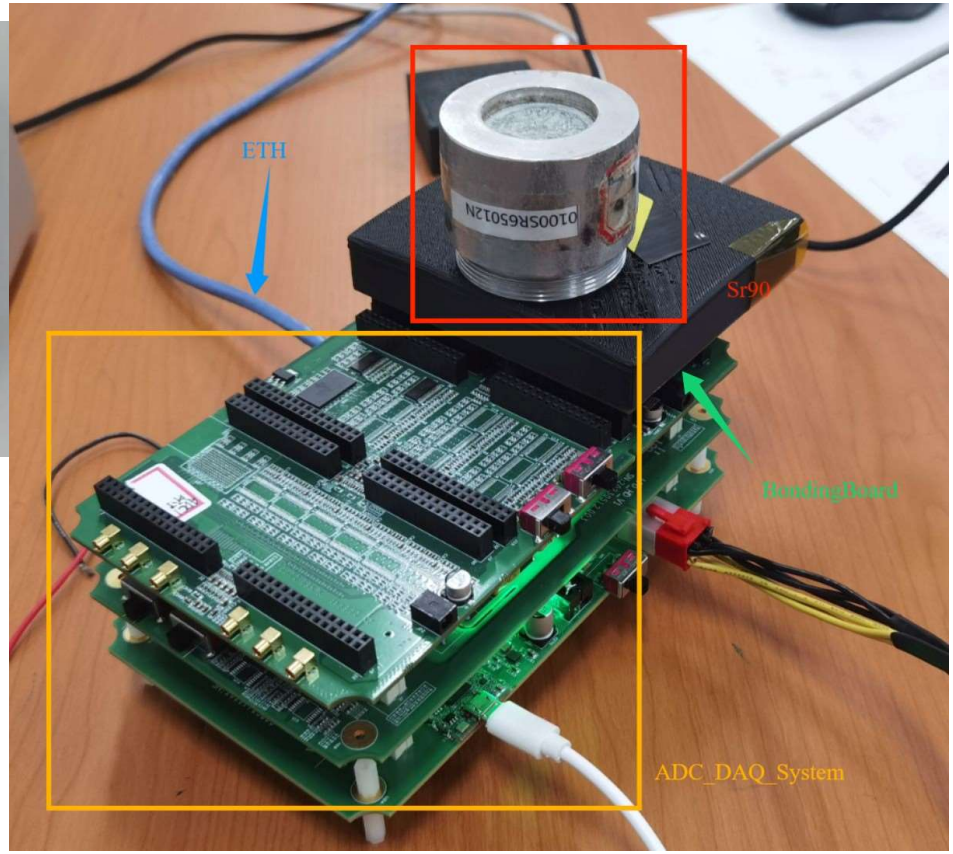
Courtesy of Prof. Xiangming Sun (CNNU)

MICA: testing methology development

Pixel Array Testing Chip



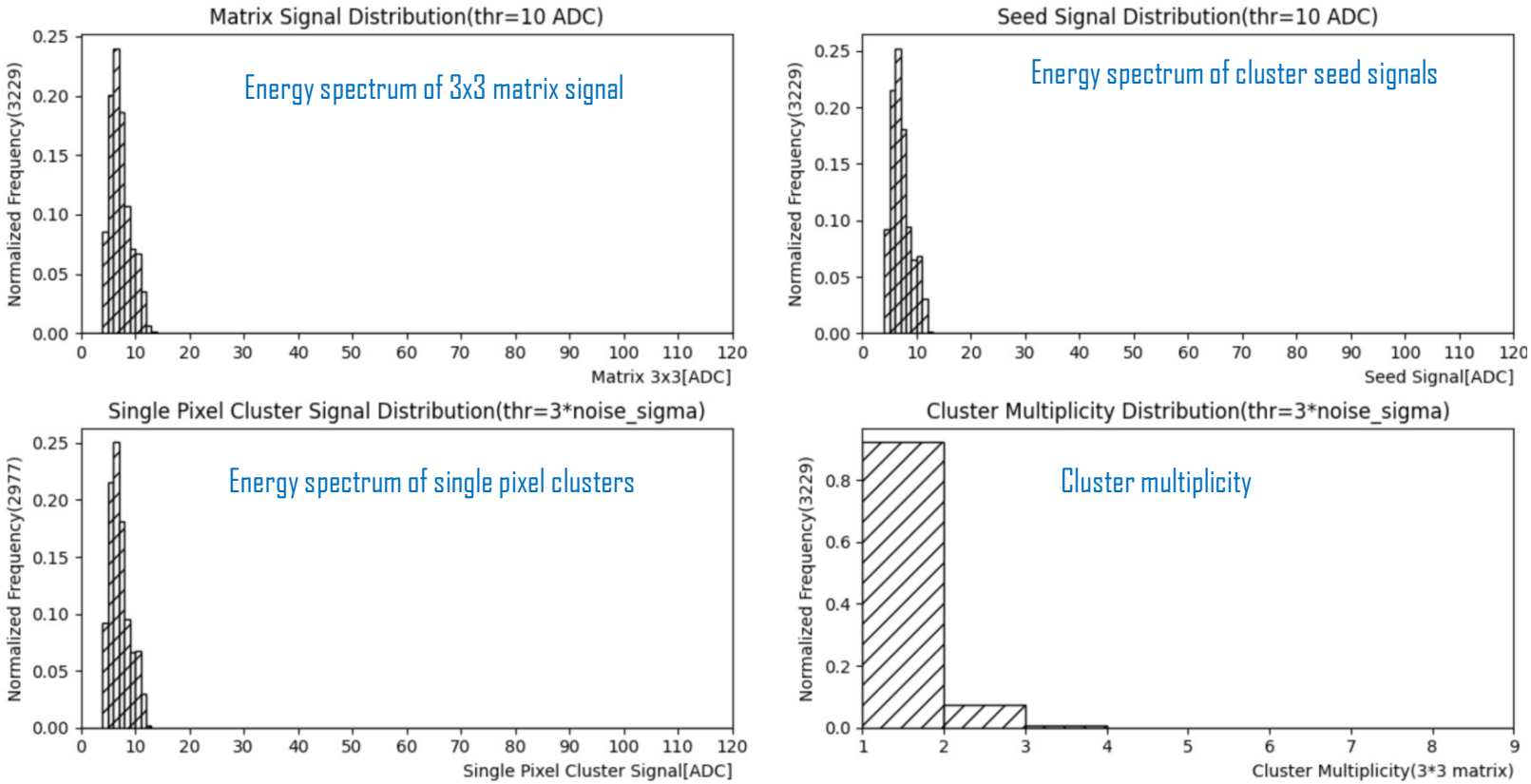
- Pixel Structure : Diode + SF
- Pixel Size : 30 × 30 um
- Array Size : (4 × 4) × 6
- Chip Size : 1580um × 1550um
- PXL<0:7> : DIODE RESET
- PXL<8:15> : PMOS RESET



Testing System

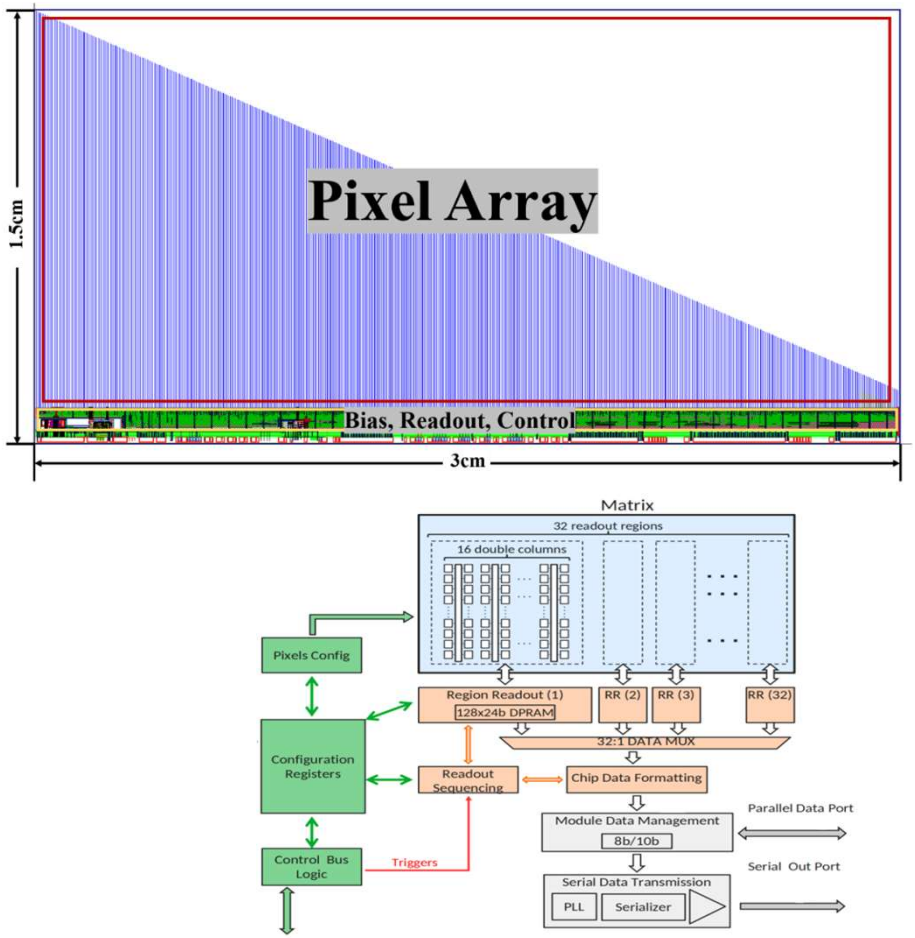
MICA: 130 nm Bulk CMOS Process Pixel Chip Test results

^{55}Fe Energy Spectrum (High Resistance Substrate -9V Bias



Courtesy of Prof. Xiangming Sun (CNNU)

Research on 130nm Bulk CMOS Process Pixel Chip— MICA prototype 1

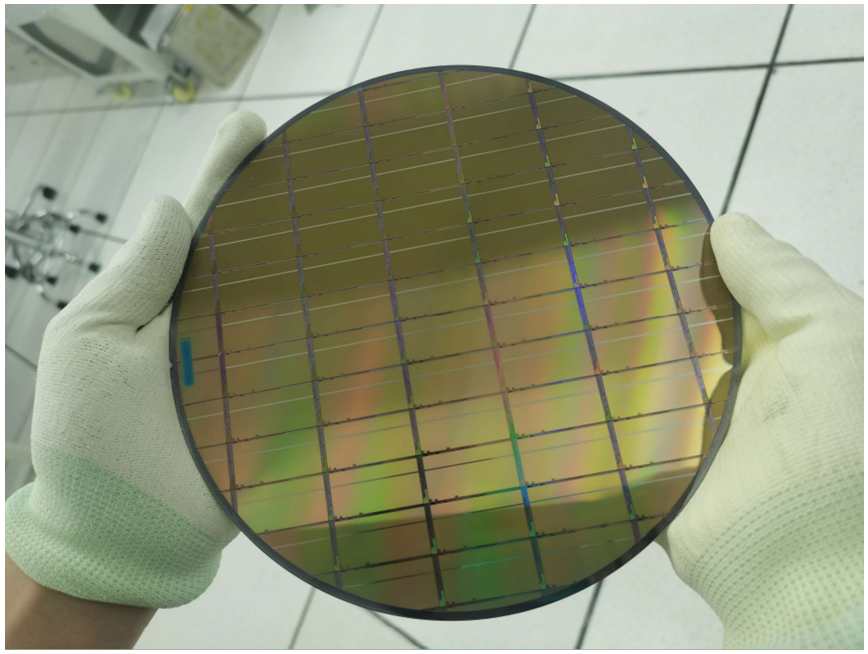


Fully functional MAPS chip MIC6_V3

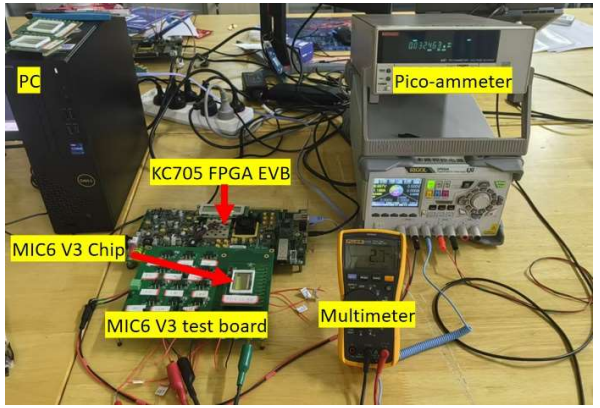
- Process: 130 nm bulk CMOS
- Chip Size: 15mm x 30mm
- Pixel Array: 512 × 2x490
- Pixel Size: 30.53 μ m × 26.8 μ m
- Peaking Time: < 1us
- Integral Time: 5-10 us
- Parallel Data Port: 80 MHz I/O CMOS 3.3 V
- High Speed Serial Data Port: 1.1 Gb/s, 8B10B encoding
- Configuration Interface: SPI
- Two Readout Modes: trigger mode and continuous mode
- Single pixel can be masked; Pixel includes built-in testing functionality
- Zero Compression Readout

Courtesy of Prof. Xiangming Sun (CNNU)

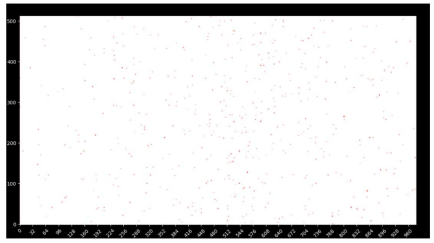
Research on 130nm Bulk CMOS Process Pixel Chip — MICA prototype #1



MICA prototype #1 wafer photo



Test platform



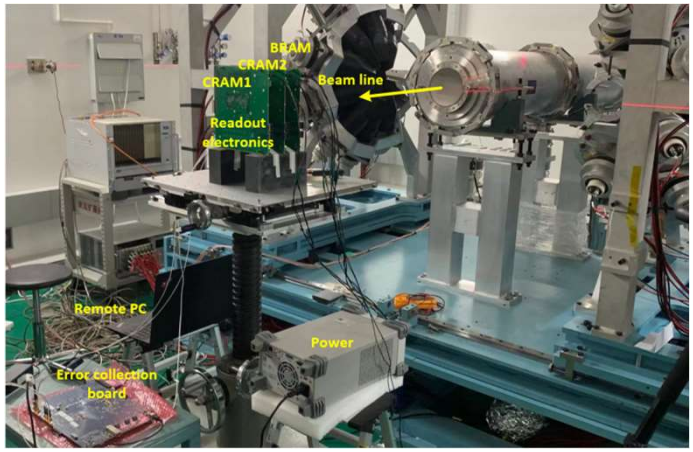
Tests result with ^{90}Sr source

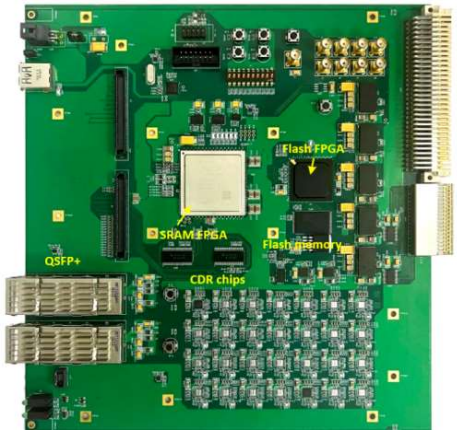
Courtesy of Prof. Xiangming Sun (CNNU)

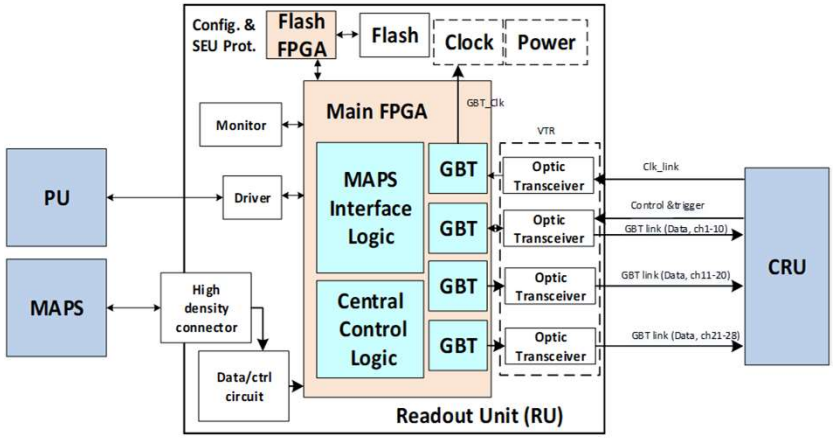
Readout Unit (RU) design by USTC

- The design of FPGA-based Readout Unit (RU) has been finished
  - Transfer data and control signals from/to staves
  - FPGA implemented GBT protocol
  - Protection from SEU based on logic scrubbing, with a flash based FPGA
  - Power supply from VME backplane

- Laboratory test and beam test
  - Input 400 MHz, ouput 5 Gbps, BER (bit error rate) $< 10^{-12}$
  - SEU events can always be detected and self-recovered.



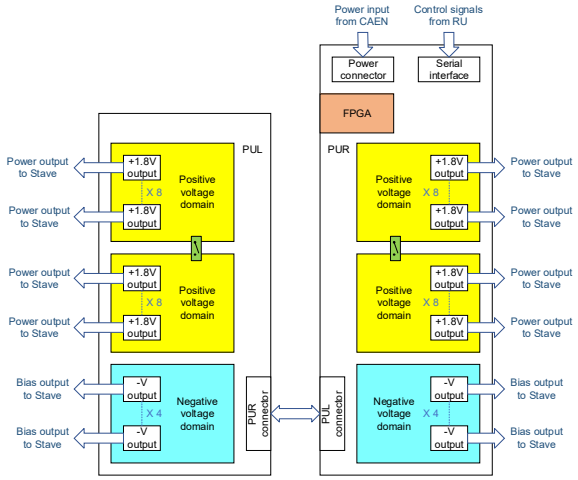


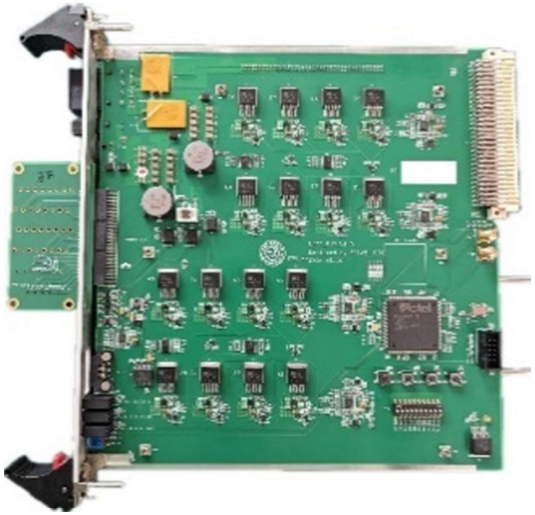


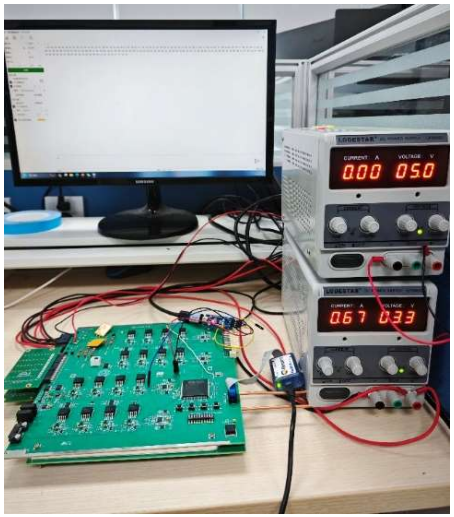
Courtesy of Prof. Lei Zhao (USTC)

Power Unit (PU) design by USTC

- The design of Power Unit (PU) has been finished
  - A power board (PB) consists of two independent PUs (PUR and PUL)
  - Each PU contains 8 channels of analog output (1.8V/250mA) and 8 channels of digital output (1.8V/1.5A)
  - A flash FPGA on PUR controls both PUR and PUL and is responsible for communication with RU
  - Real-time compensation for the voltage drop in power cable
- All desired functions have been tested in the laboratory successfully





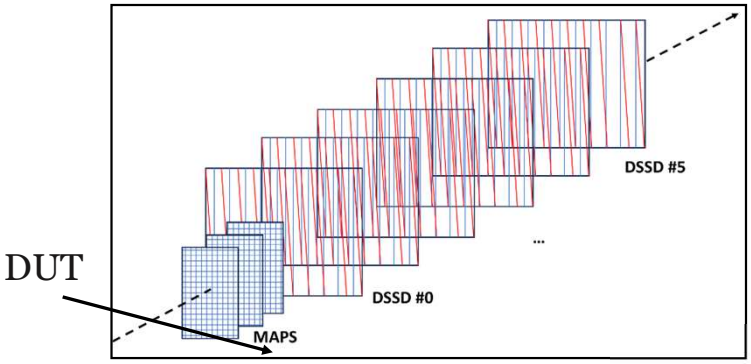


Preparations for the in-beam tests in Protvino and Gatchina

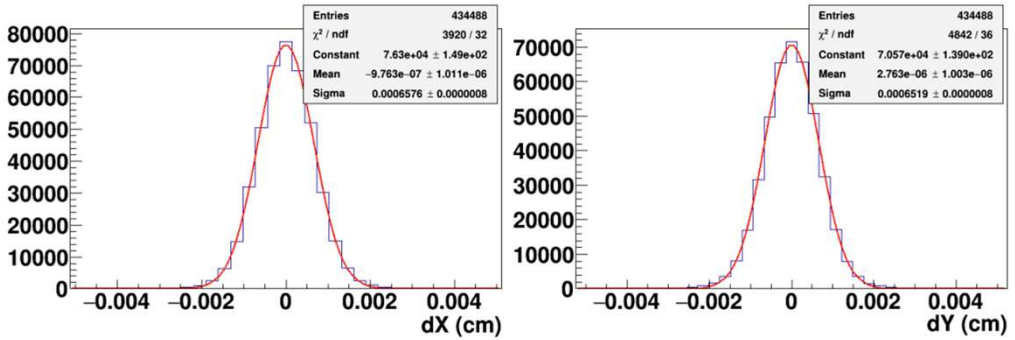
MPD ITS

NICA

Tests with 1 GeV proton beam in Gatchina

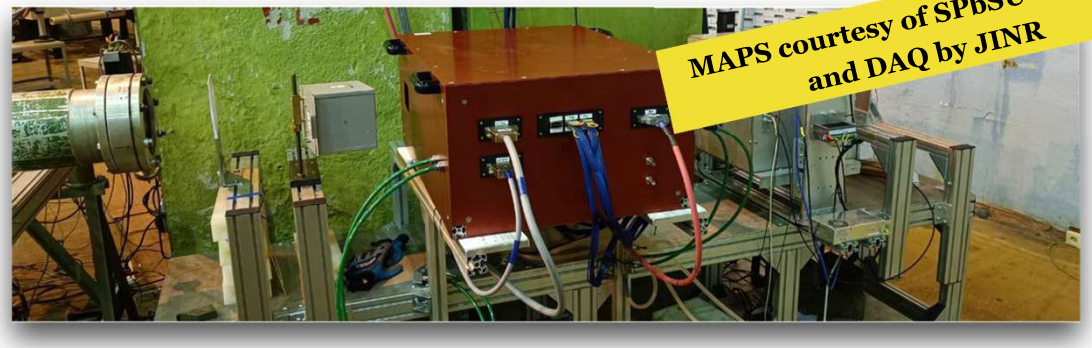


Residuals



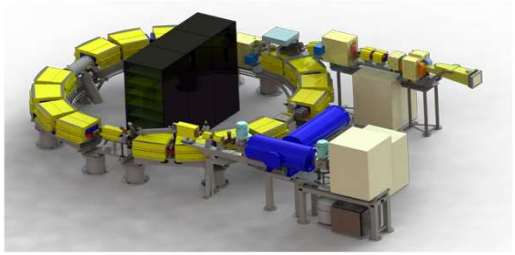
Residual X/Y = 6.58 um / 6.52 um;

Spatial resolution X/Y = 4.1±0.4 um /4.06 ± 0.4 um;,Efficiency > 99 %



MAPS courtesy of SPbSU readout and DAQ by JINR

Anticipated tests in Protvino with 150 – 300 MeV protons



PROTOM Ltd.

D.Dementiev,R.Arteche, M.Shitenkov,V.Leontiev, V.Kolazhvari

Working together for NICA MPD ITS

- **In order to further cooperate between JINR and Chinese institutions, the "NICA MPD-ITS Consortium" has been established:**
  - The acting time for the consortium is 5 years;
  - The coordinator center within the Russian Federation will be the JINR and in China will be the CCNU
  - The other institutions participating in the Consortium will have each one representative on the project structure for decision making and control.

Conclusions and lookout

- The MPD ITS in full configuration requests a considerable effort of the accelerator division to reduce the beampipe diameter to 40 mm and the length of the interaction diamond to 30 cm. Installation of the IB and additional 12 staves of OB calls for exchange of the FFDs for modern up-to-date technical solution of ATLAS HGTD with LGAD sensors developed for the HL-LHC. Expected date of completion 2030?

- The MPD ITS in “OB-only” configuration (42 staves in three layers) will be finalized in 2028 provided

- the MICA chip serial production will start in 2027 which seems to be feasible.

- Computer simulations and discussion of the physics cases to exploit first with TPC-ITS(OB) tracking system shall to continue.

Credits and Thanks

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