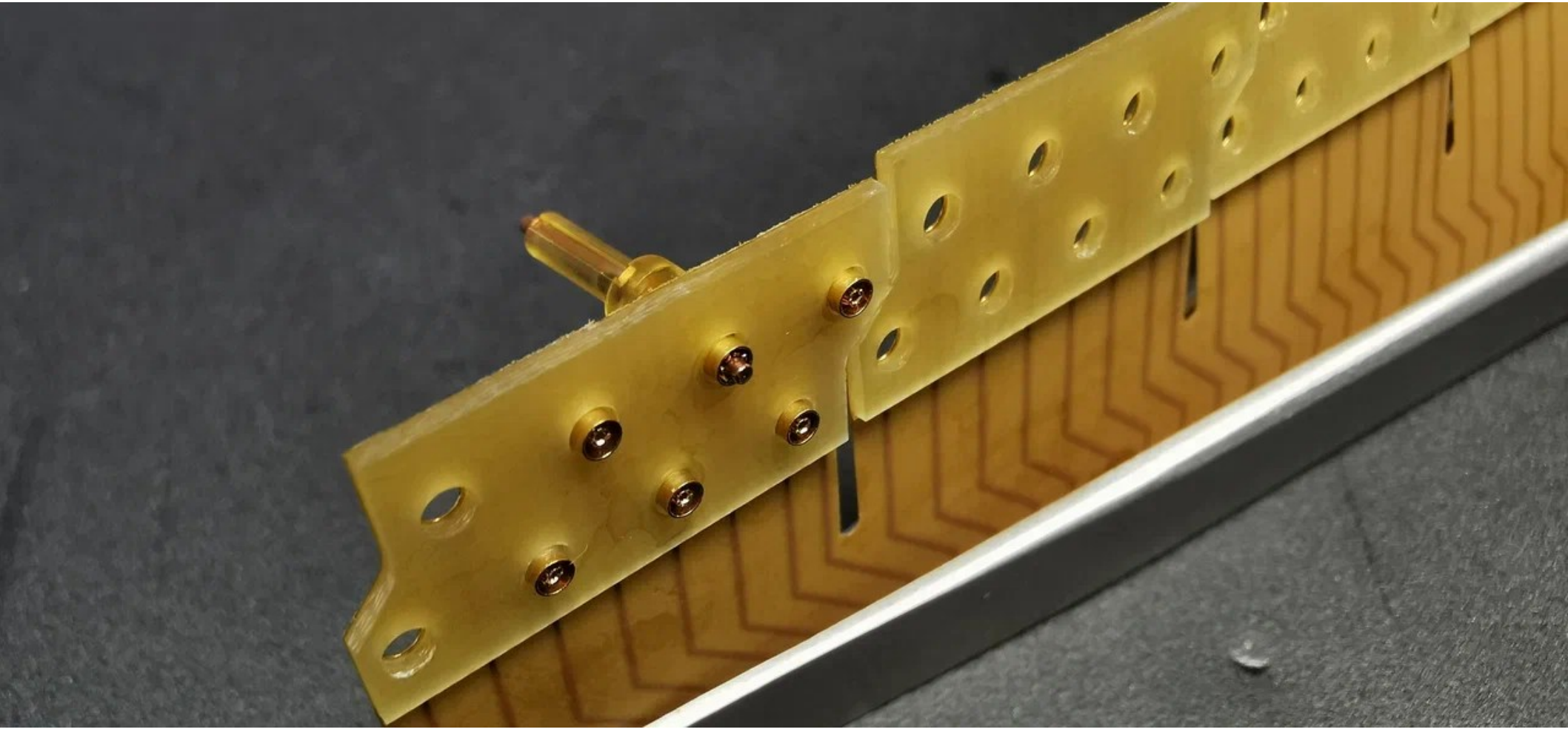
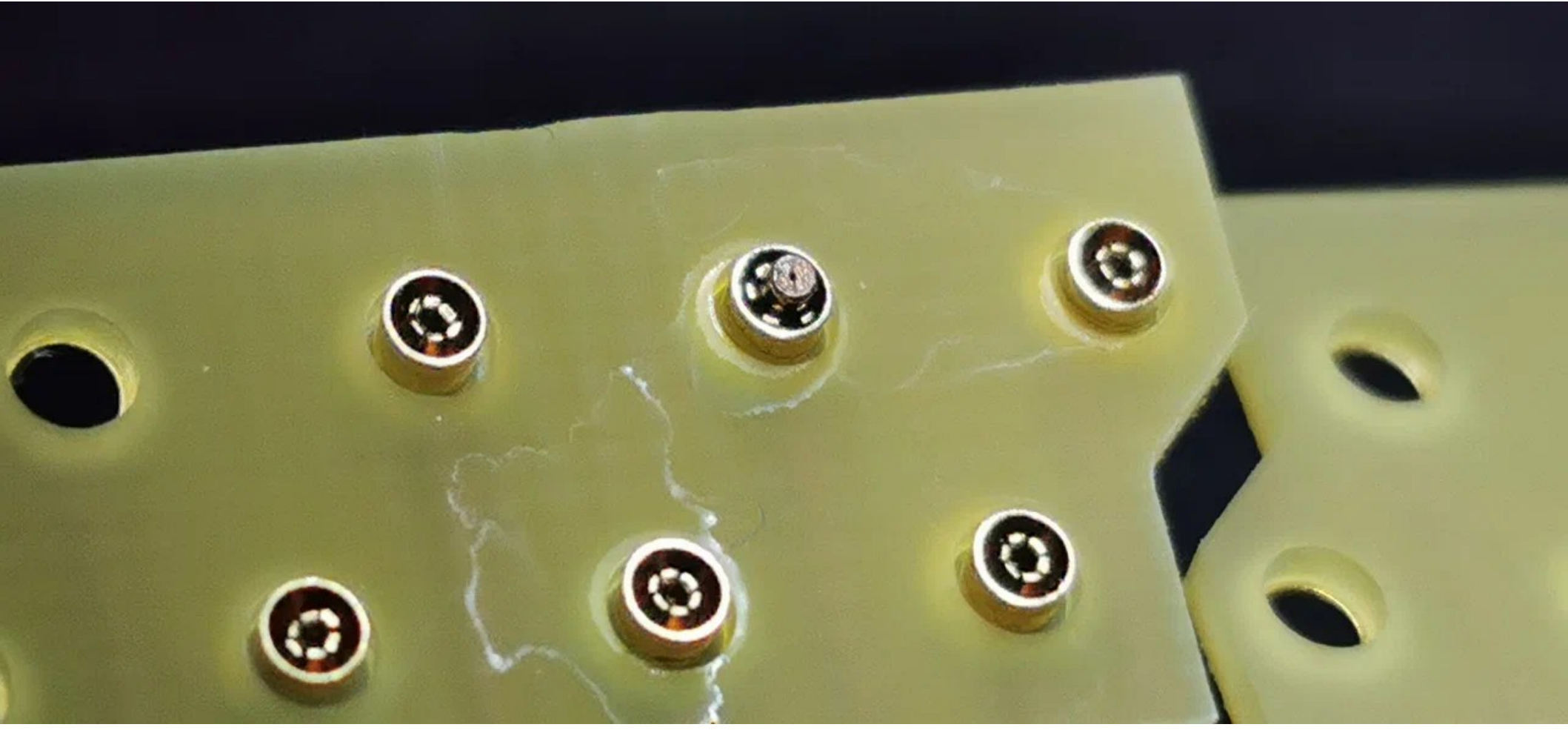
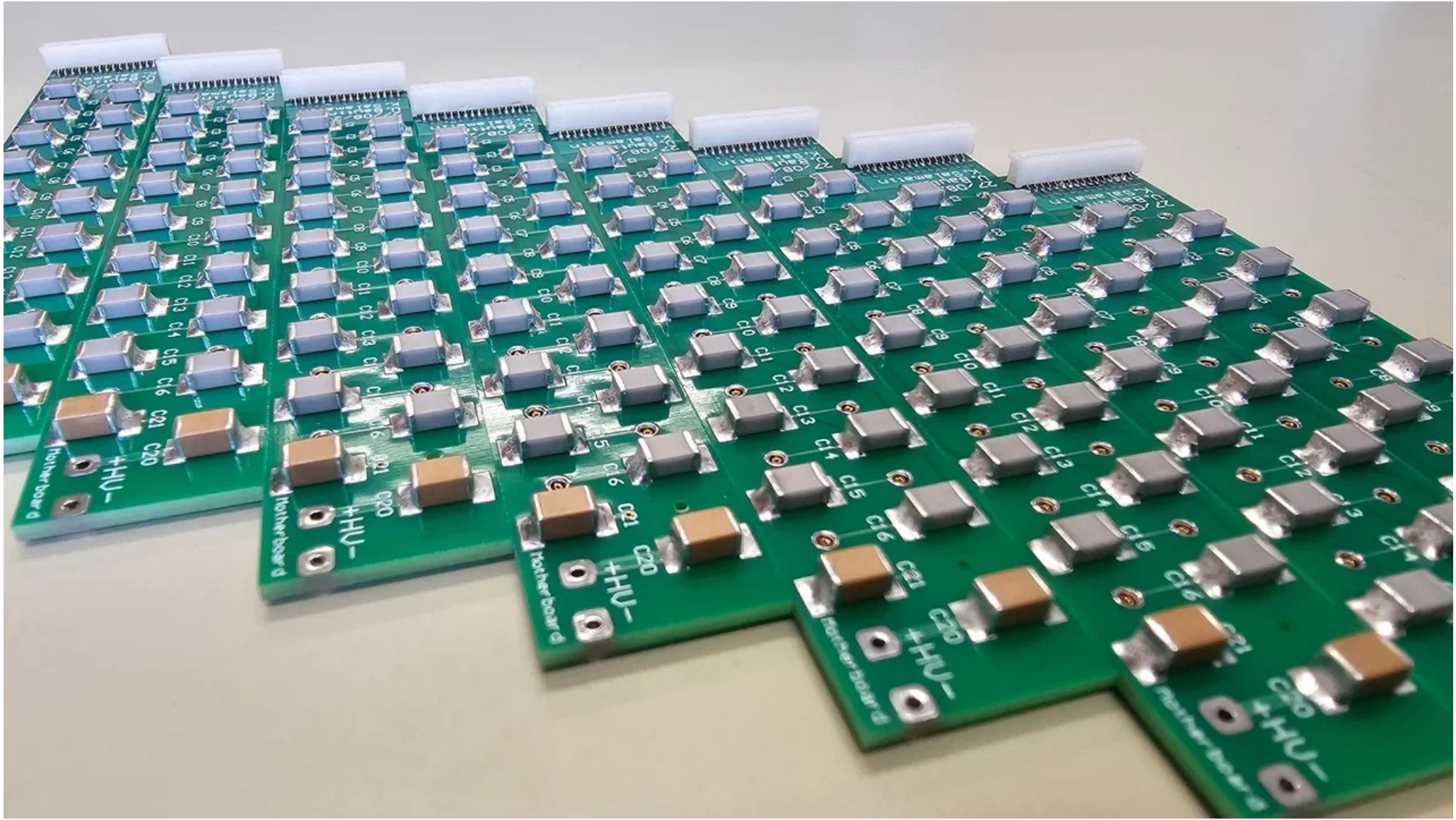
Update on SPD FEE

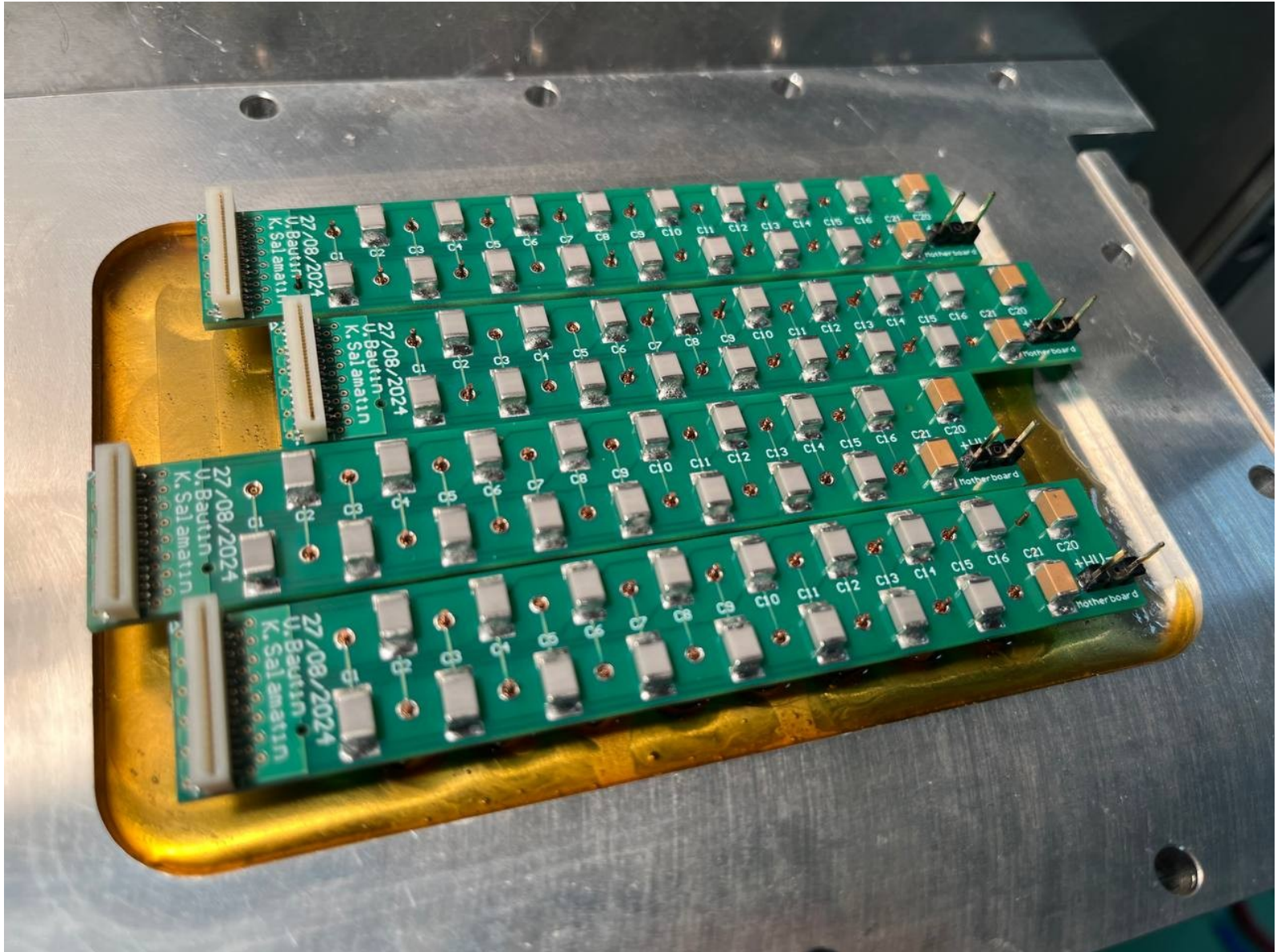
Vitalii Bautin
20 MAR 2025
for the Straw Team

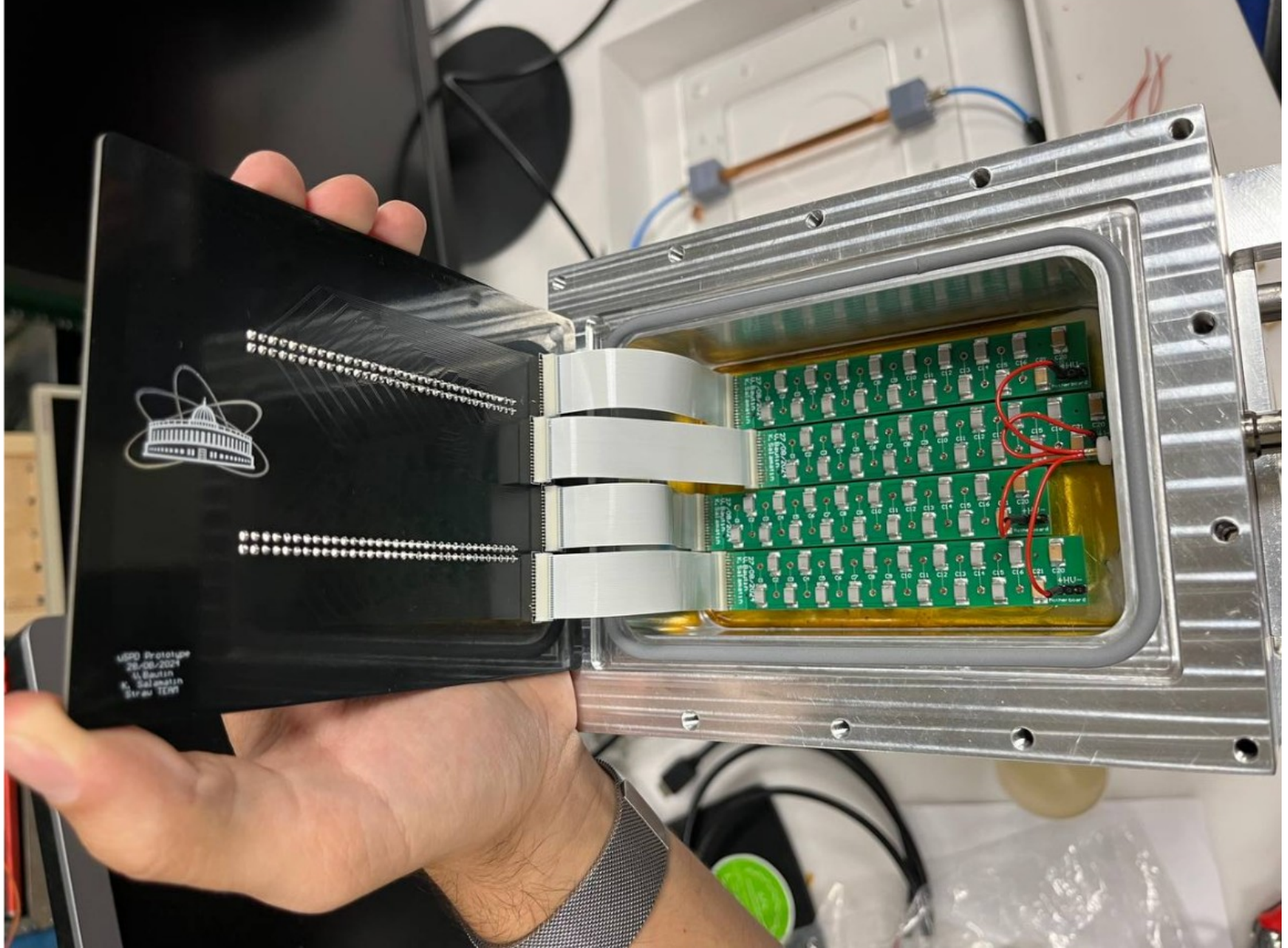
On-Chamber Motherboards





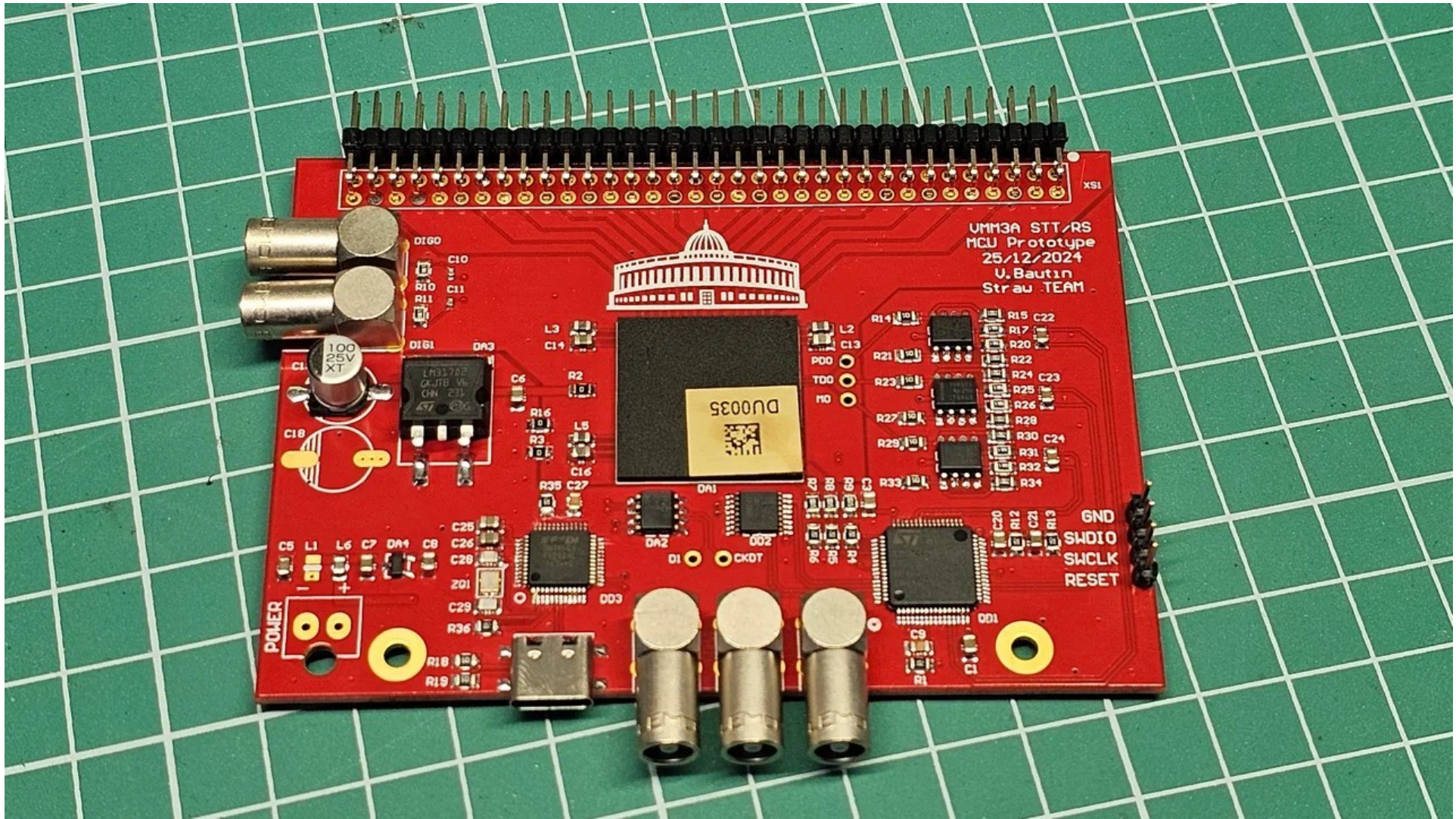

+HV-
Motherboard


27/08/2024
V.Bautin
K.Salamatin
Mother board

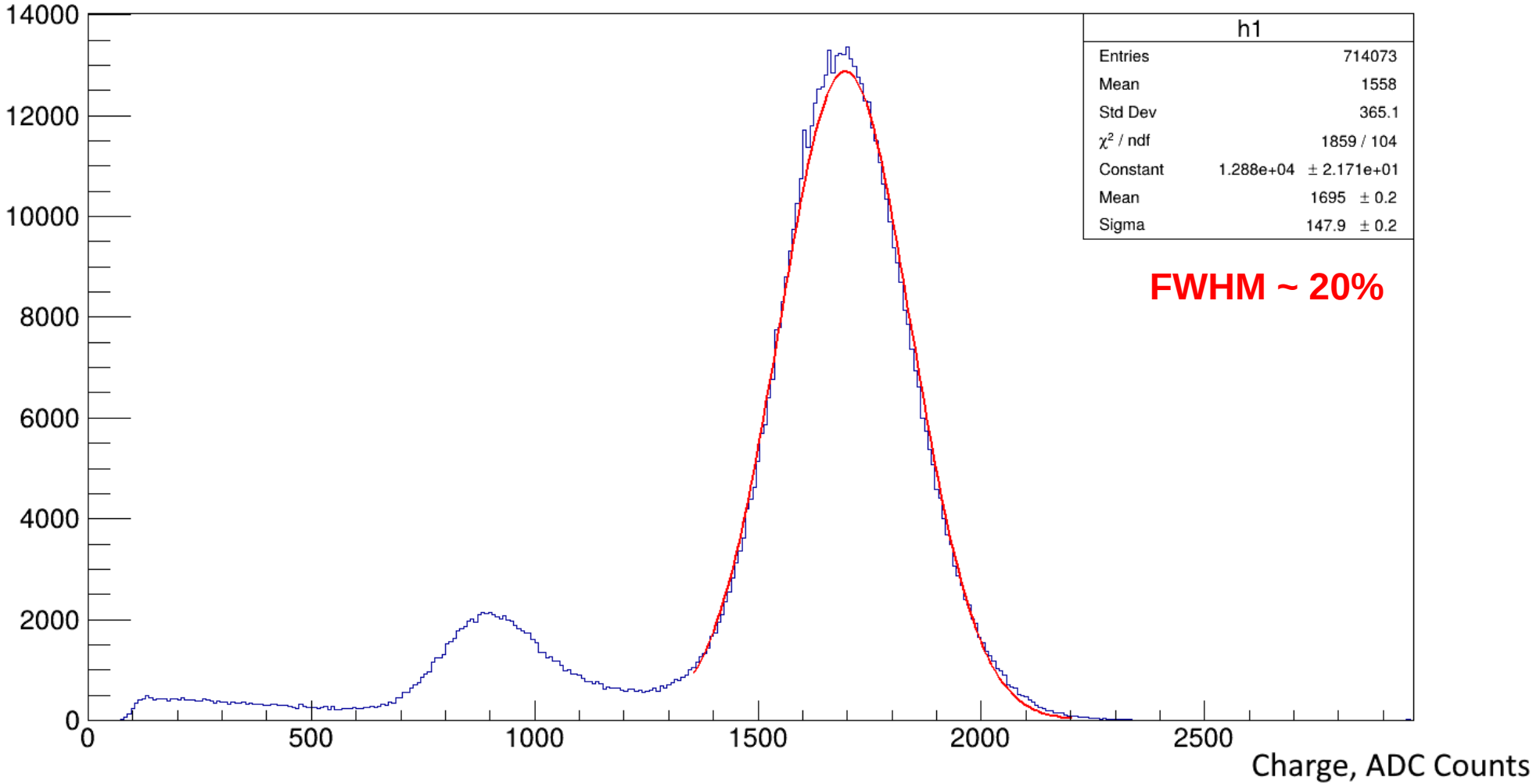

uRPD Prototype
28-08-2024
U.Bautin
K. Salamatin
Straw TEAM

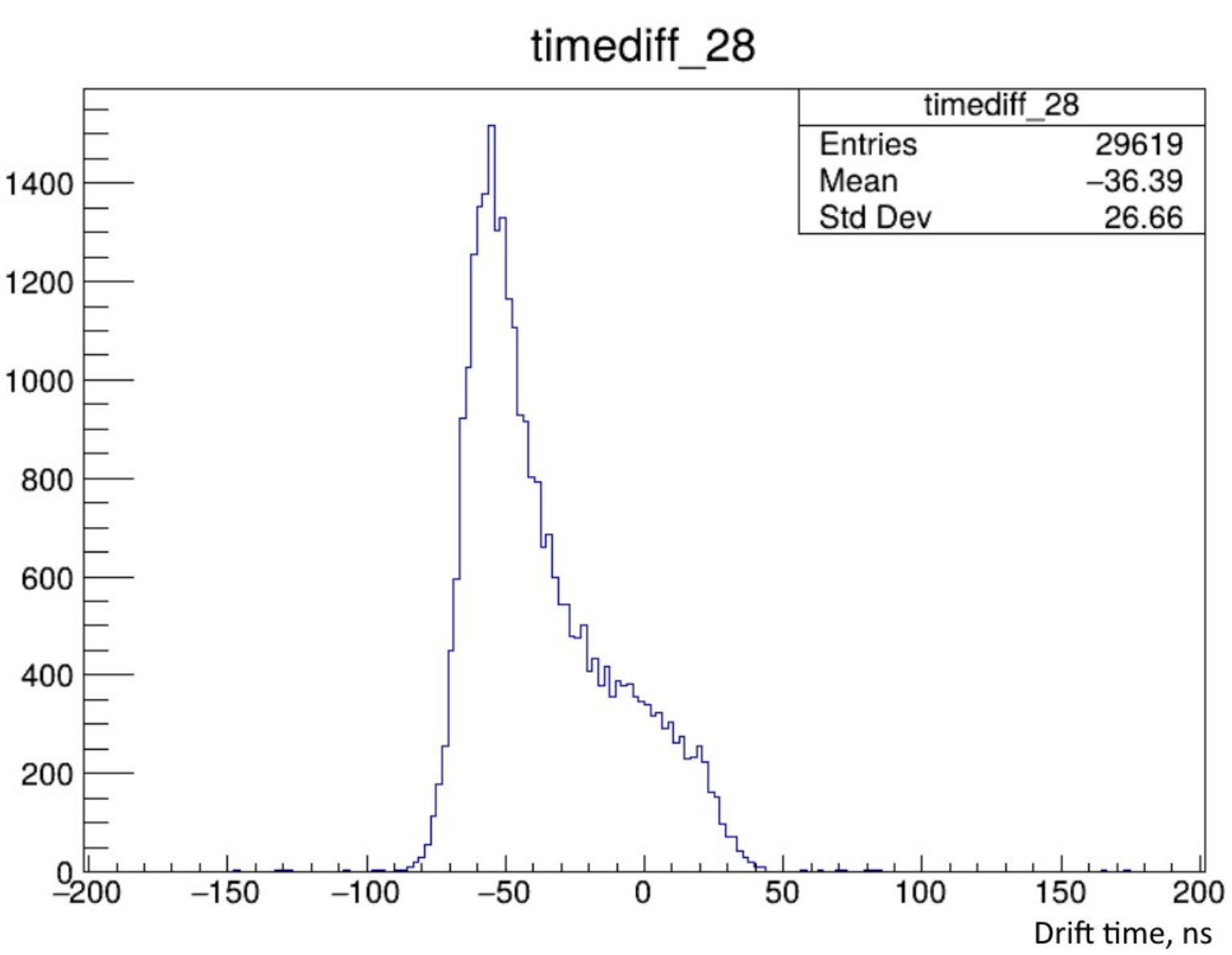
VMM3a FEE Prototype

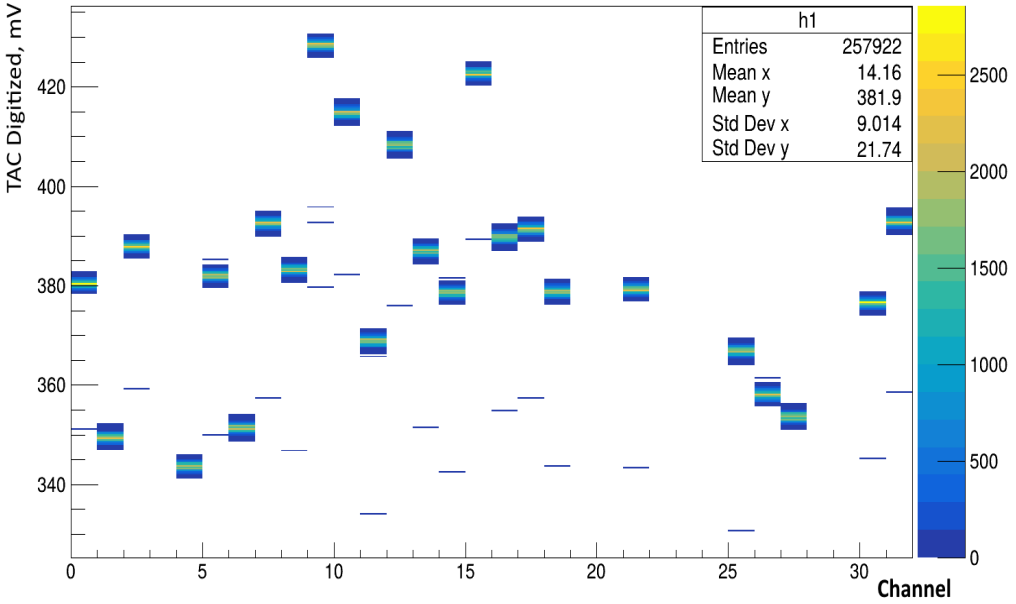
VMM3A FEB designed

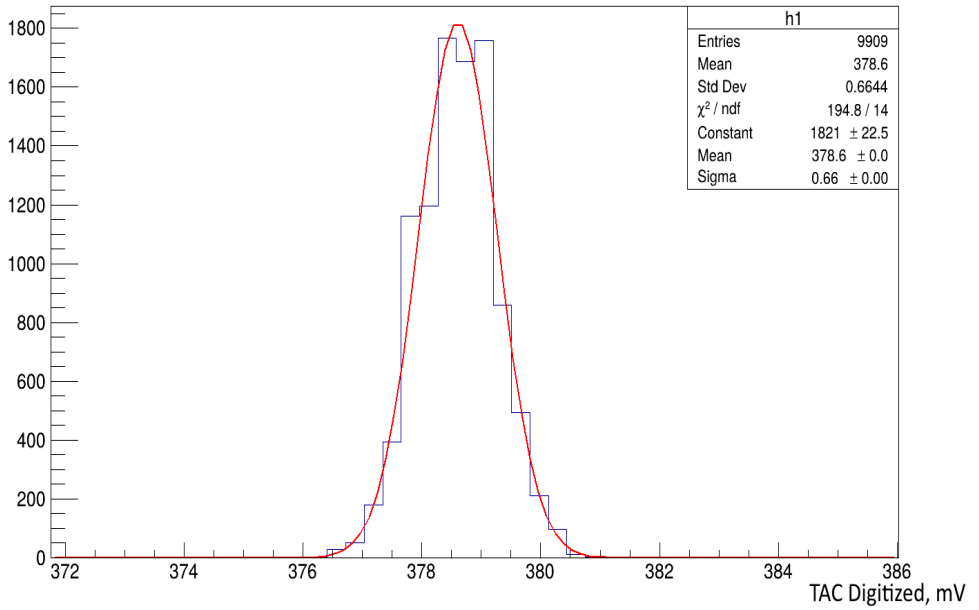


Fe55 Source, Ar/CO2 70:30 Mixture




timediff_28
timediff_28
Entries 29619
Mean −36.39
Std Dev 26.66
1400
1200
1000
800
600
400
200
0
−200
−150
−100
−50
0
50
100
150
200
Drift time, ns



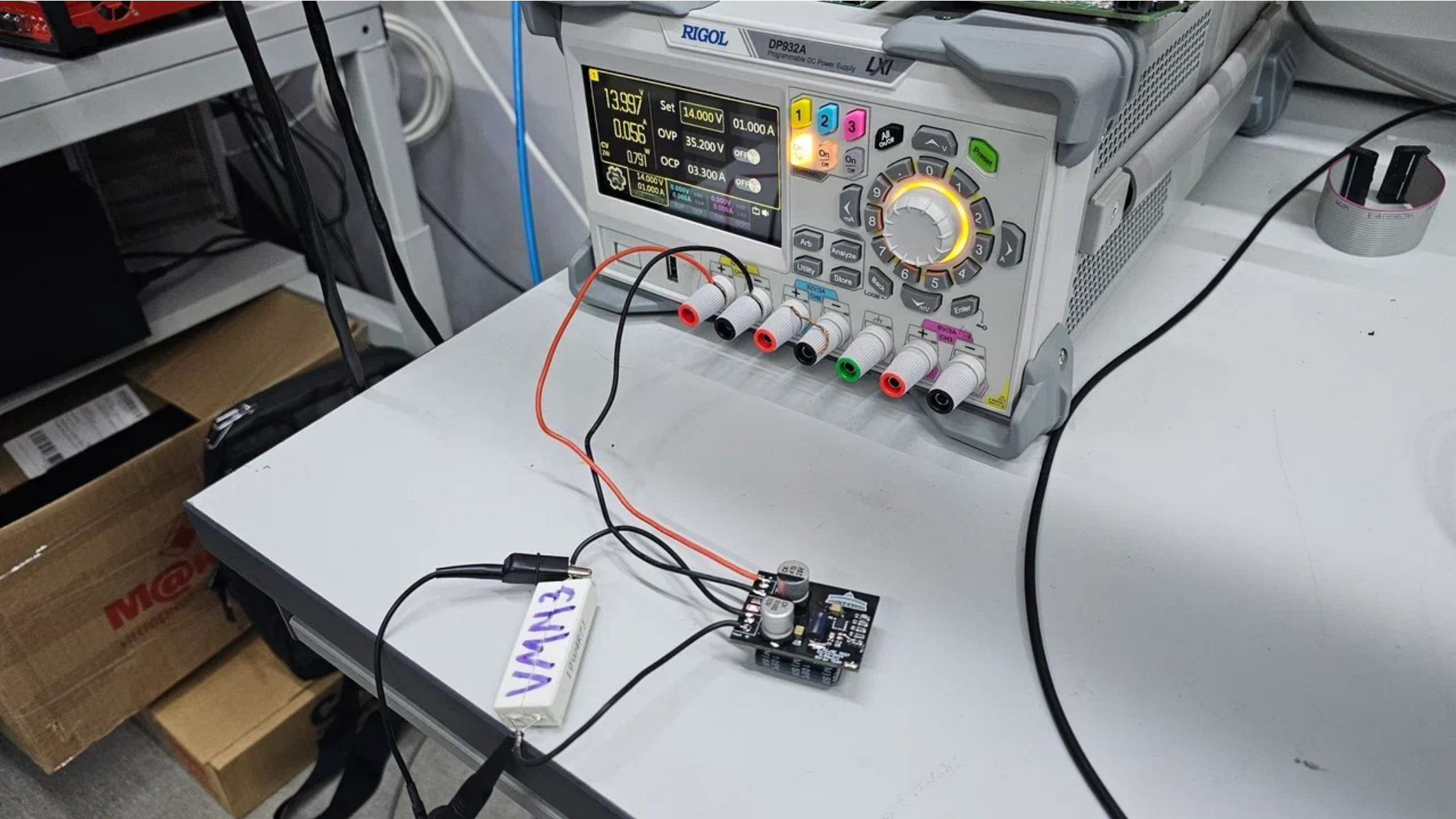


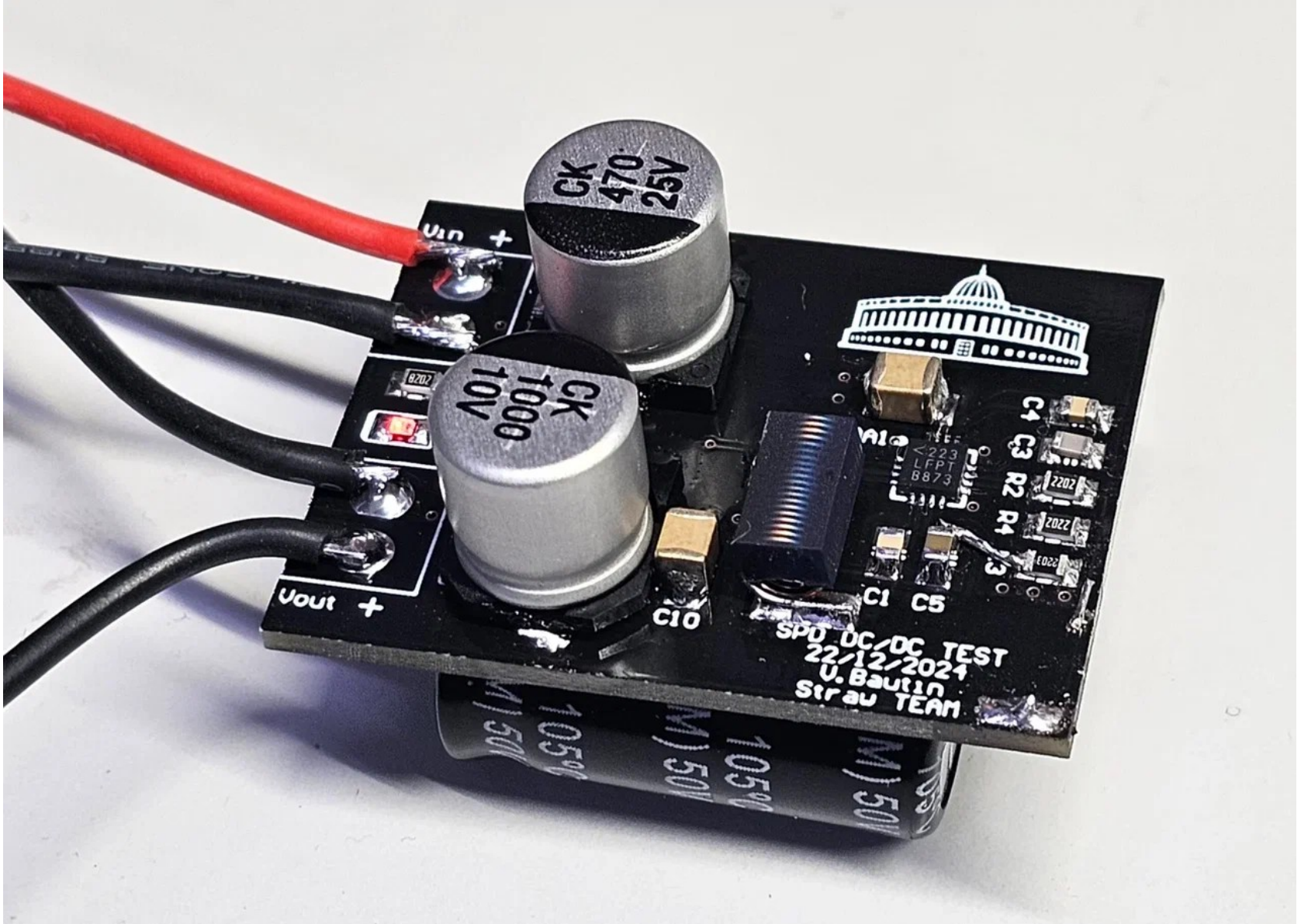
Timing resolutions obtained from a readout board equipped with VMM3a, MCU, and differential drivers for the internal ADC of the MCU with test pulses (300 fC) and different TAC slopes.

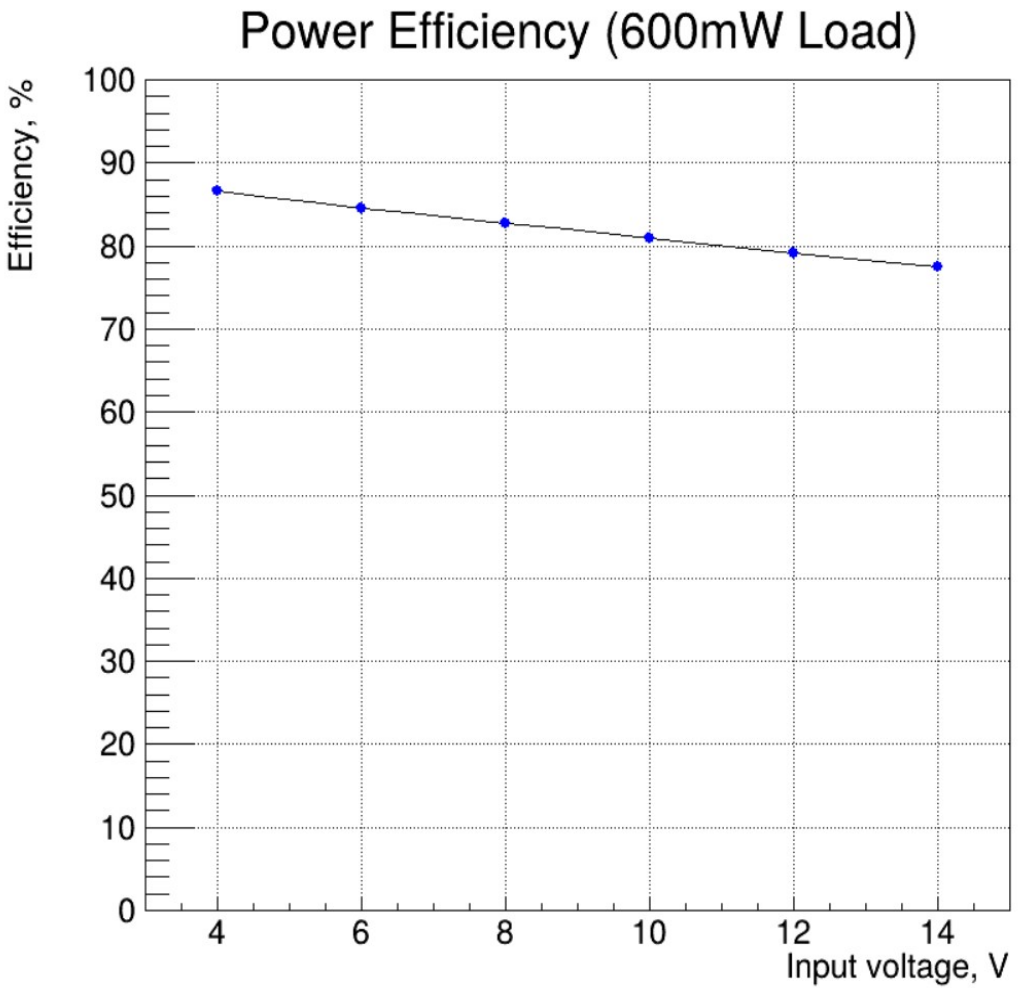
	TAC slope 100 ns	TAC slope 350 ns	TAC slope 650 ns
Slew rate	10 V/μs	2.8 V/μs	1.5 V/μs
Bin size	30 ps	110 ps	200 ps
Timing resolution	70 ps	230 ps	440 ps

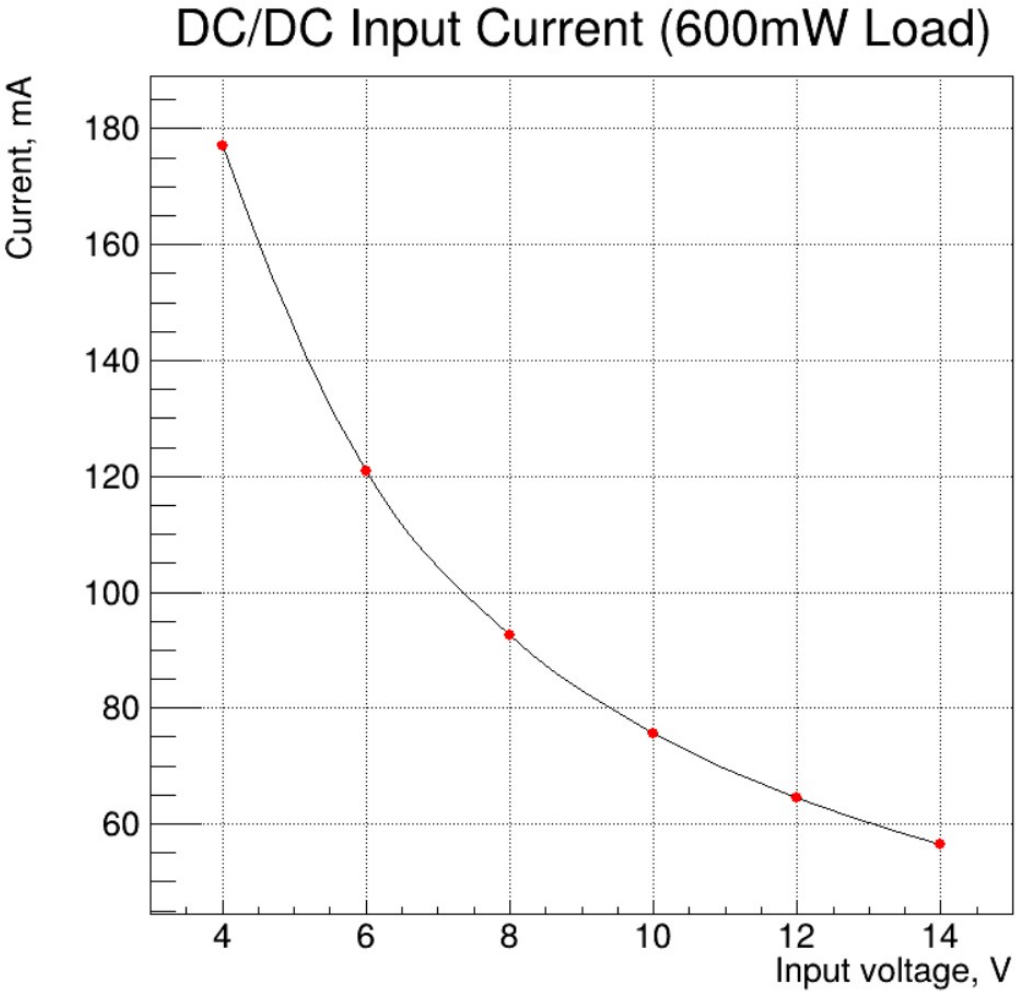
Extremely Preliminary

DC/DC with Magnetic Field

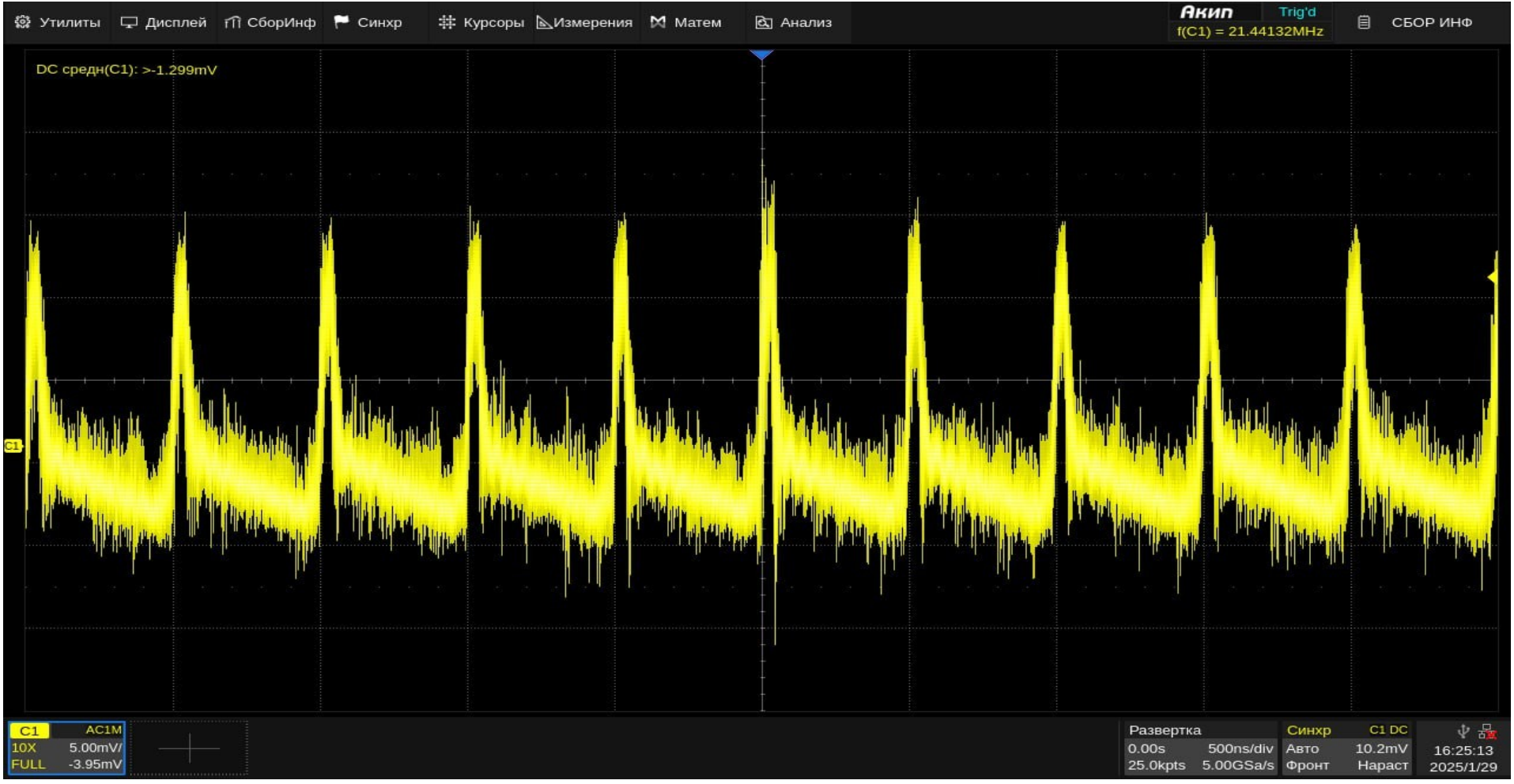

RIGOL
DP932A
Programmable DC Power Supply
LXI
13.997
0.056
0.791
Set
14.000 V
01.000 A
OVP
35.200 V
OCP
03.300 A
VMN3


CK
470
25V
CK
1000
10V
Vin +
Vout +
C10
C1 C5
C4 C3 R2 R1
SPD DC/DC TEST
22/12/2024
V. Bautin
Strau TEAM



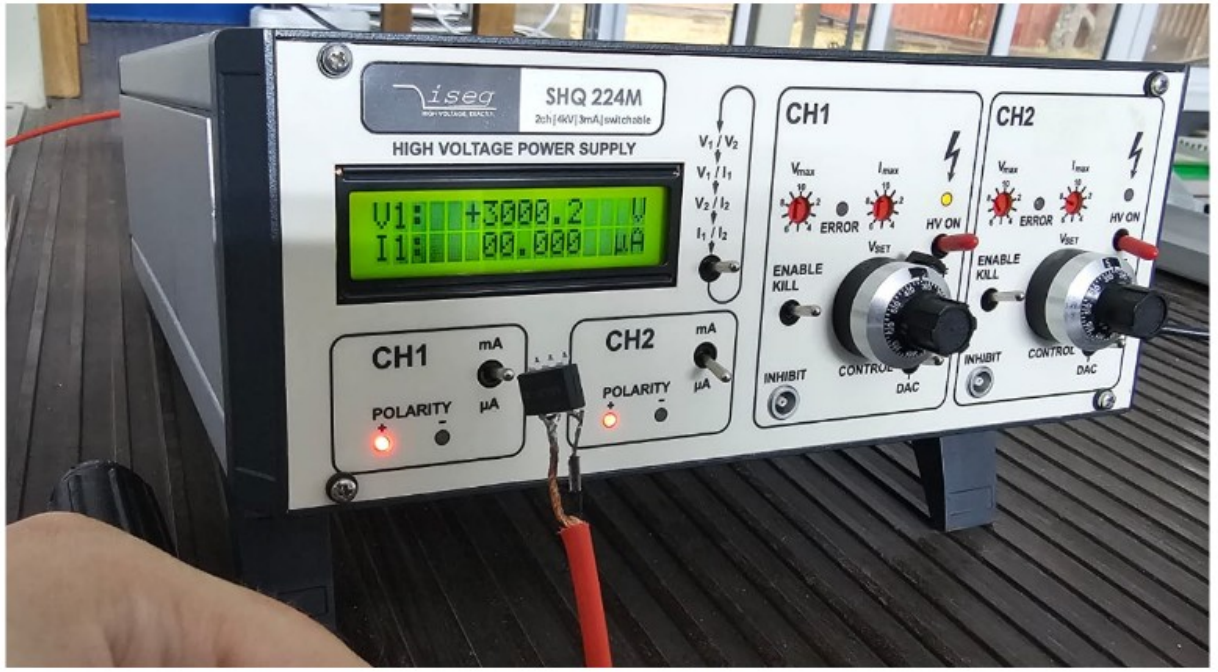


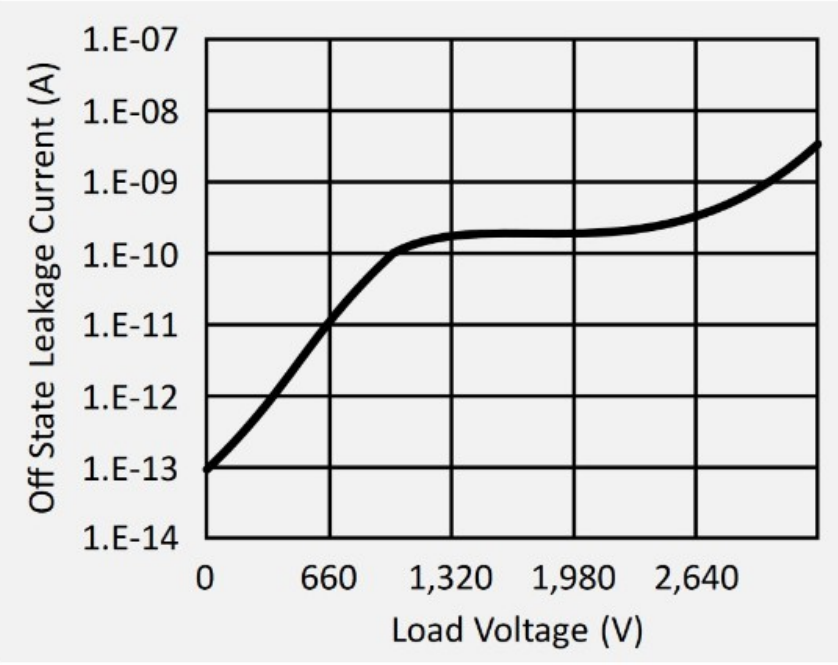
Without DC/DC VMM3a consumption is 600mW @ 1.2V (500mA)



20mVpp pulsations so far. To be improved

HV Segmentation





Tests of the solid state relay for the STT readout boards at 3000 V