Neutron Radiation Effects on the Reliability of the Cyclone V FPGA Development Board

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***Agenda Item: Radiation Testing of Cyclone V FPGA Using* DE0-Nano SoC Development Board.**

Objective: Evaluate the performance and stability of Cyclone V FPGA under neutron irradiation, as used in the Time Projection Chamber (TPC) of the Multi-Purpose Detector (MPD).

Test Platform: DE0-Nano SoC Development Board, controlled via Verilog-based QUARTUS firmware.

Irradiation Site: JINR FRANK and Neutron Laboratories, Use of shielding materials to protect components except the FPGA.

Key Focus Areas on DE0-Nano SoC Development Board.

- Data transmission stability and firmware efficiency under radiation.
- Impact of radiation on power modules and ARM processor performance.

Radiation Analysis:

- Assessment of FPGA logic errors and power reliability post-irradiation.
- Fluence estimation using silicon sensors measuring leakage current due to irradiation damage.

Introduction

TPC Overview

The **Time Projection Chamber (TPC)** is the **main tracking detector** in the **Multi-Purpose Detector (MPD)** at the **NICA** collider.

It tracks **charged particles** produced in **nucleus-nucleus collisions**, providing precise spatial and momentum information.

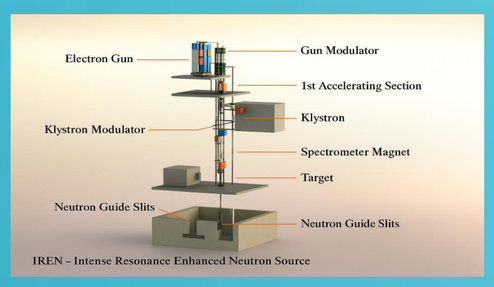
Irradiation Process for the Electronic Kit Utilizing the IREN Accelerator

IREN (Intense Resonance Neutron Source)

- Located at JINR, IREN is a pulsed neutron facility.
- Designed to produce high-intensity neutron bursts through nuclear reactions.
- Supports research in nuclear physics, neutron spectroscopy, and materials science.

Neutron-Producing Target Design

- Cylindrical TNF target: 40 mm (diameter) × 100 mm (height)
- Enclosed in a 160 mm diameter aluminum tank.



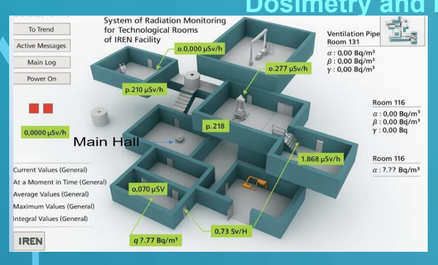
Neutron Production Mechanism

- Target material: Tungsten-based alloy (VNZh-90) with non-multiplying properties
- Reaction type: A W (γ, n) A–1 (neutron emission from tungsten isotopes)

Two-step neutron generation process:

1. High-energy electrons produce bremsstrahlung gamma rays upon hitting the target
2. Gamma rays interact with tungsten nuclei, generating neutrons via (γ, n) reactions

Dosimetry and Radiation Monitoring



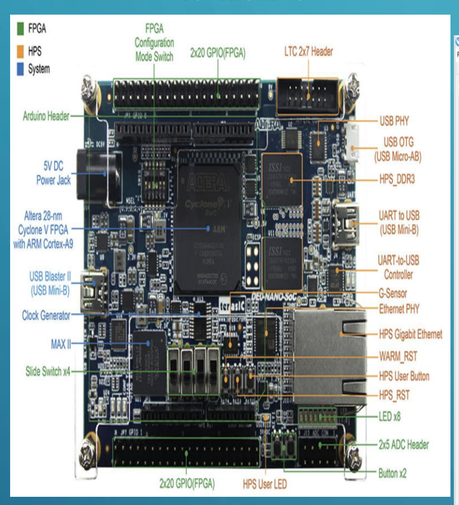
Dosimetry screen showing radiation levels after the exposure period ended for the KIT board, taken in the main hall and technical rooms of the IREN Facility, with the primary irradiation unit powered off.

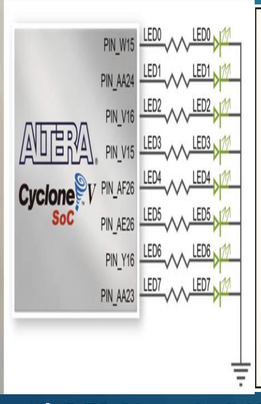
- Broad neutron energy range: thermal to fast neutrons
- Fast neutron energy: **20–30 MeV**
- During KIT board irradiation: flux was **~10^7 n/cm²·s**

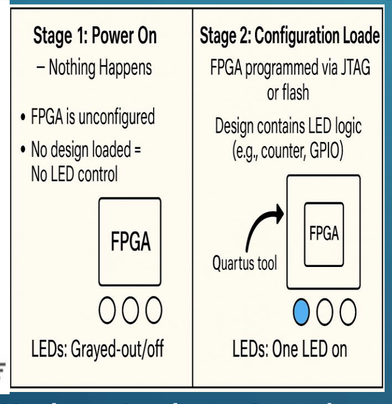
Methodological

Radiation Testing of FPGA-Based Readout System

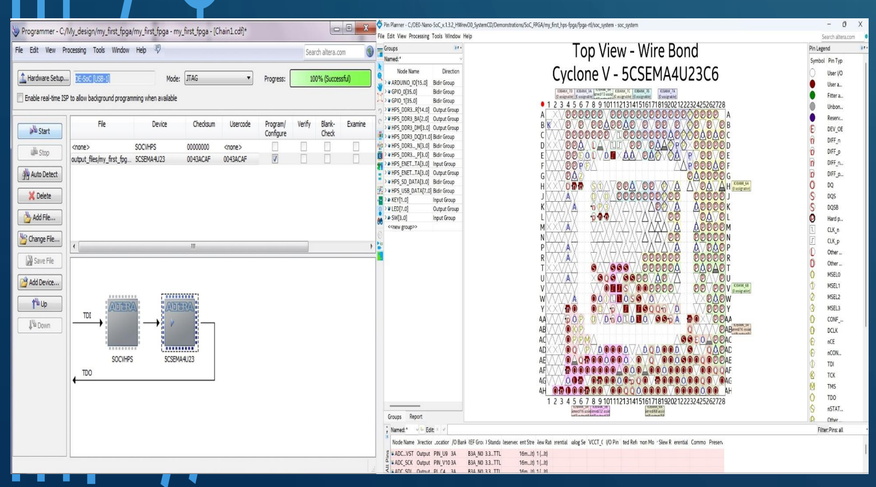
- A **DE0-Nano SoC development board** with a **Cyclone V FPGA** was used as a test platform, chosen for its similarity to the TPC readout electronics.
- The board was **exposed to neutron irradiation** at the **JINR FRANK** and **FLNP Neutron Laboratories.**
- **Remote operation** was enabled using **custom Quartus firmware** developed in **Verilog HDL.**
- During irradiation, **data transmission stability** was continuously monitored to evaluate **FPGA performance under radiation.**



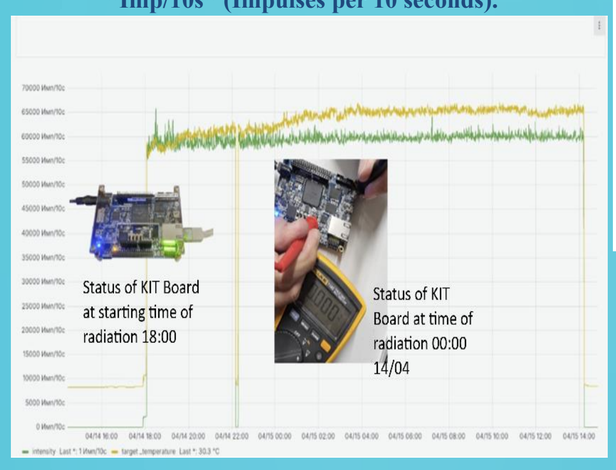




Quartus Integration with DE0-Nano SoC Kit during Irradiation Procedure.



Neutron flux intensity indicators over the irradiation period for the Deo Nano SoC KIT board " Имп /10с" → "Imp/10s" (Impulses per 10 seconds).

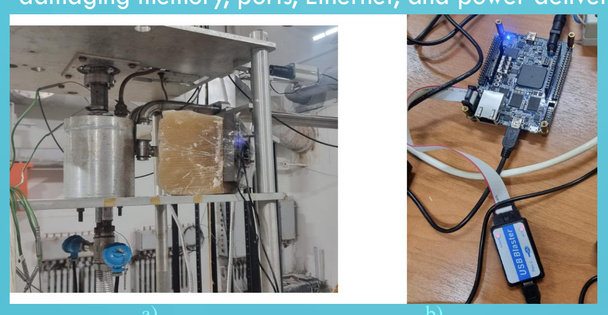


Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.

The DE0-Nano SoC kit's functionality was validated using Verilog, with PC-to-FPGA communication established via USB Blaster and JTAG.

Quartus software served as both a remote-control and simulation tool using Verilog code from earlier tests.

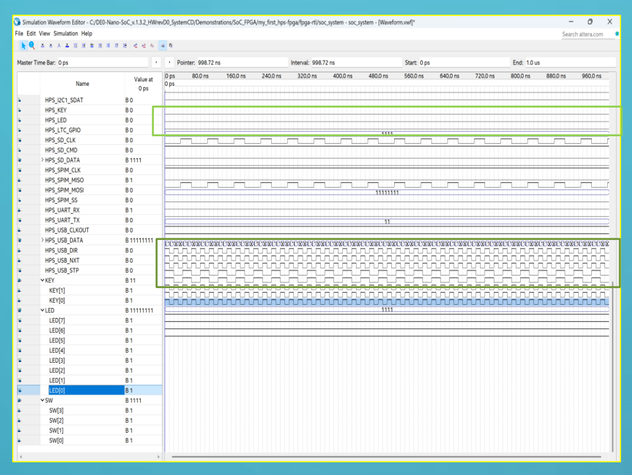
Results show that irradiation from the IREN Accelerator disrupted the DE0-Nano SoC kit's power system, damaging memory, ports, Ethernet, and power delivery.

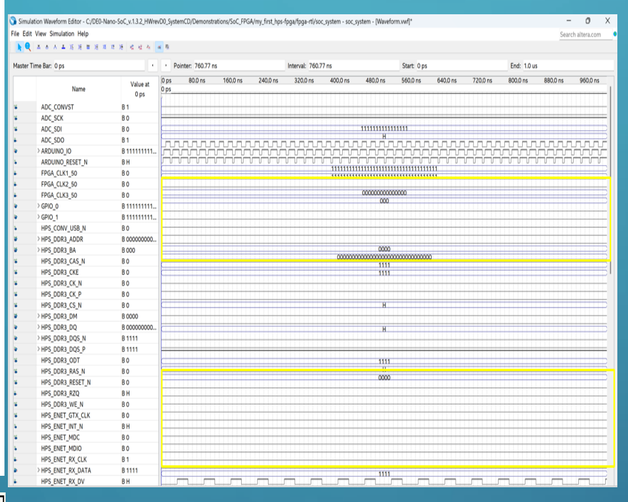


a) b)

Irradiation setup using the IREN Accelerator (a). DE0-Nano SoC kit successfully connected to PC via USB Blaster for Verilog-based testing (b)

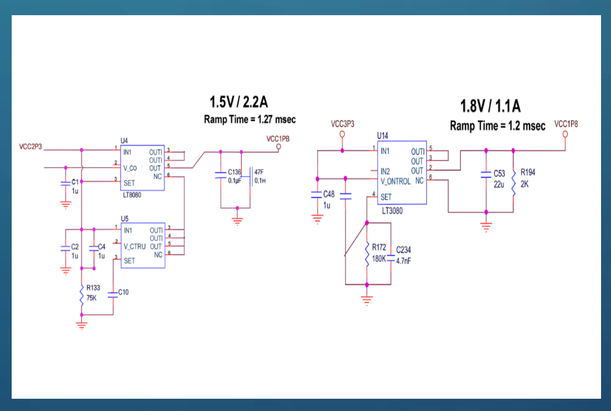
Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.





Voltage readings and schematics reveal that the DE0-Nano SoC kit's power regulation circuits for the HPS DDR3 and FPGA are malfunctioning.

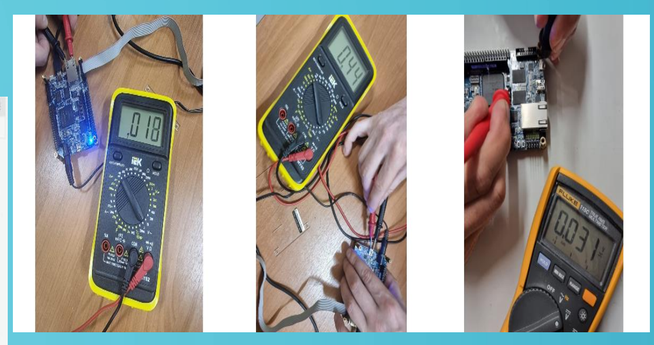
This disruption in power distribution likely resulted from irradiation exposure in the IREN Accelerator.



a) b)

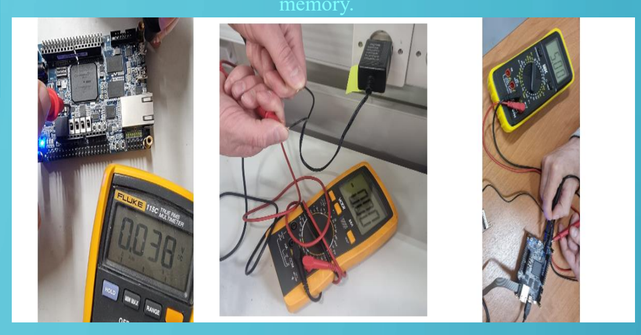
Power supply scheme for the electronic circuit, detailing the voltage regulation for (a the HPS DDR3 memory and b) the FPGA processor.

Irradiation of the DE0-Nano SoC Kit using the IREN Accelerator caused ionization effects, leading to voltage and current fluctuations in its 5V/2A power network. These disruptions resulted in malfunctions of key components, including the HPS_DDR3 memory, UART-to-USB, USB Blaster II, and the Ethernet port (Figure a–c).



a) b) c)

Radiation-induced disruptions affecting key components — (a) Ethernet port, (b) UART to USB interface, and (c) HPS_DDR3 memory.



a) b) c)

a) Radiation-induced disruption in power delivery to the FPGA: instability in the +1.2 V supply to the processor due to irradiation effects on voltage regulation, (b) damaged external 5V/2A power supply, and (c) its power input connection of 5V.

Irradiation Setup for the DE0-Nano SoC Kit Using the EG-5 Accelerator

Radiation Exposure Setup at JINR

- **Neutron irradiation** was carried out at the **Neutron Physics Laboratory** of the **Joint Institute for Nuclear Research (JINR),** using neutrons generated by the **EG-5 electrostatic accelerator.**
- The neutron-producing reaction was: **Li (d, n) ^{8}Be**

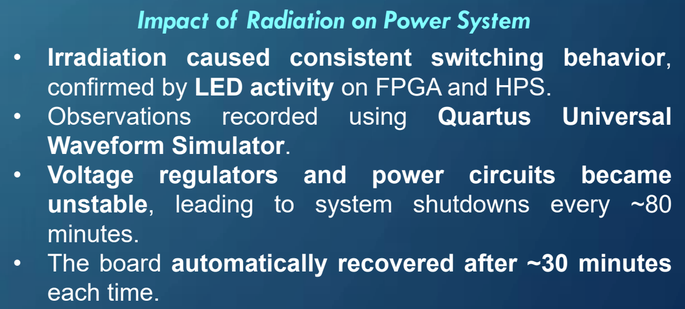
Irradiation Schedule

- **April 3rd:** 11:00 AM – 5:00 PM
- **April 4th:** 10:00 AM – 5:00 PM

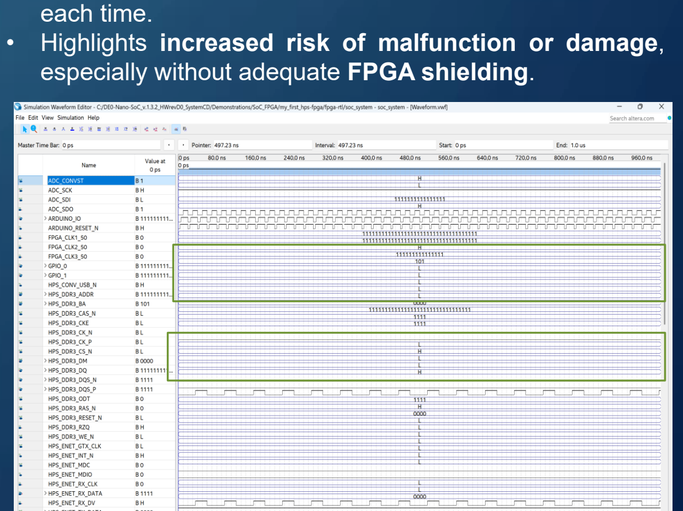
Total Exposure Duration

- Approx. **10 hours and 40 minutes** total exposure

Estimated neutron flux: **0.5 × 10^7 n/cm²·s~30% of neutrons** had energies near **14 MeV,** suitable for testing radiation effects on electronics.



Shielding of the Deo Nano SOC KIT Board



a) installation of the EG5 accelerator's third channel to expose the electronic kit board for neutron radiation source.

b) Connect the kit board for the FPGA Cyclone V to the power supply and make the connection between the kit board and the personal computer using UART to USB (USB MINI-B) Cable to remote control the kit while being irradiated.

c) two layers of Borated polyethylene and Cadmium.

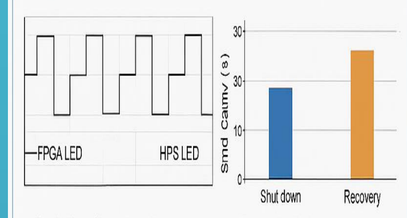
d) shielding materials consist of three layers of (Borated polyethylene, Paraffin, and Cadmium).

Impact of Radiation on Power System

- **Irradiation caused consistent switching behavior**, confirmed by **LED activity** on FPGA and HPS.
- Observations recorded using **Quartus Universal Waveform Simulator**.
- **Voltage regulators and power circuits became unstable**, leading to system shutdowns every ~80 minutes.
- The board **automatically recovered after ~30 minutes** each time.
- Highlights **increased risk of malfunction or damage**, especially without adequate **FPGA shielding**.

The kit board temporarily stop functioning and then resume during irradiation due to radiation-induced transient faults, such as Single Event Upsets (SEUs) or Single Event Functional Interrupts (SEFIs). These effects can momentarily disrupt the FPGA's operation without causing permanent damage.

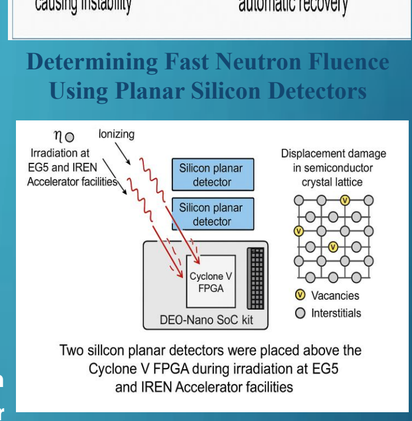
Experimental Results



Radiation disrupts voltage regulators and bower circuits, causing instability

- Each shuth down followed by a 30-minute automatic recovery

Determining Fast Neutron Fluence Using Planar Silicon Detectors



Two sillcon planar detectors were placed above the Cyclone V FPGA during irradiation at EG5 and IREN Accelerator facilities

Silicon detectors are sensitive to fast neutron irradiation.

- Radiation **damages silicon**, increasing its **reverse bulk (dark) current**.
- This **current increase** is proportional to:
  - **Neutron fluence (Φ)**
  - **Sensitive volume (V)** of the detector

Fluence Estimation Formula

$$\Delta I = \alpha \times \Phi \times V,$$

$$\Delta I = I - I_0 \text{ (A)}$$

- **I**: Post-irradiation dark current
- **I_0**: Pre-irradiation dark current
- Both measured at full depletion voltage and normalized to **+20 °C**

Parameter Definitions

Φ (cm^{-2}): 1 MeV-equivalent fast neutron fluence

α_I = (5 ± 0.5) × 10^{-17} A/cm:

- Current-related damage constant
- For 1 MeV neutrons at +20 °C (excluding self-annealing)

V = d × S (cm³):

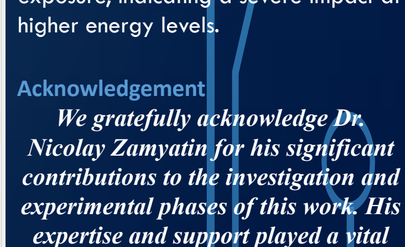
- Sensitive volume
- **d** = detector thickness (cm)
- **S** = active area (cm²)

Final Fluence Calculation

$$\Phi = \Delta I / (\alpha_I \cdot V),$$

By measuring **ΔI** and knowing **α_I**, **d**, and **S**, the neutron fluence **Φ (n/cm²)** can be accurately determined.

№ Silicon Detector	d, mm	S, mm²	I, n A (V = 100 V) (before irradiation)	I, n A (V = 100 V) (after irradiation)	ΔI, nA (V = 100 V)	$\Phi_{n,eq\ <1MeV>}$ /см²
№16	0.266	13	0.6	4.21	3.56	2.06×10^{10} Van de Graaff
№17	0.251	13	0.7	105	104	6.36×10^{11} Van de Graaff +IREN



Leakage current increases more rapidly and breakdown voltage decreases in silicon detectors irradiated with the IREN accelerator.

Conclusion

Radiation testing on **DE0-Nano SoC boards** was conducted at the **EG-5** and **IREN** facilities using two neutron energy setups.

- In **Setup 1** (~3 MeV neutrons), the **Cyclone V FPGA** remained functional for about **80 minutes** before experiencing **periodic shutdowns,** each followed by a **30-minute automatic recovery.** The exact cause of the shutdowns remains under investigation.
- In **Setup 2** (20–40 MeV neutrons), the board's **power system failed entirely** after approximately **4 hours** of exposure, indicating a severe impact at higher energy levels.

Acknowledgement

We gratefully acknowledge Dr. Nicolay Zamyatin for his significant contributions to the investigation and experimental phases of this work. His expertise and support played a vital role in the development and completion of this study.