Neutron Radiation Effects on the Reliability of the Cyclone V FPGA Development Board

Youmna Ghoneim [a,c*], Sergey Movchan [a], Ilya Chepurchenko [a], Rafael Isayev [a,b] , Kirill Mikhailov [a], konstantin Udovichenko [a].

a) *Joint Institute for Nuclear Research, 6 Joliot-Curie St., 141980 Dubna, Russia.*

b) *Innovation and Digital Development Agency, Baku, Azerbaijan.*

c) *National Research Tomsk Polytechnic University, 634050, Tomsk Russia.*

Agenda Item: Radiation Testing of Cyclone V FPGA Using DE0-Nano SoC Development Board.

Objective: Evaluate the performance and stability of Cyclone V FPGA under neutron irradiation, as used in the Time Projection Chamber (TPC) of the Multi-Purpose Detector (MPD).

Test Platform: DE0-Nano SoC Development Board, controlled via Verilog-based QUARTUS firmware.

Irradiation Site: JINR FRANK and Neutron Laboratories, Use of shielding materials to protect components except the FPGA.

Key Focus Areas on DE0-Nano SoC Development Board.

- Data transmission stability and firmware efficiency under radiation.
- Impact of radiation on power modules and ARM processor performance.

Radiation Analysis:

- Assessment of FPGA logic errors and power reliability post-irradiation.
- Fluence estimation using silicon sensors measuring leakage current due to irradiation damage.

Introduction

- The **Time Projection Chamber (TPC)** is the main tracking detector in the **Multi-Purpose Detector (MPD)** at the **NICA collider**.
- It tracks **charged particles** from **nucleus-nucleus collisions**.
- **Momentum** and **energy resolution** are defined by the TPC's design and the applied magnetic field.
- The baseline readout system uses a **Multi-Wire Proportional Chamber (MWPC)** with **cathode pad readout**.

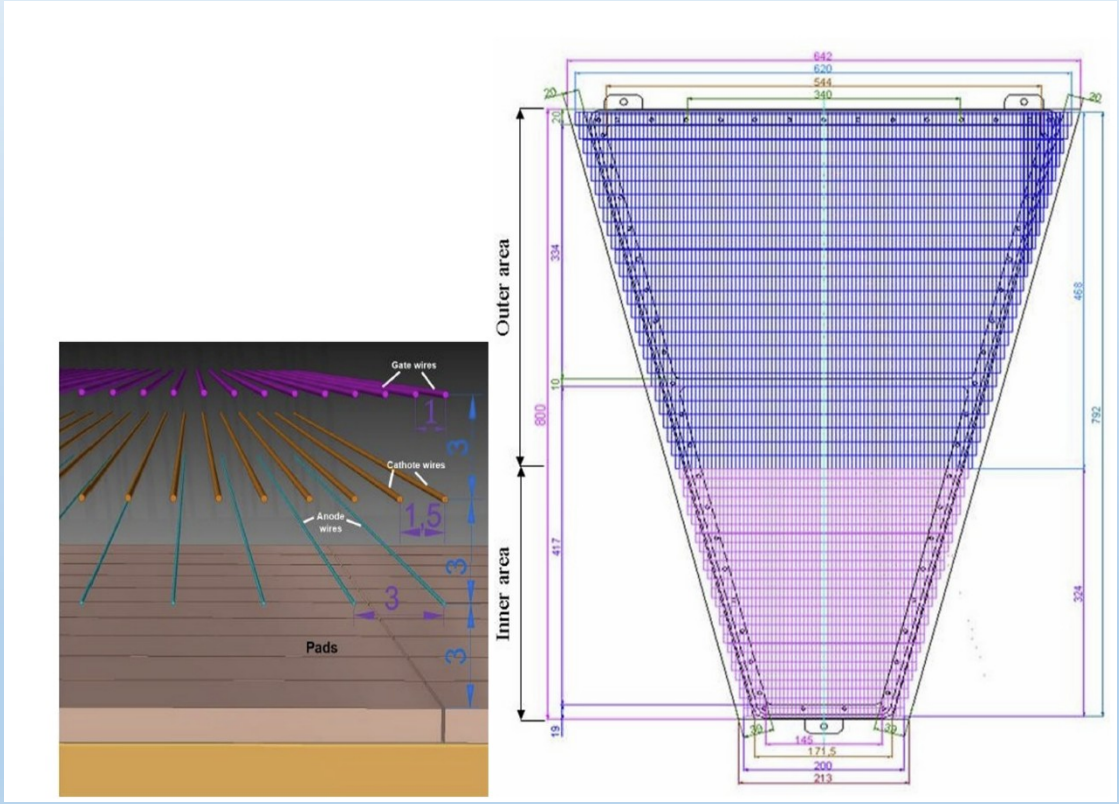


Diagram of the ROC chamber (left) and the pad plane electrode layout (right)

TPC Front-End Card (FEC) Prototype Based on the SAMPA ASIC Chip and FPGA

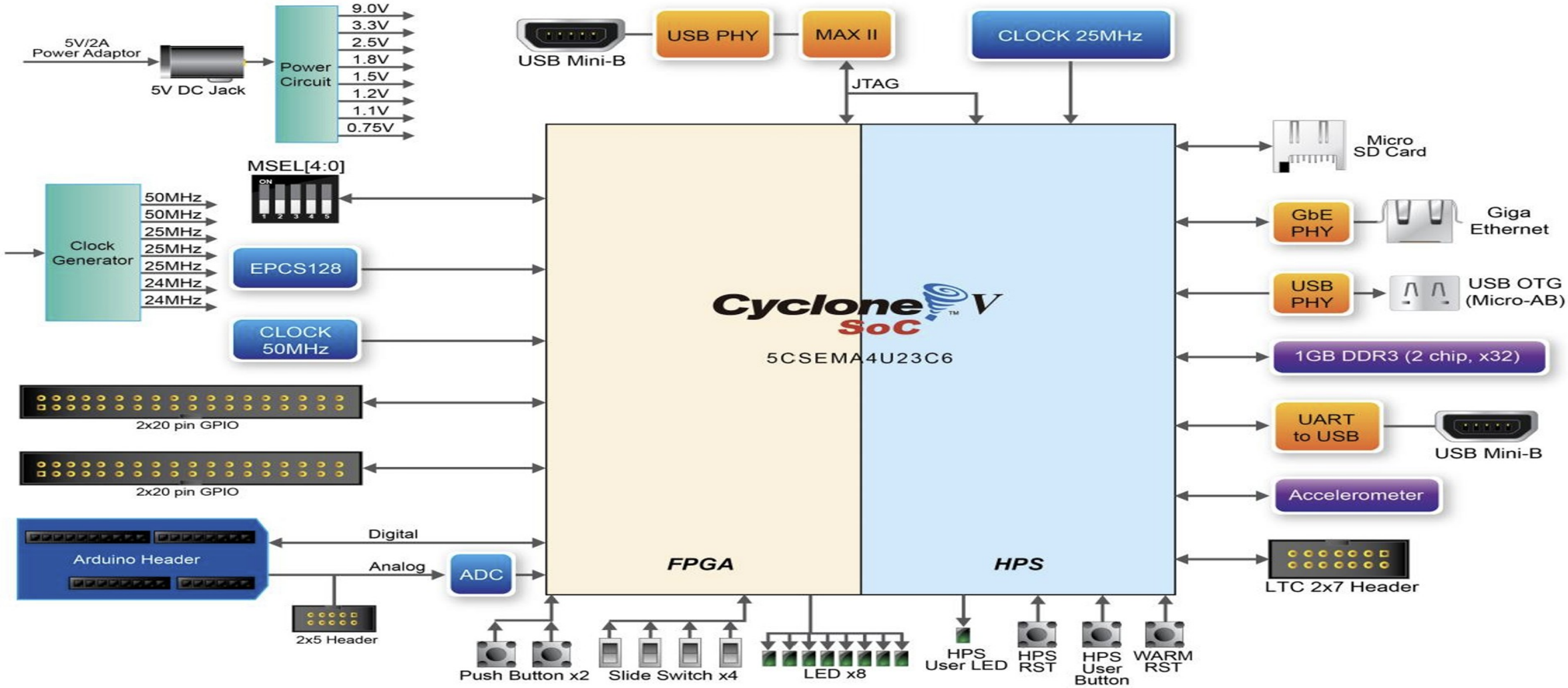
Two 32-channel **SAMPA ASICs** for signal amplification, shaping, ADC, and zero suppression

ALTERA Cyclone V FPGA for core data processing and transmission

FPGA Functions:
- Synchronizes SAMPA links
- Initializes channels
- Reformats data to 32-bit
- Sends data to RCU via high-speed serial links (up to **2.5 Gbps**)

Deployment:
- ~1,500 Cyclone V FPGAs used
- Designed for **radiation-prone environments**

DE0-Nano-SoC system block diagram

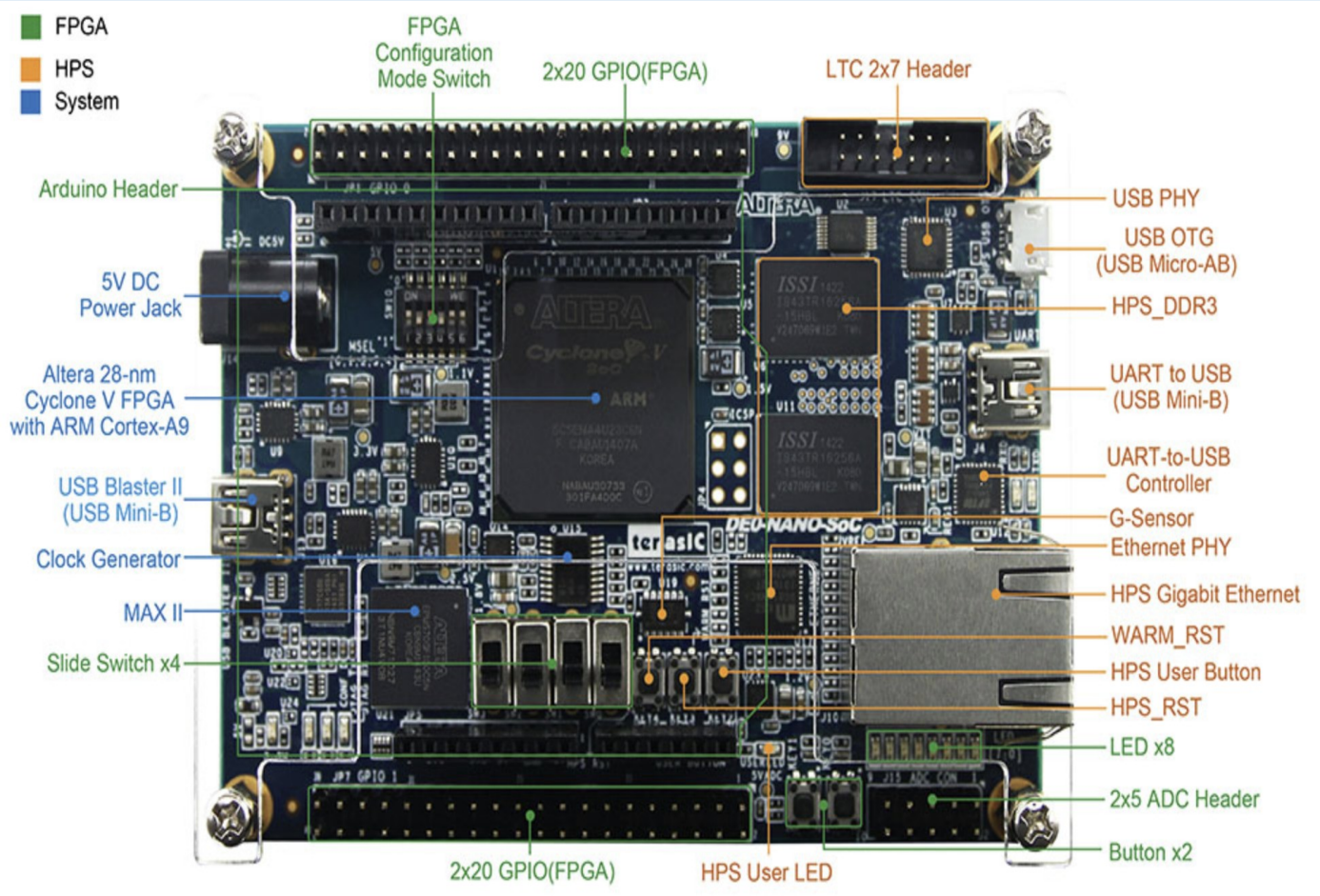


Methodological

- The next phase of the investigation involved the DE0-Nano SoC development board, featuring the Cyclone V FPGA, selected as the closest match to the current TPC electronics setup.

- This board was exposed to neutron irradiation at the JINR FRANK and FLNP Neutron Laboratories, with remote control facilitated through Quartus FPGA firmware developed in Verilog HDL.

- During irradiation, the FPGA's data transmission stability was closely monitored to assess performance.



Key components of the DE0-Nano-SoC Kit/Atlas-SoC Kit

Main components of the DE0-Nano-SoC block diagram

Cyclone V SoC FPGA: Integrates dual-core ARM Cortex-A9 with programmable logic

Hard Processor System (HPS): includes ARM cores and key peripherals (UART, USB, Ethernet, memory controllers)

FPGA Logic Fabric: Customizable logic blocks for user-defined hardware functions

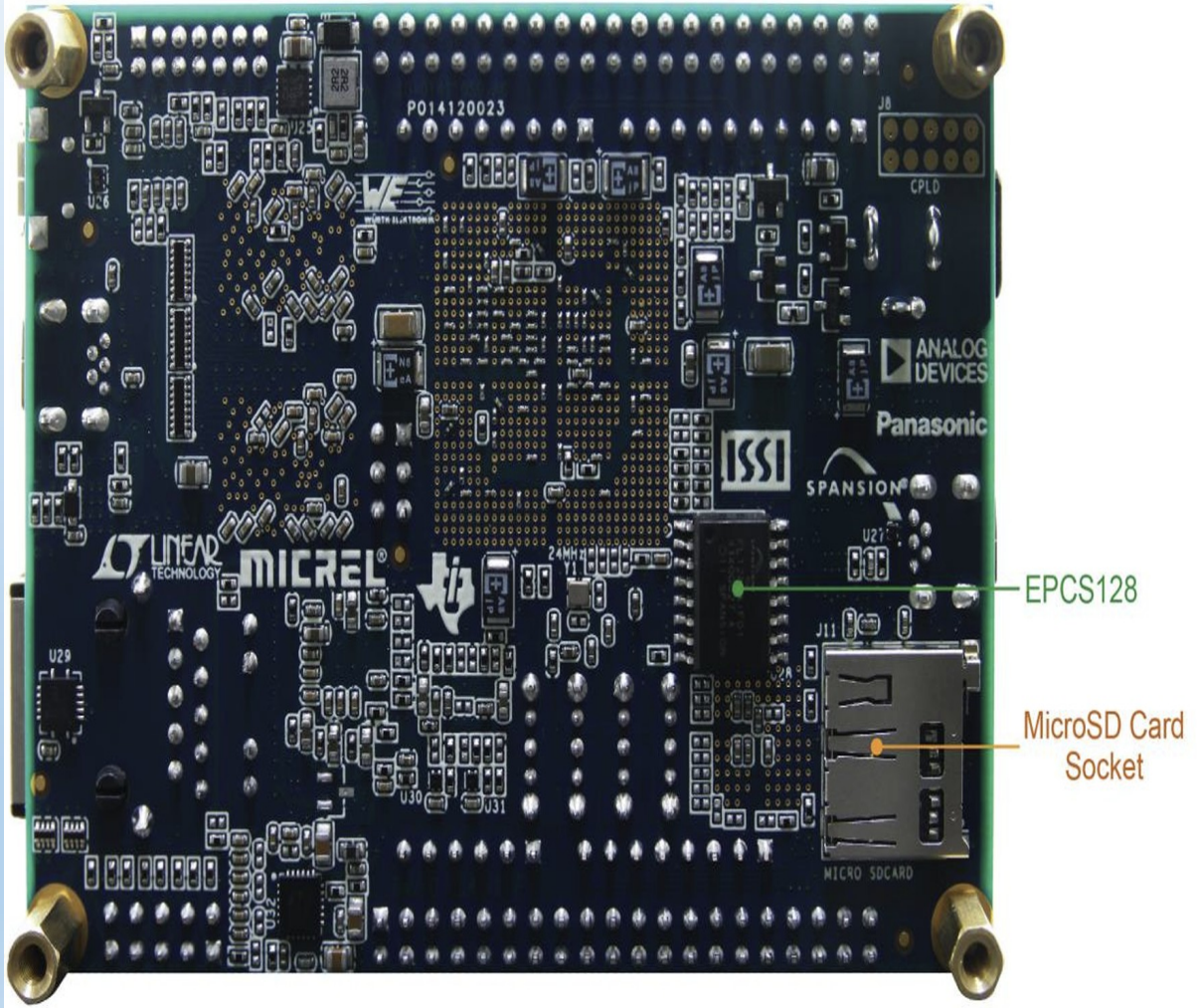
DDR3 SDRAM (HPS_DDR3):External memory for data storage and processing

Configuration Memory (EPCS/EPCQ):Stores FPGA configuration for system startup

Clock Generators: Provide timing for FPGA and HPS operation

Power Supply System: Manages board power through regulators and connectors

I/O Interfaces: Includes GPIOs, switches, LEDs, and expansion headers



Bottom view of the DE0-Nano-SoC development board

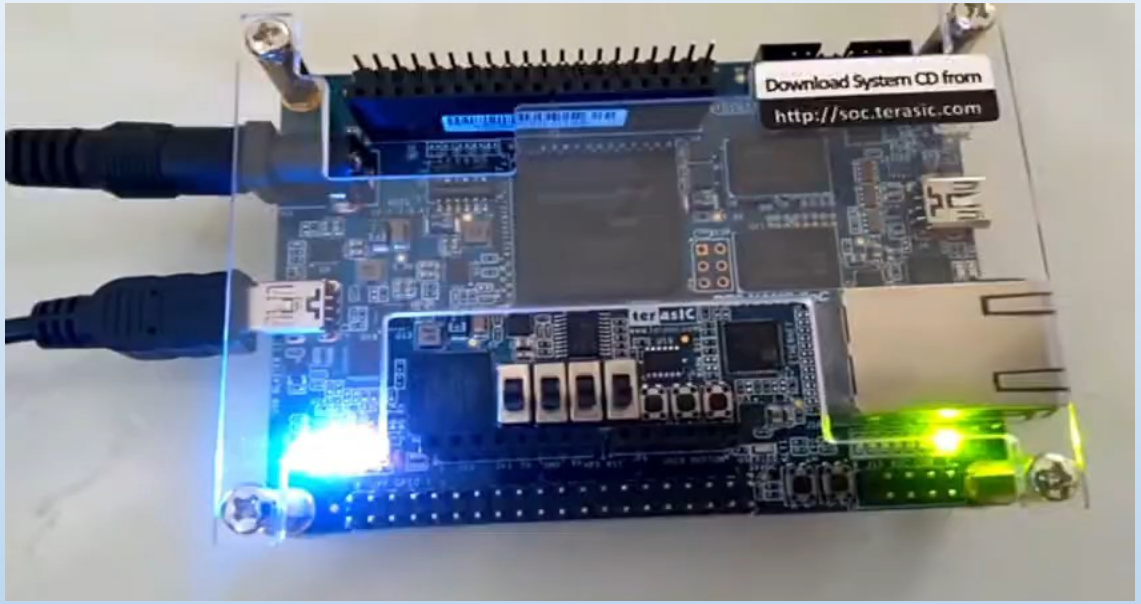
When Do the FPGA [0–7] LED Indicators Turn On?

Stage 1: Power On — Nothing Happens

FPGA chip work properly?

"FPGA is un-configured"
"No design loaded = No LED control"

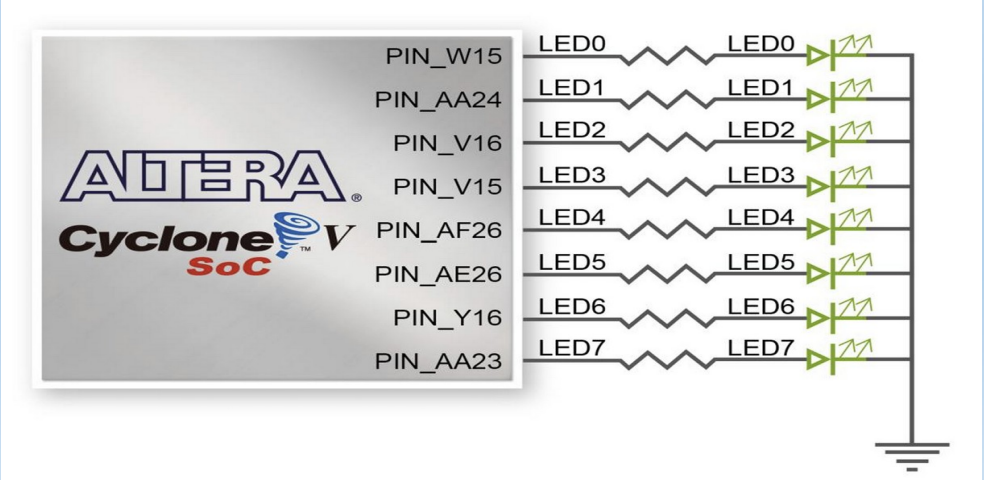
LEDs: Grayed-out/off



Stage 2: Configuration Loaded

Quartus tool with uploading first FPGA module or USB/JTAG arrow pointing to FPGA

- *"FPGA programmed via JTAG or flash"*
- *"Design contains LED logic (e.g., counter, GPIO)"*
- **LEDs**: LED turns on (indicating logic is active, Clock for FPGA Active configured)



First Irradiation Set –up for the Deo-Nano Soc Kit board Utilizing the EG-5 Accelerator

Radiation Exposure Setup:

Neutron irradiation was performed using neutrons produced by the **EG-5 electrostatic accelerator** at the **Neutron Physics Laboratory, Joint Institute for Nuclear Research (JINR)**.

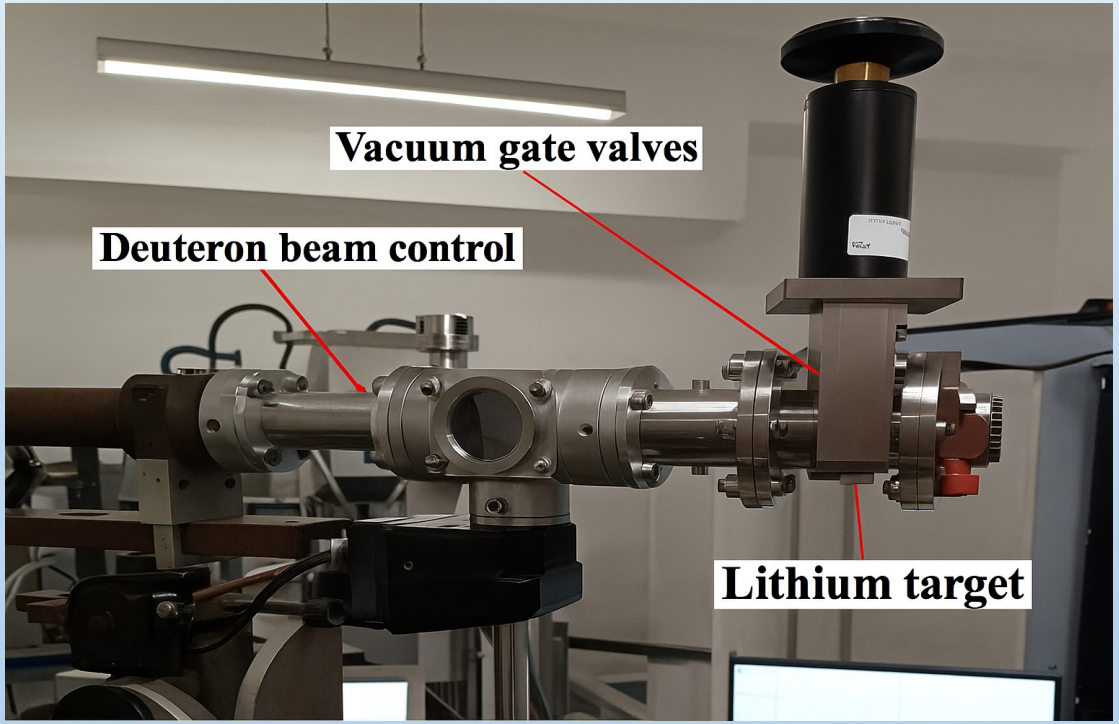
Irradiation Schedule:

The **DE0-Nano SoC Kit board** was exposed over **two days**:

- **April 3rd**: 11:00 AM – 5:00 PM
- **April 4th**: 10:00 AM – 5:00 PM

Total Exposure Time:

Approximately **10 hours and 40 minutes**, accounting for **10-minute breaks every hour** of irradiation.



Lithium target on the third channel of the EG5 accelerator.

Neutron Source Setup

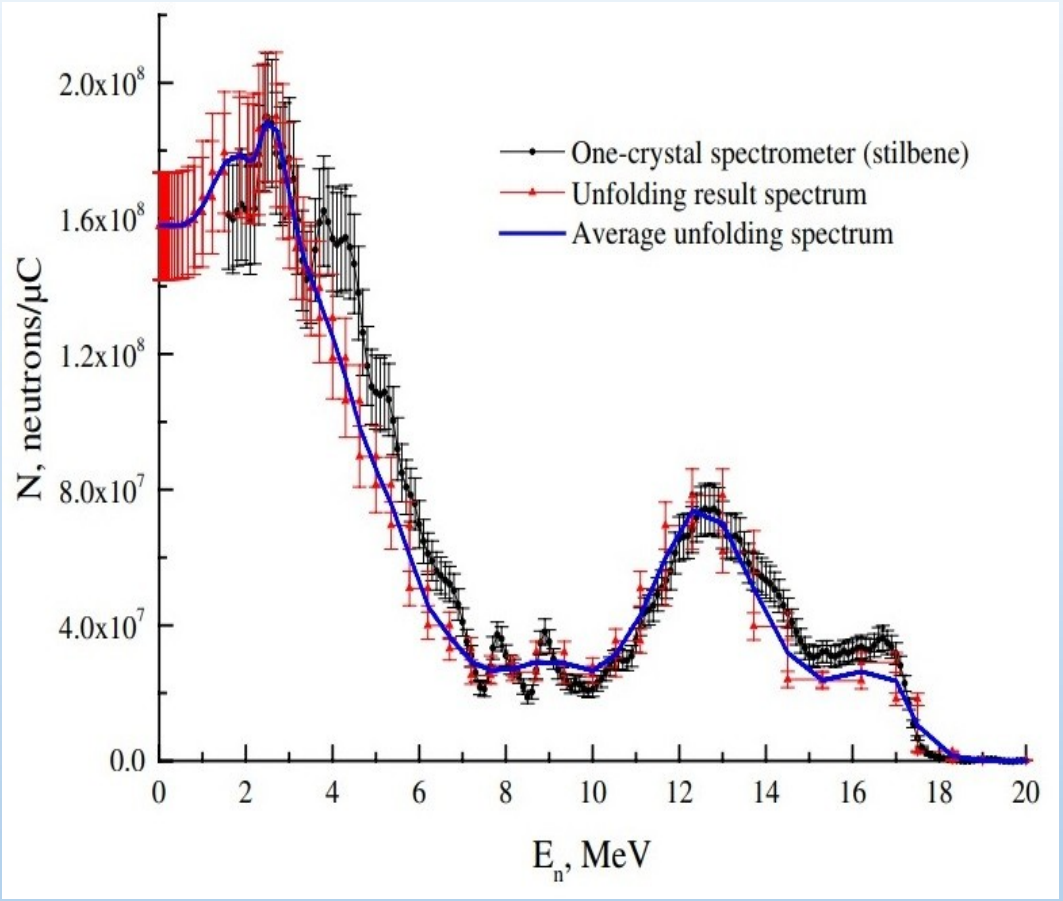
Neutrons were produced by bombarding a **270 µm thick, 5 cm² lithium target** with **deuterons**, generated from **deuterium gas** in the ion source.

Reaction Used:
The neutron-producing reaction was:
Li (d, n) ^{8}Be

Irradiation Configuration:
Neutron flux calculations considered:
- Gas cell **length and pressure**
- Entrance **molybdenum (Mo) foil**

Neutron Characteristics:
- Estimated flux: **0.5 × 10⁷ n/cm²·s**
- Approximately **30% of neutrons** had energies around **14 MeV**

Tools Used:
Neutron flux estimated using the **Energy Set Version 3.1** program



Neutron spectrum from the Li (d, n)^{8}Be reaction, expressed in neutrons/µC, representing the number of neutrons produced per micro coulomb of beam charge

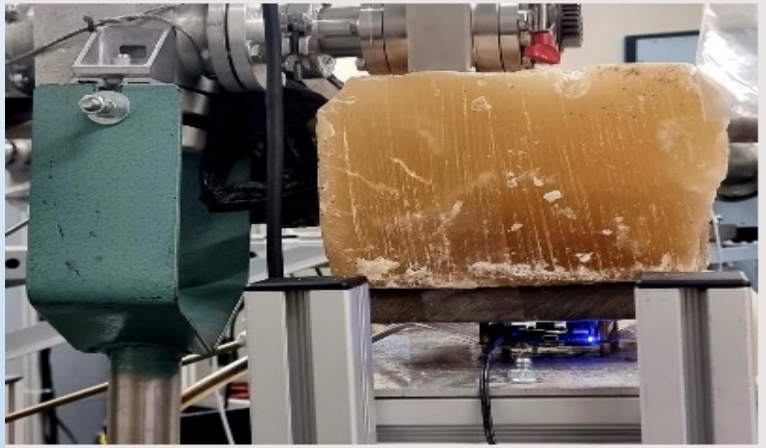
Shielding of the Deo Nano SOC KIT Board

a) installation of the EG5 accelerator's third channel to expose the electronic kit board for neutron radiation source.

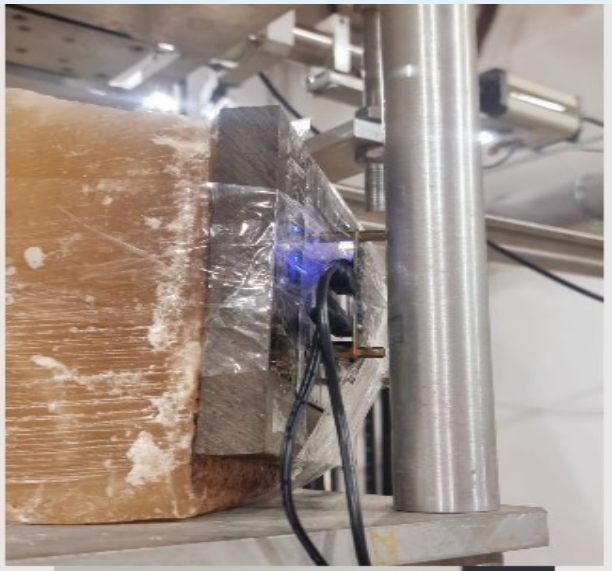
b) Connect the kit board for the FPGA Cyclone V to the power supply and make the connection between the kit board and the personal computer using UART to USB (USB MINI-B) Cable to remote control the kit while being irradiated.

c) two layers of Borated polyethylene and Cadmium.

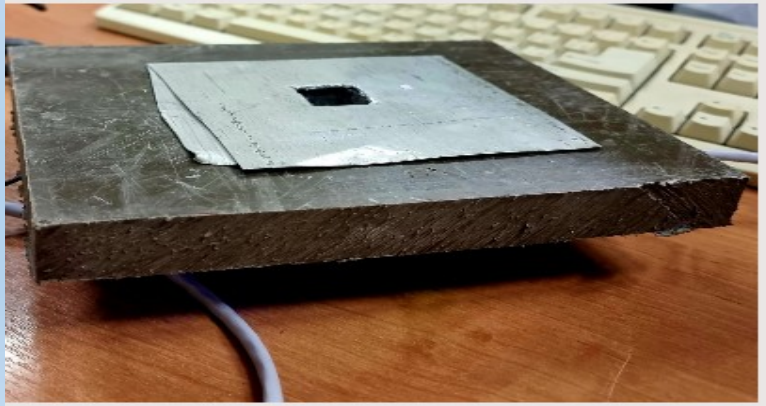
d) shielding materials consist of three layers of (Borated polyethylene, Paraffin, and Cadmium).



a)



b)



c)

d)

Installation of the Deo –Nano Soc KIT Board in the EG-5 Accelerator Irradiation Facility

Board Installation
Mount the **DE0-Nano SoC Kit** above the **EG-5 Accelerator irradiation surrounding table**.

Power and Communication Setup
Power on the board within the radiation room. connect the **FPGA Cyclone V Kit** to:

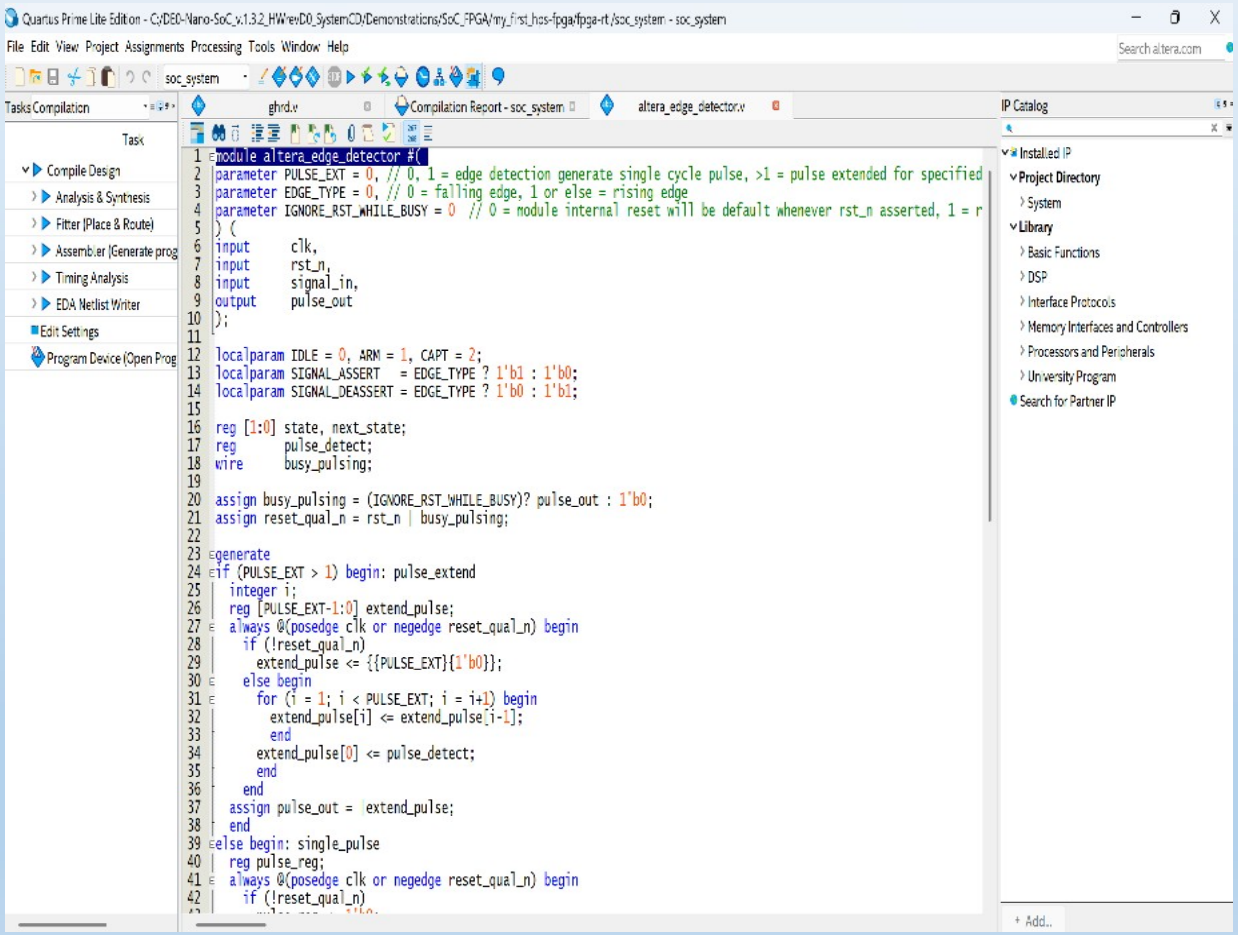
- A **power supply**
- A **PC via UART-to-USB (Mini-B) cable** for remote communication

Remote Operation
This setup enables **remote control and data logging** from outside the radiation area during exposure.

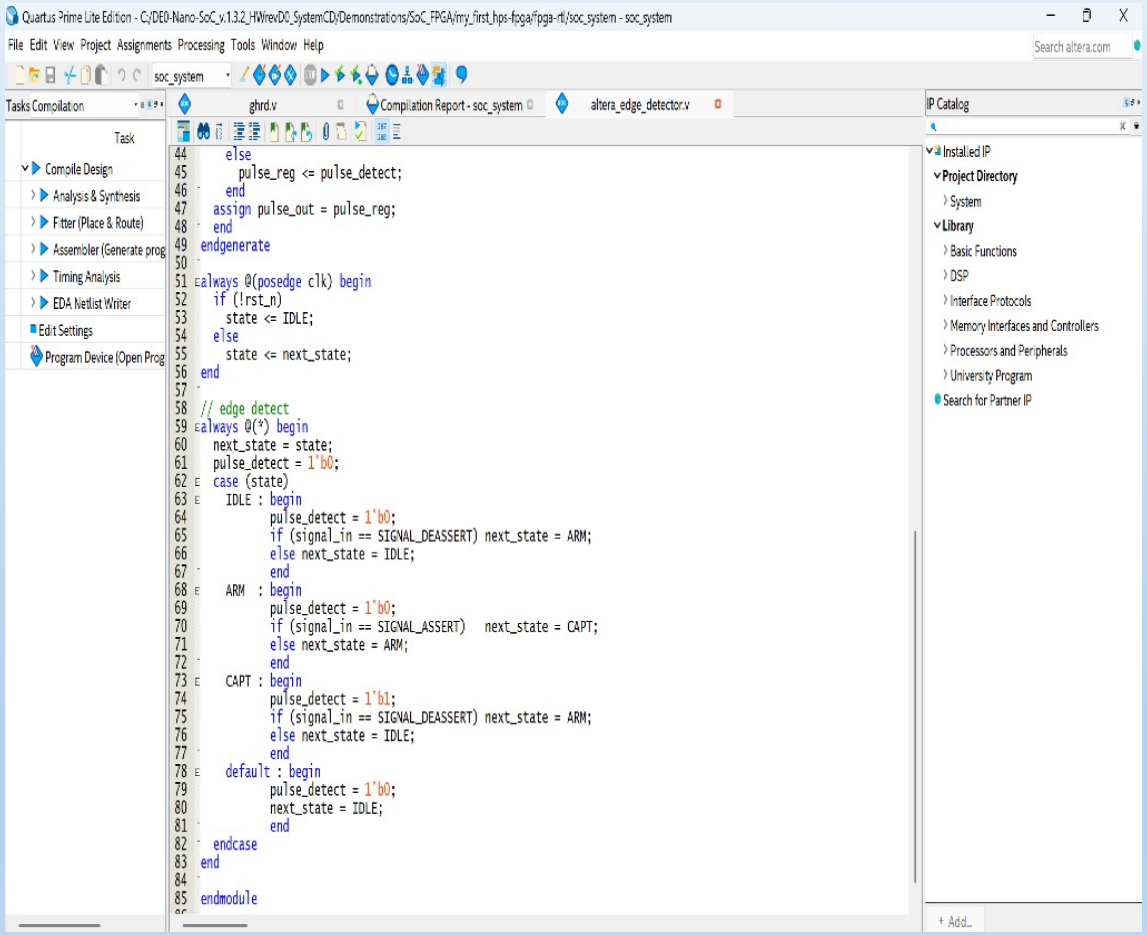
Neutron Shielding
*Apply **three layers of shielding** to filter neutrons (up to 14 MeV):*

- **Borated Polyethylene "moderator + absorber"**, **Paraffin "moderator"**, **Cadmium Sheet "absorber"**
- **Average energy** during exposure is approximately **3 MeV**

Quartus software tool for control and simulation design for Deo Nano Soc Development board



a)



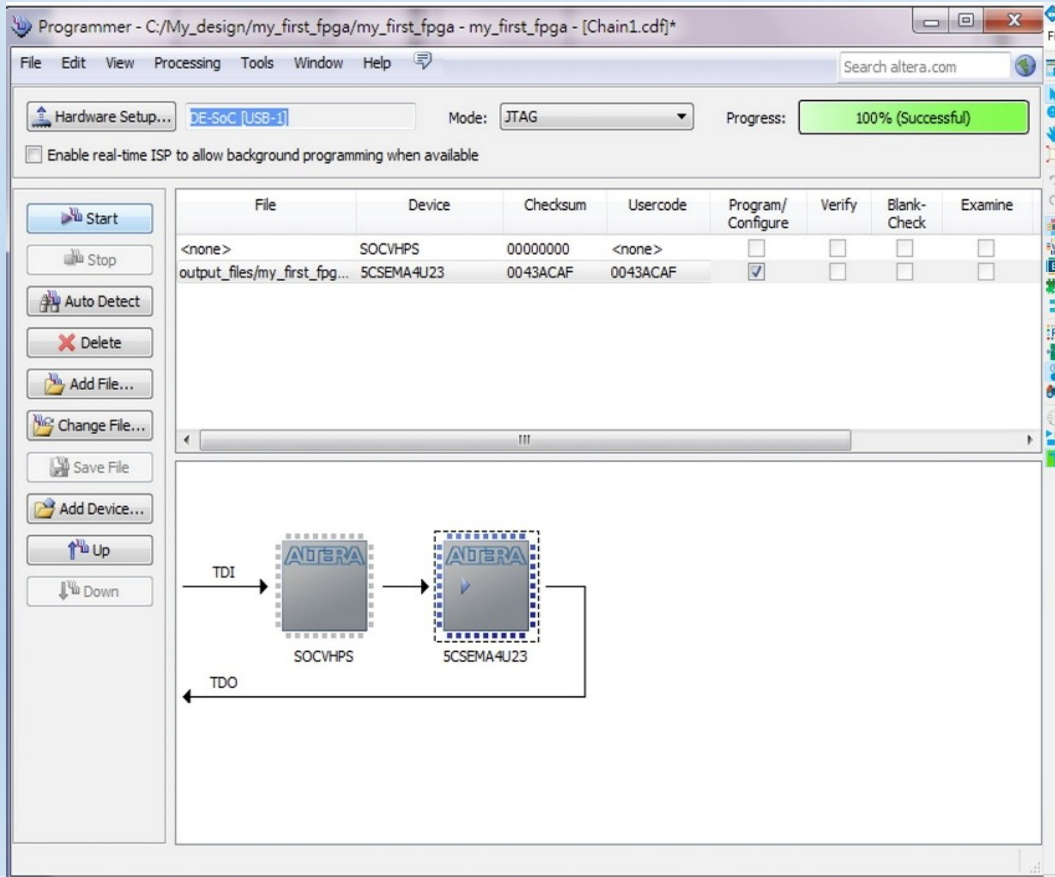
b)

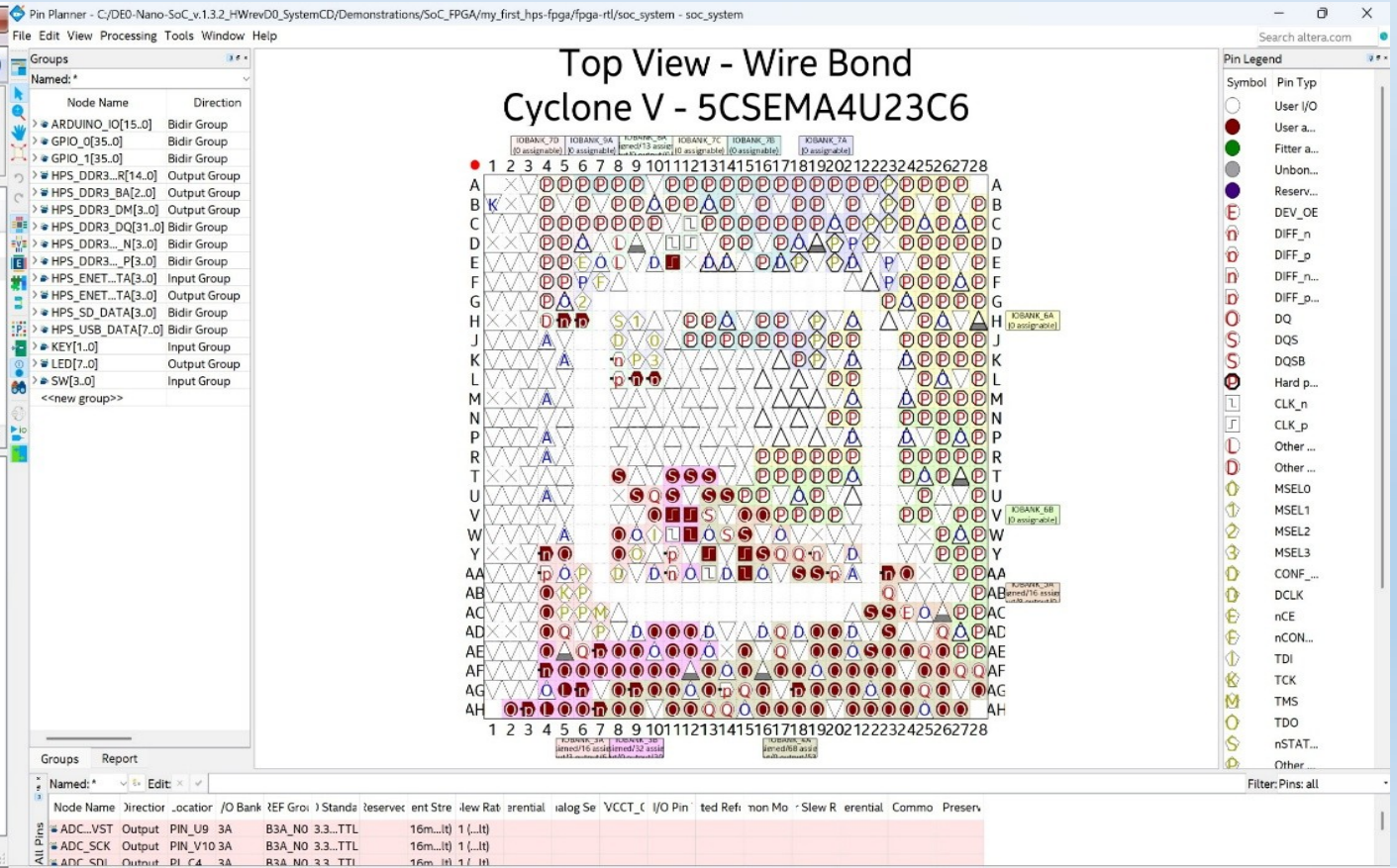
Verilog HDL code that was used to program and control the first FPGA test for the DEO Nano SOC Kit board.

Quartus Integration with DE0-Nano SoC Kit during Irradiation Procedure.

- **Quartus** enables full development flow using **Verilog**, from design to hardware deployment
- Connected to the **KIT board** via **UART-to-USB (Mini-B) cable**

a) Successful UART-to-USB (Mini-B) connection established between PC and DE0-Nano SoC kit using Quartus; b) shows the Top View Wire Board interface for the Cyclone V.





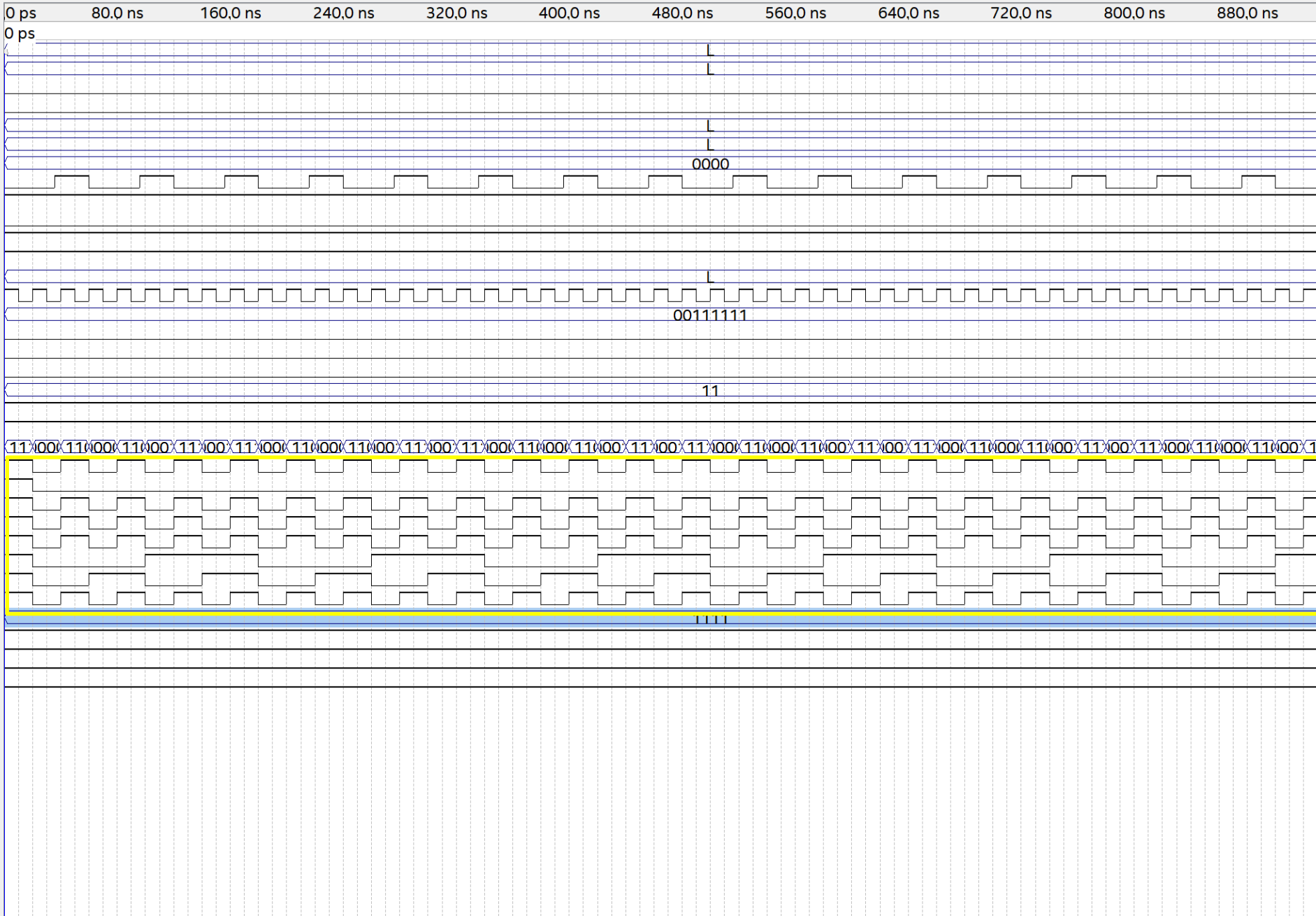
Radiation Impact on Power Distribution System

- The **power system** showed clear effects during **irradiation**, seen in consistent **switching behavior**.
- **LED activity** on the FPGA and HPS confirmed the system's response.
- Observations were captured using **Quartus Universal Waveform Simulator** **in the following two slides.**

1. **Radiation disrupts voltage regulators** and power circuits, causing instability
2. The **DE0-Nano SoC kit shut down approx. every 80 minutes** during exposure
3. Each shutdown was followed by a **30-minute automatic recovery**
4. increased **risk of malfunction or damage**, especially without proper FPGA shielding

Master Time Bar: 0 ps | Pointer: 372.56 ns | Interval: 372.56 ns | Start: 0 ps | End: 1.0 us

Name	Value at 0 ps
HPS_I2C1_SDAT	B L
HPS_KEY	B L
HPS_LED	B 0
HPS_LTC_GPIO	B 0
HPS_SD_CLK	B L
HPS_SD_CMD	B L
HPS_SD_DATA	B 0000
HPS_SPIM_CLK	B 0
HPS_SPIM_MISO	B 1
HPS_SPIM_MOSI	B 0
HPS_SPIM_SS	B 1
HPS_UART_RX	B 1
HPS_UART_TX	B L
HPS_USB_CLKOUT	B 1
HPS_USB_DATA	B 00111111
HPS_USB_DIR	B 0
HPS_USB_NXT	B 0
HPS_USB_STP	B 0
KEY	B 11
KEY[1]	B 1
KEY[0]	B 1
LED	B 11111111
LED[7]	B 1
LED[6]	B 1
LED[5]	B 1
LED[4]	B 1
LED[3]	B 1
LED[2]	B 1
LED[1]	B 1
LED[0]	B 1
SW	B 1111
SW[3]	B 1
SW[2]	B 1



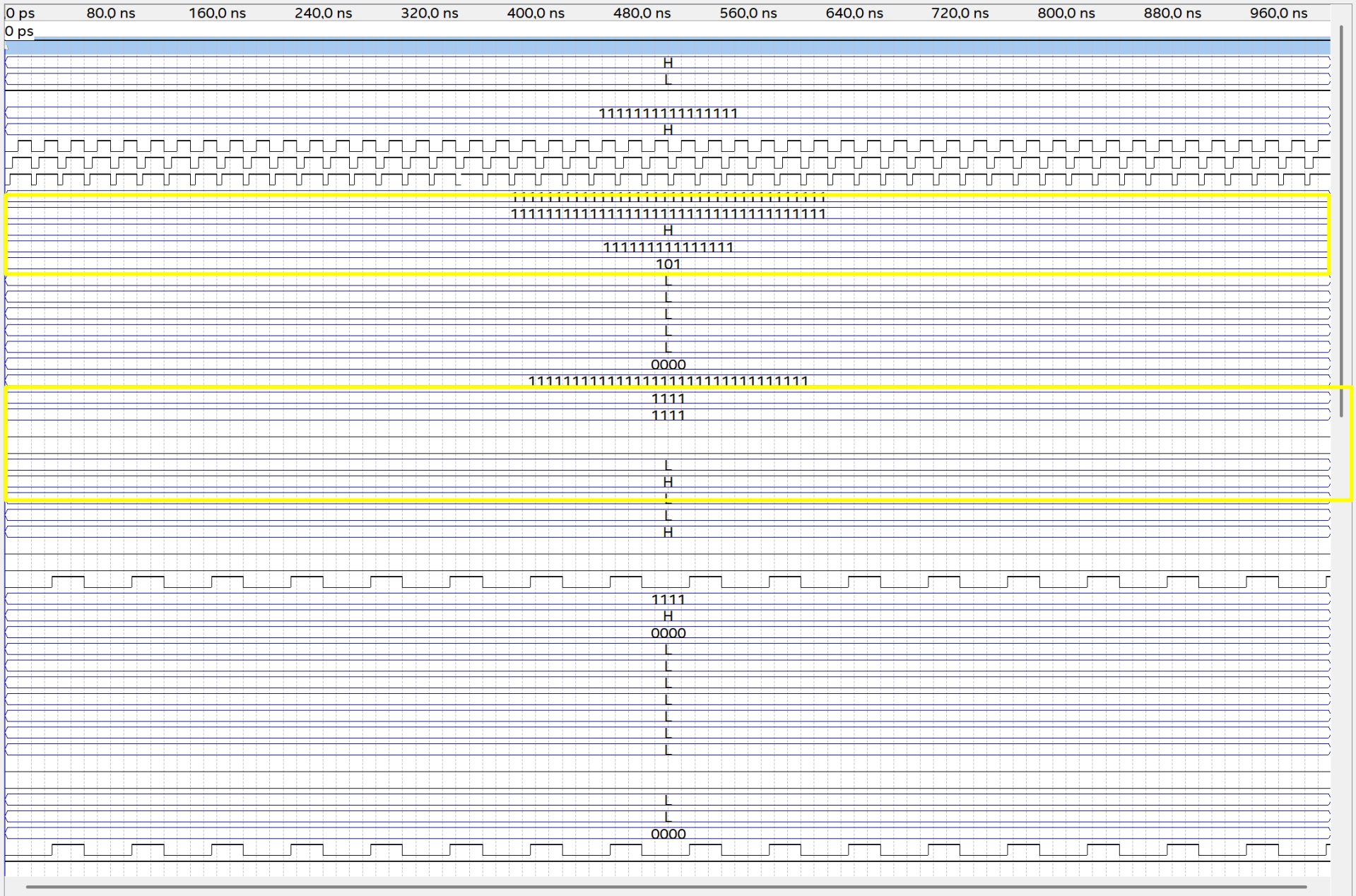
Simulation Waveform Editor - C:/DE0-Nano-SoC_v.1.3.2_HWrevD0_SystemCD/Demonstrations/SoC_FPGA/my_first_hps-fpga/fpga-rtl/soc_system - soc_system - [Waveform.vwf]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 497.23 ns | Interval: 497.23 ns | Start: 0 ps | End: 1.0 us

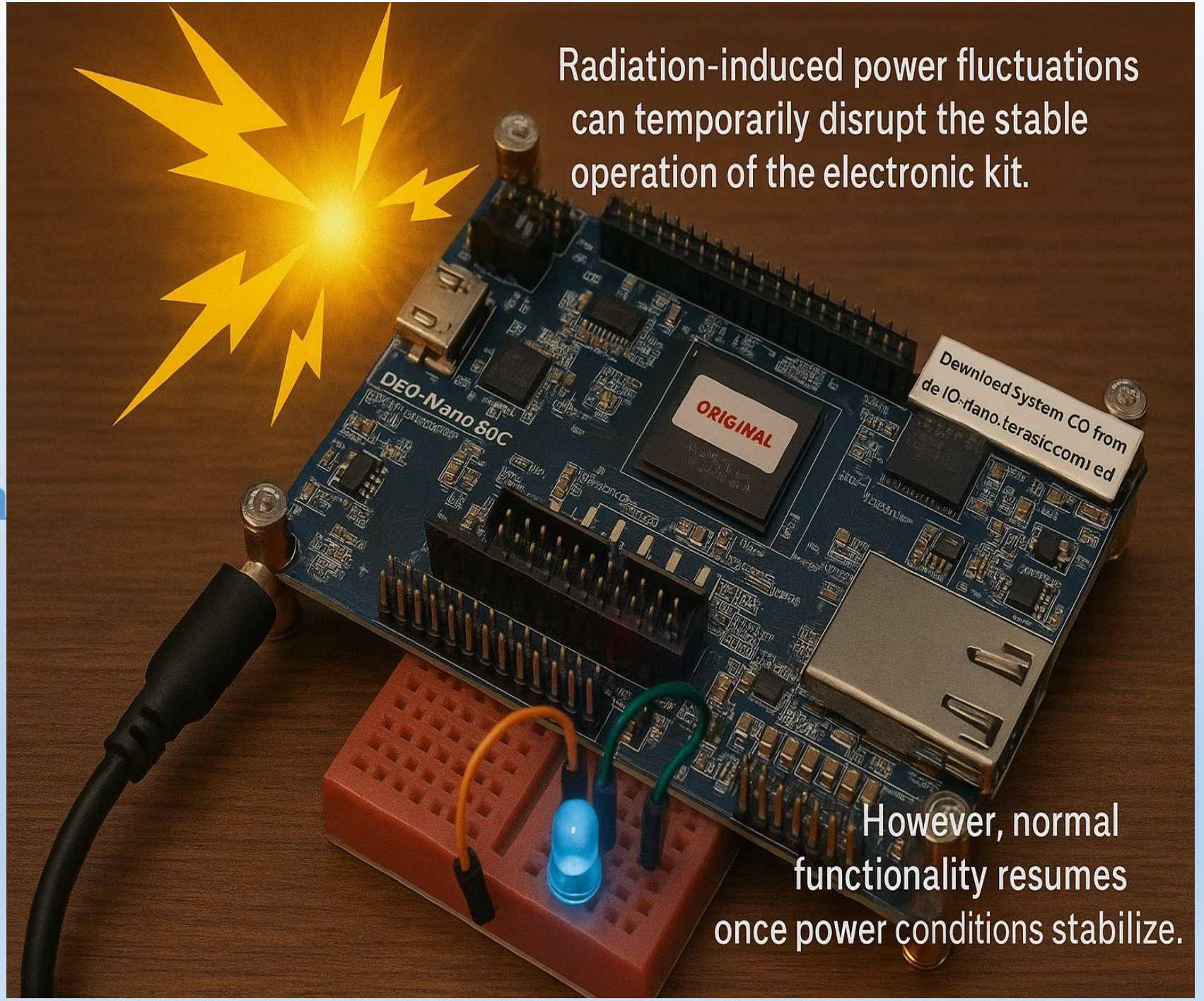
Name	Value at 0 ps
ADC_CONVST	B 1
ADC_SCK	B H
ADC_SDI	B L
ADC_SDO	B 1
ARDUINO_IO	B 111111111...
ARDUINO_RESET_N	B H
FPGA_CLK1_50	B 0
FPGA_CLK2_50	B 0
FPGA_CLK3_50	B 0
GPIO_0	B 111111111...
GPIO_1	B 111111111...
HPS_CONV_USB_N	B H
HPS_DDR3_ADDR	B 111111111...
HPS_DDR3_BA	B 101
HPS_DDR3_CAS_N	B L
HPS_DDR3_CKE	B L
HPS_DDR3_CK_N	B L
HPS_DDR3_CK_P	B L
HPS_DDR3_CS_N	B L
HPS_DDR3_DM	B 0000
HPS_DDR3_DQ	B 111111111...
HPS_DDR3_DQS_N	B 1111
HPS_DDR3_DQS_P	B 1111
HPS_DDR3_ODT	B 0
HPS_DDR3_RAS_N	B 0
HPS_DDR3_RESET_N	B L
HPS_DDR3_RZQ	B H
HPS_DDR3_WE_N	B L
HPS_ENET_GTX_CLK	B L
HPS_ENET_INT_N	B H
HPS_ENET_MDC	B 0
HPS_ENET_MDIO	B 0
HPS_ENET_RX_CLK	B 0
HPS_ENET_RX_DATA	B 1111
HPS_ENET_RX_DV	B H
HPS_ENET_TX_DATA	B 0000



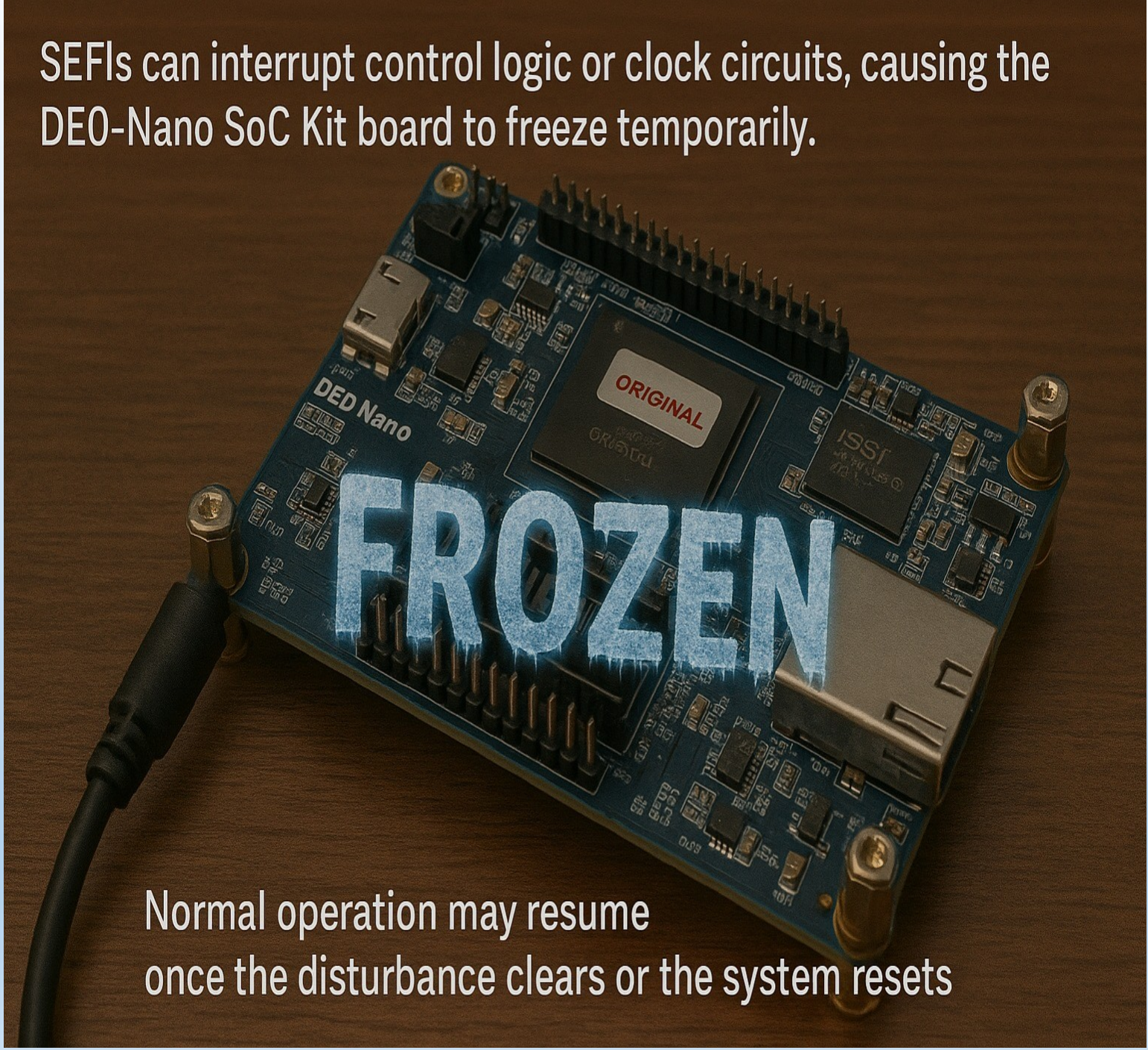
The kit board temporarily stop functioning and then resume during irradiation due to radiation-induced transient faults, such as ***Single Event Upsets (SEUs)*** *or* ***Single Event Functional Interrupts (SEFIs).*** *These effects can momentarily disrupt the FPGA's operation without causing permanent damage.*

This behaviour can occur for several reasons:

Power fluctuations caused by radiation

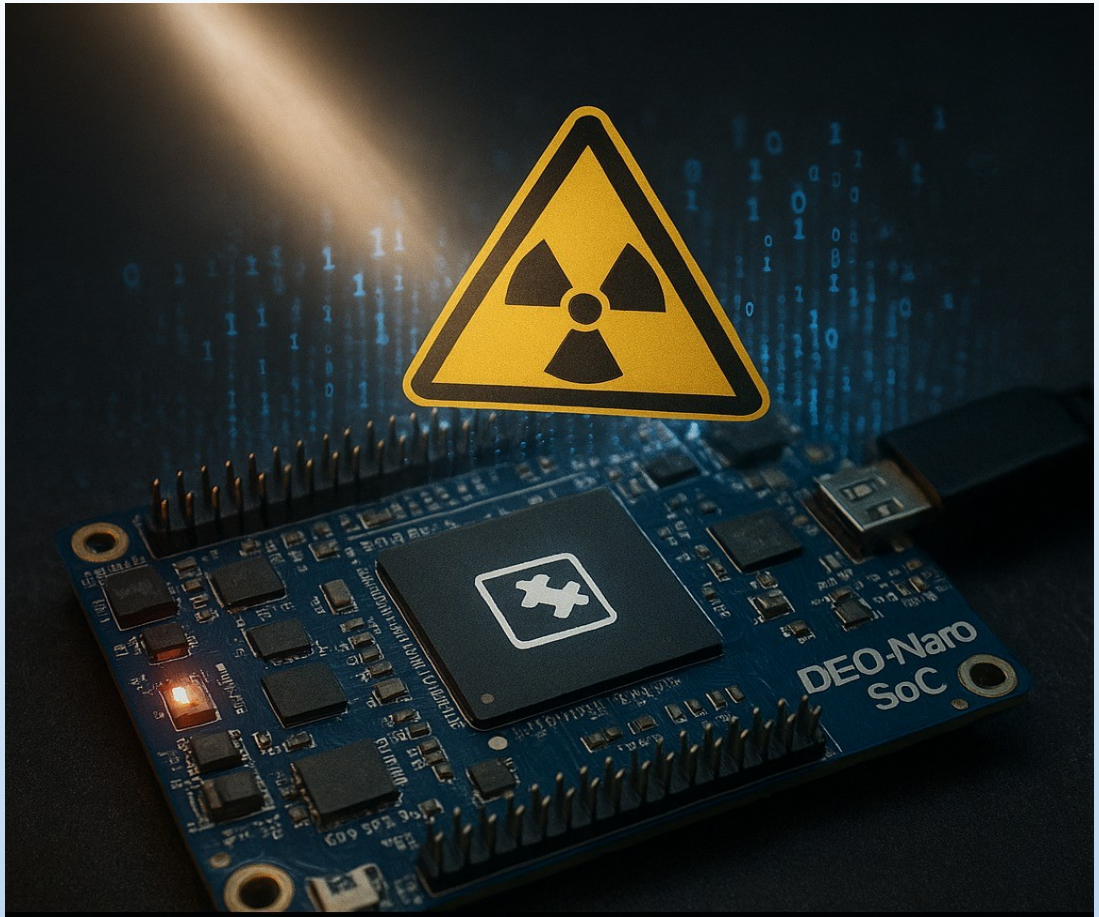


Single Event Functional Interrupts .(SEFIs)



SEUs in Configuration

logic elements may flip individual bits, leading to temporary malfunctions. The system may recover if critical functions are not affected or if built-in error-handling mechanisms correct the fault.



A DE0-Nano SoC development board experiencing a Single Event Upset (SEU) due to irradiation.
Key elements include:
- A radiation warning symbol indicating the presence of ionizing radiation.
- A glowing red LED suggesting abnormal activity or malfunction.
- The FPGA chip marked with a glitch-like icon to symbolize a bit flip or fault

Charge accumulation or localized thermal effects

radiation effect : Once the charge dissipates or thermal conditions return to normal, functionality is restored.

Charge accumulation or localized thermal effects from radiation can briefly affect the DEO Nano SOC kit.

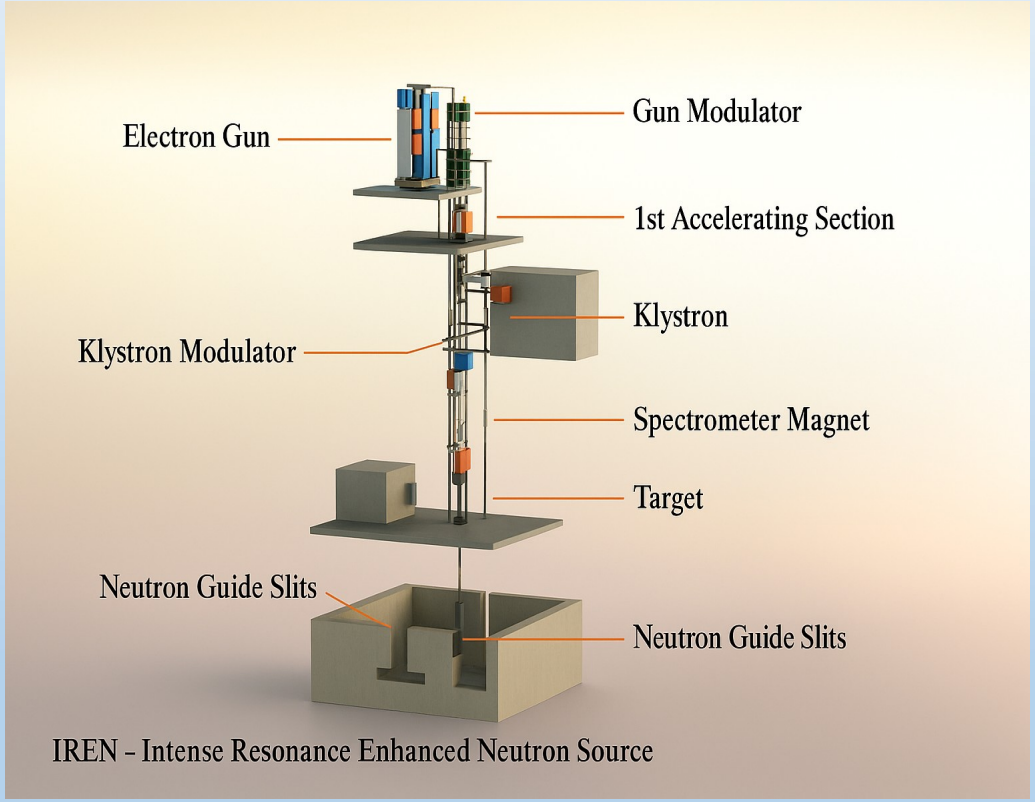
Second Irradiation Process for the Electronic Kit Utilizing the IREN Accelerator

IREN (Intense Resonance Neutron Source)

- Located at JINR, IREN is a pulsed neutron facility.
- Designed to produce high-intensity neutron bursts through nuclear reactions.
- Supports research in nuclear physics, neutron spectroscopy, and materials science.

Key components:

1. Pulsed electron gun
2. Accelerating structure
3. Microwave power sources (10-cm klystrons with modulators)
4. Beam focusing and transport system
5. Broadband magnetic spectrometer for diagnostics



Schematic layout of the IREN (Resonance Neutron Source) facility, including the accelerator and target halls

Second Irradiation Process for the Electronic Kit Utilizing the IREN Accelerator

Neutron-Producing Target Design

- Cylindrical TNF target: 40 mm (diameter) × 100 mm (height)
- Enclosed in a 160 mm diameter aluminum tank.

- Cooled and moderated by a 50 mm thick distilled water layer in a closed-loop system.
- High-energy electrons enter via a 36 mm diameter, 1 mm thick beryllium window.

Neutron Production Mechanism

- Target material: Tungsten-based alloy (VNZh-90) with non-multiplying properties
- Reaction type: A W (γ, n) A–1 (neutron emission from tungsten isotopes)

Two-step neutron generation process:

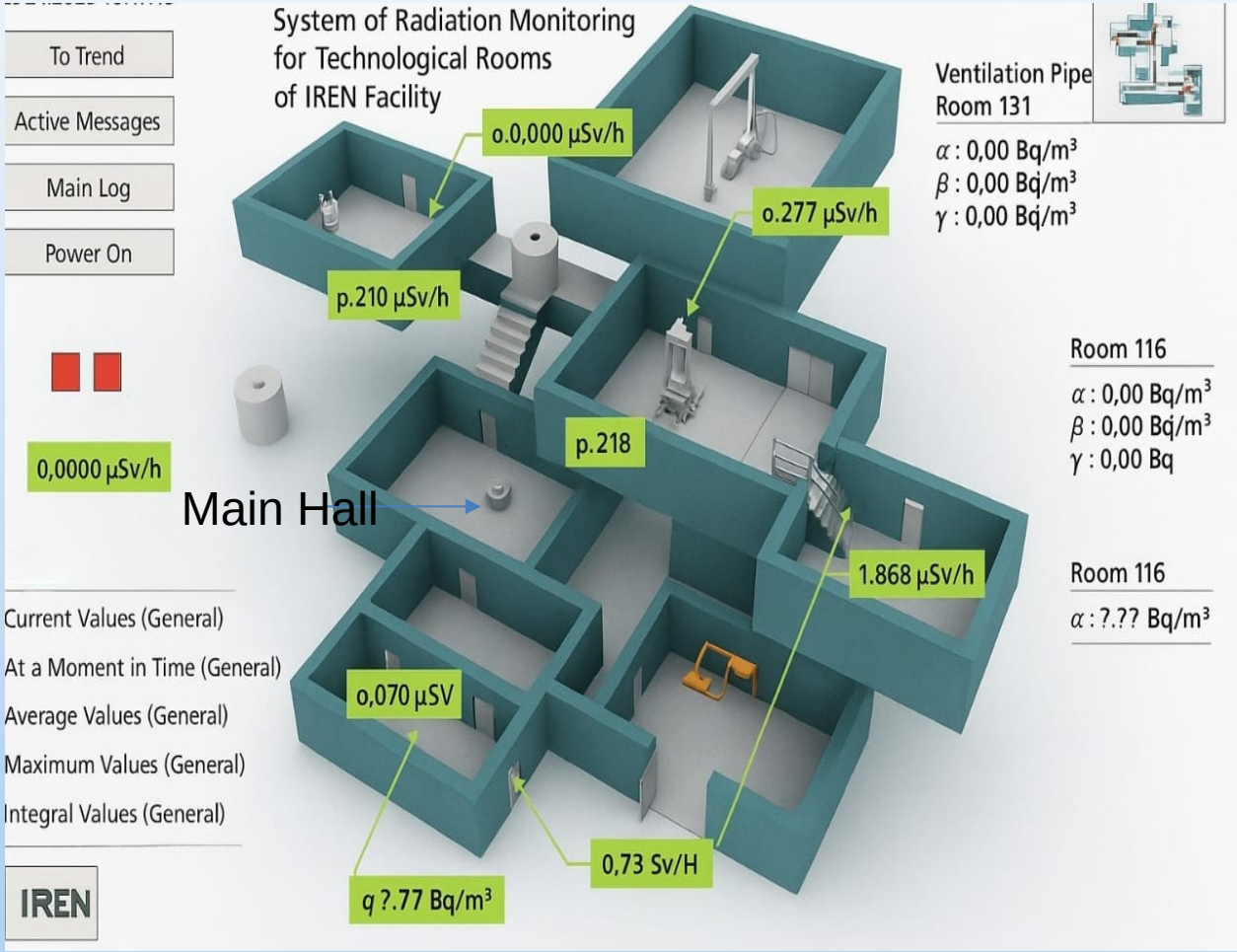
1. High-energy electrons produce bremsstrahlung gamma rays upon hitting the target
2. Gamma rays interact with tungsten nuclei, generating neutrons via (γ, n) reactions

Dosimetry and Radiation Monitoring

- Dosimetry screen shows readings at the main hole of the IREN accelerator immediately after KIT board exposure ends.

- Reflects post-irradiation conditions.

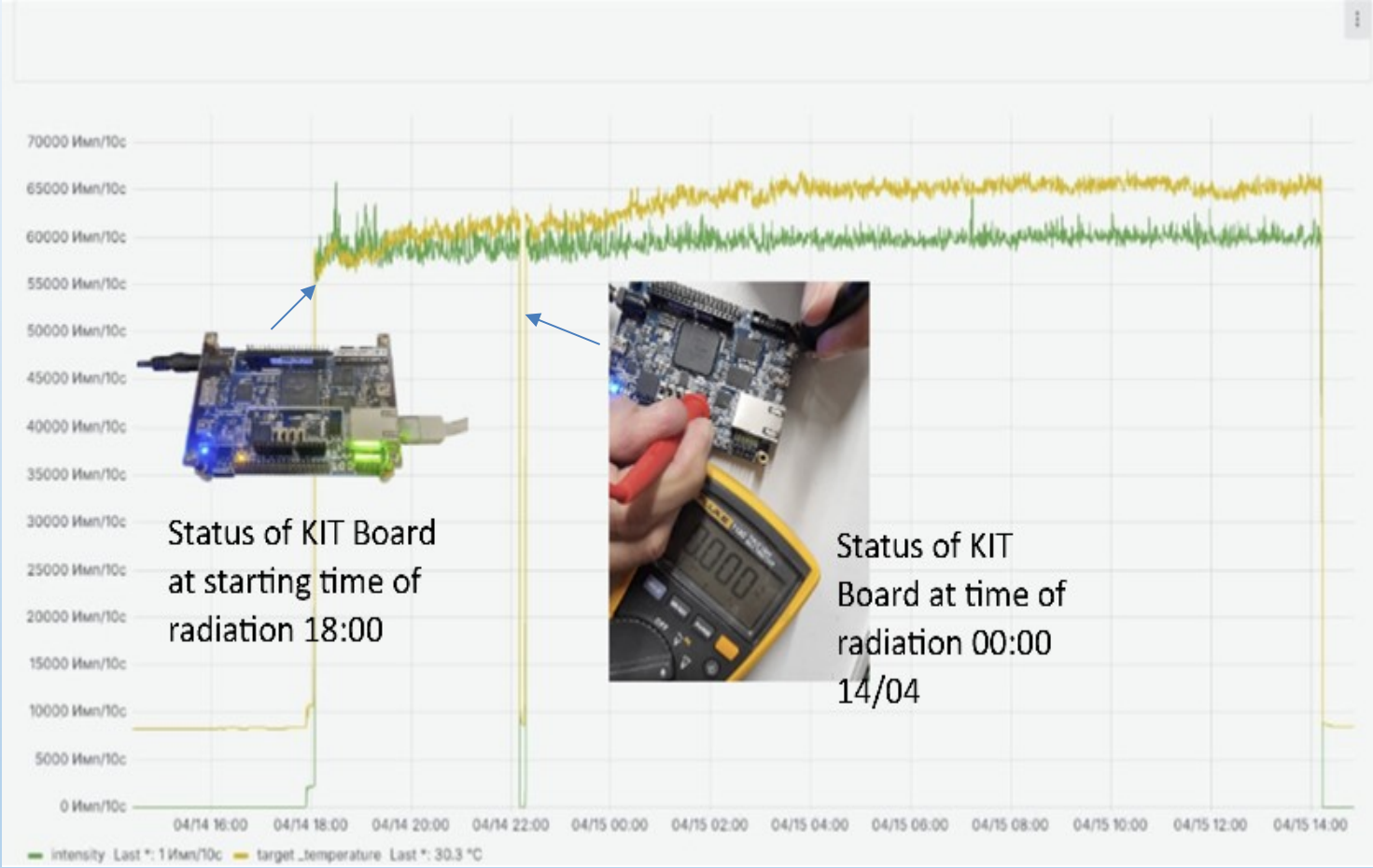
- Detectors show a linear response to accelerator frequency (2–50 Hz), confirming reliable tracking of radiation intensity changes.



Dosimetry screen showing radiation levels after the exposure period ended for the KIT board, taken in the main hall and technical rooms of the IREN Facility, with the primary irradiation unit powered off.

Neutron Flux and Energy Spectrum at IREN

- Broad neutron energy range: thermal to fast neutrons
- Thermal neutron flux: up to **1×10^{8} n/cm²·s**
- Resonance neutron flux: **2×10^{7} to 4×10^{7} n/cm²·s**
- Average total neutron fluence: **~1.6×10^{12} neutrons/s** (in 4π geometry)
- Fast neutron energy: **20–30 MeV**
- During KIT board irradiation: flux was **~10^{7} n/cm²·s**



Neutron flux intensity indicators over the irradiation period for the Deo Nano SoC KIT board " Имп /10с" → "Imp/10s" (Impulses per 10 seconds).

Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.

The DE0-Nano SoC kit's functionality was validated using Verilog, with PC-to-FPGA communication established via USB Blaster and JTAG.

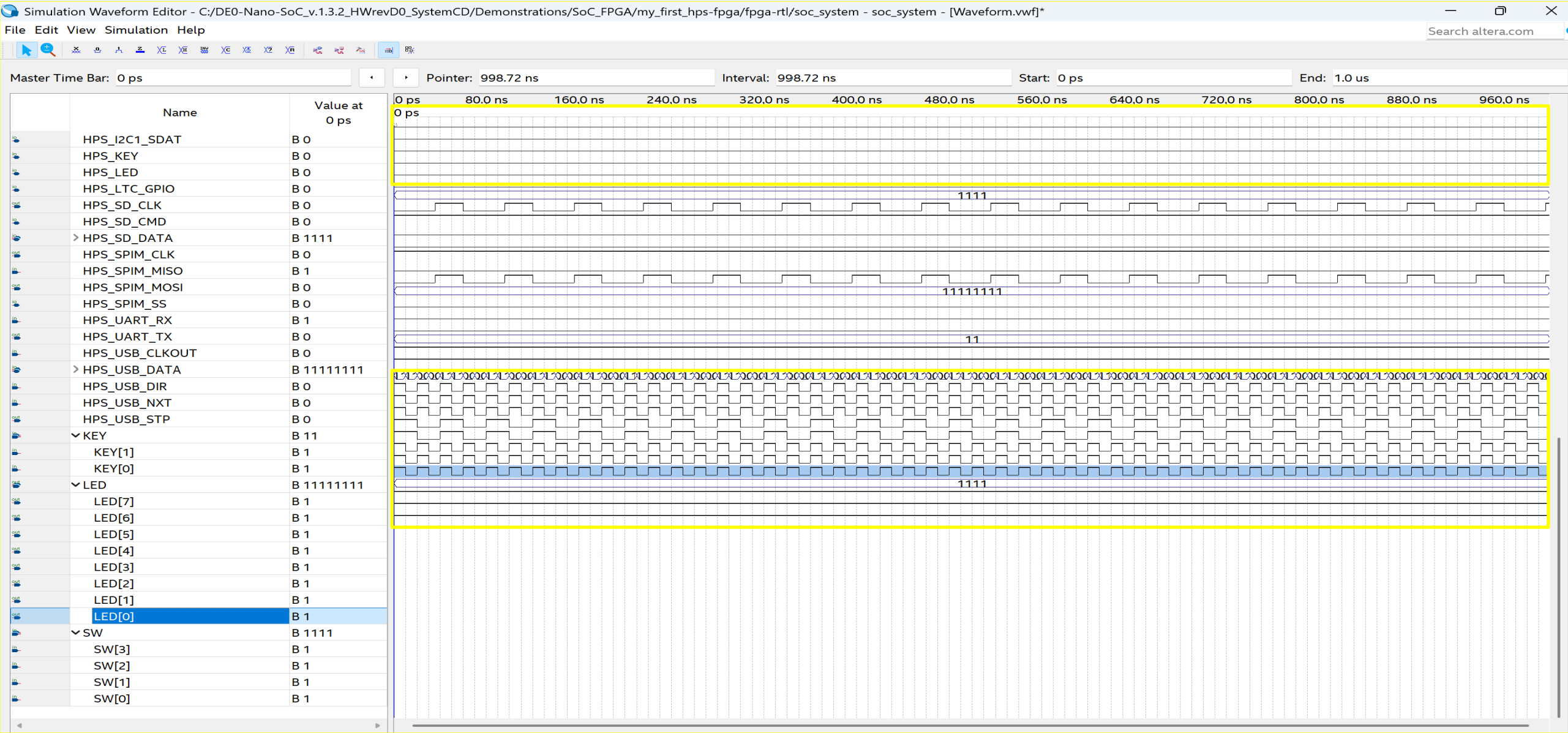
Quartus software served as both a remote-control and simulation tool using Verilog code from earlier tests.

Results show that irradiation from the IREN Accelerator disrupted the DE0-Nano SoC kit’s power system, damaging memory, ports, Ethernet, and power delivery.

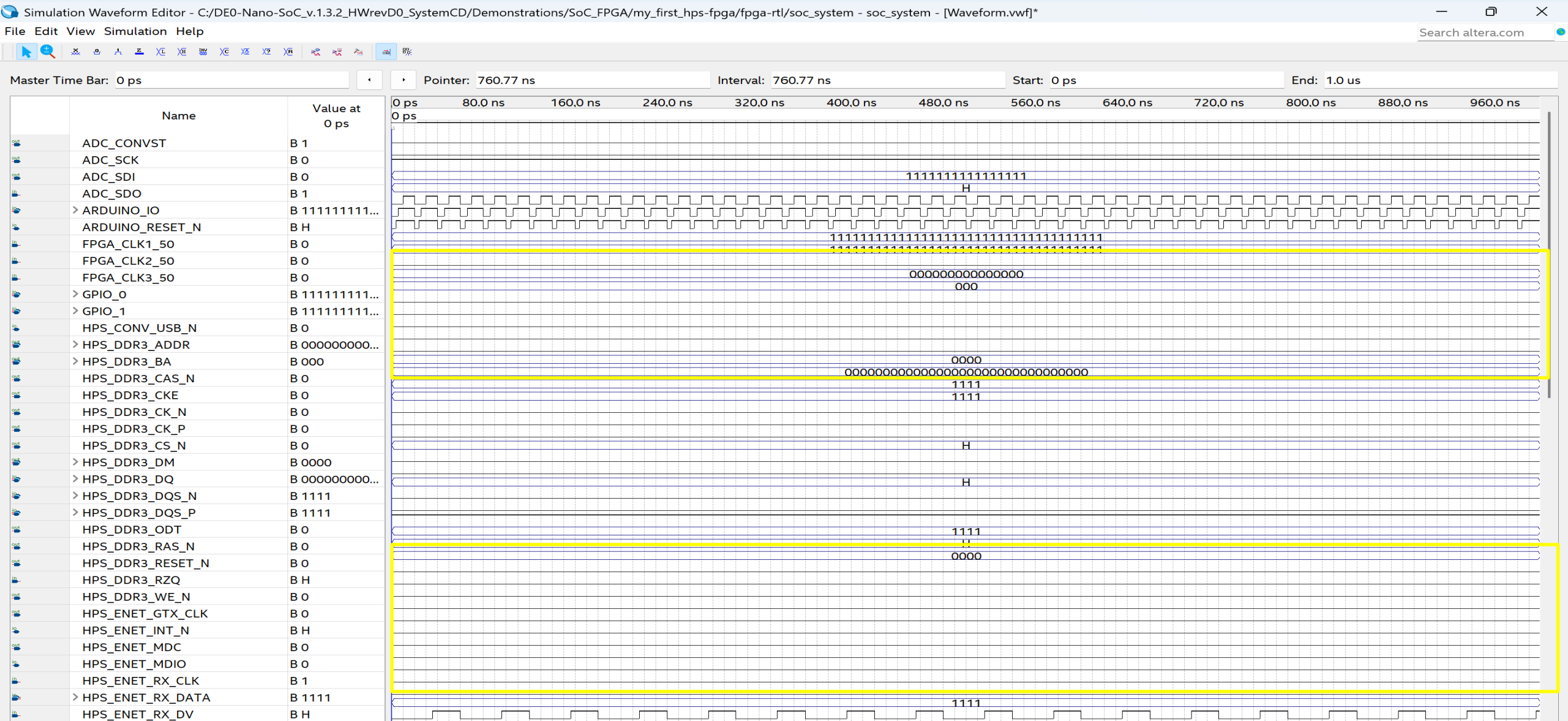
a) b)

Irradiation setup using the IREN Accelerator (a). DE0-Nano SoC kit successfully connected to PC via USB Blaster for Verilog-based testing (b)

Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.



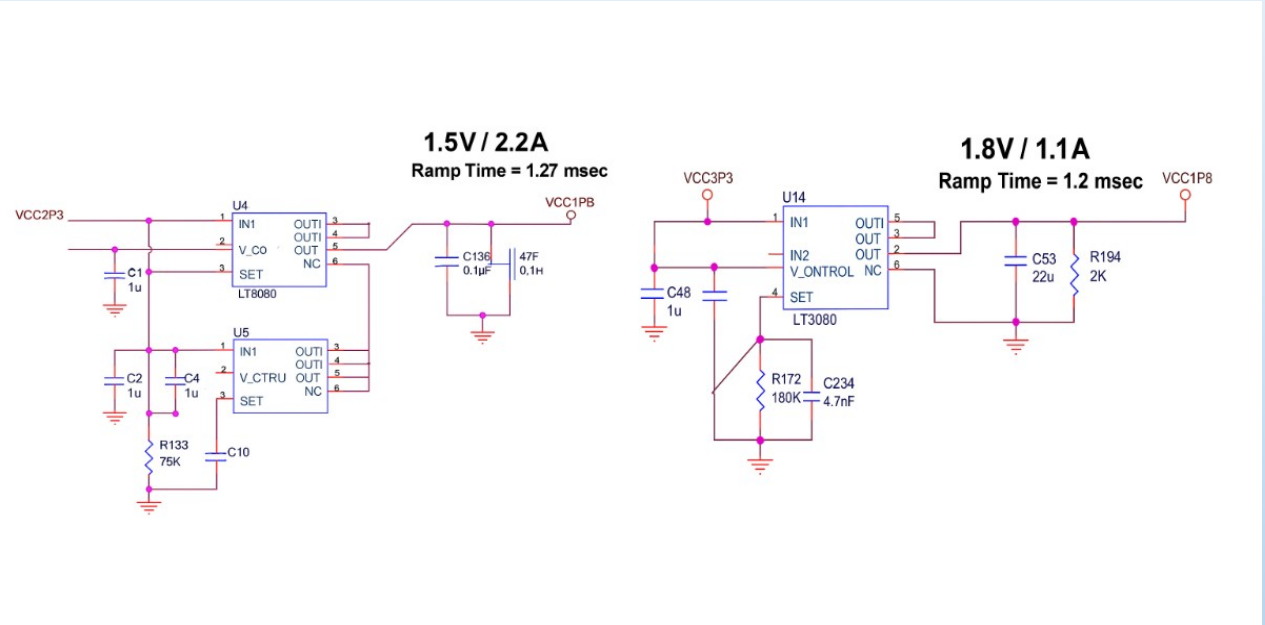
Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.



Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.

Voltage readings and schematics reveal that the DE0-Nano SoC kit's power regulation circuits for the HPS DDR3 and FPGA are malfunctioning.

This disruption in power distribution likely resulted from irradiation exposure in the IREN Accelerator.



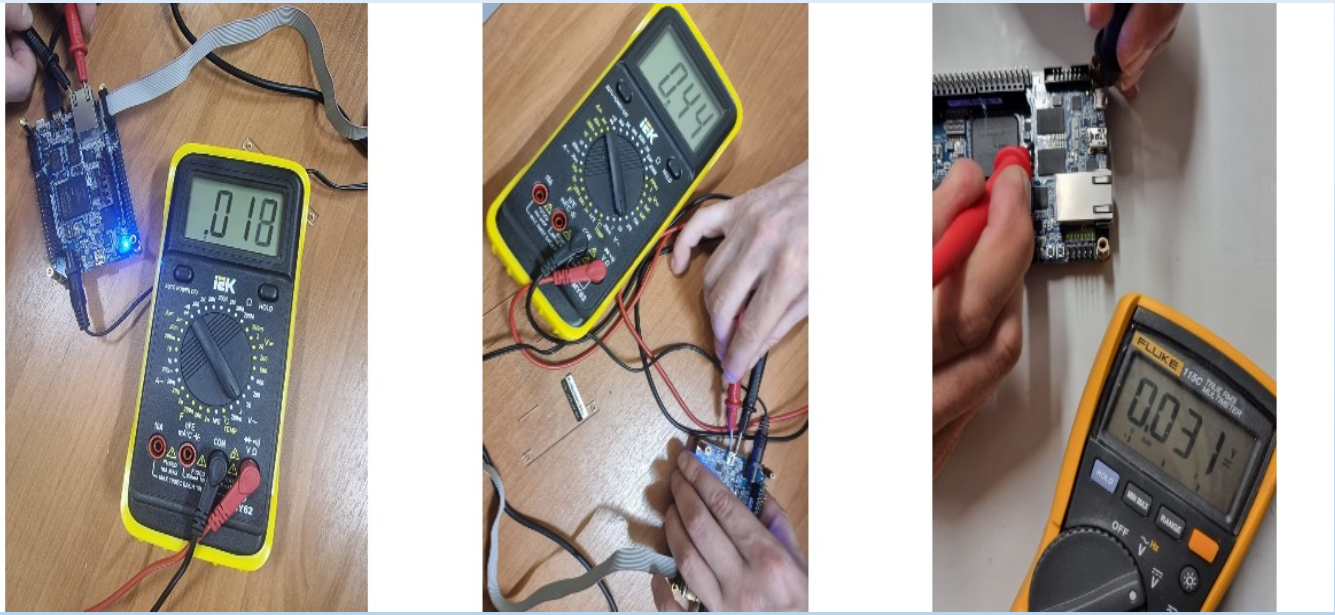
a) b)

Power supply scheme for the electronic circuit, detailing the voltage regulation for (a the HPS DDR3 memory and b) the FPGA processor.

Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.

Irradiation of the DE0-Nano SoC Kit using the IREN Accelerator caused ionization effects, leading to voltage and current fluctuations in its 5V/2A power network.

These disruptions resulted in malfunctions of key components, including the HPS_DDR3 memory, UART-to-USB, USB Blaster II, and the Ethernet port (Figure a–c).

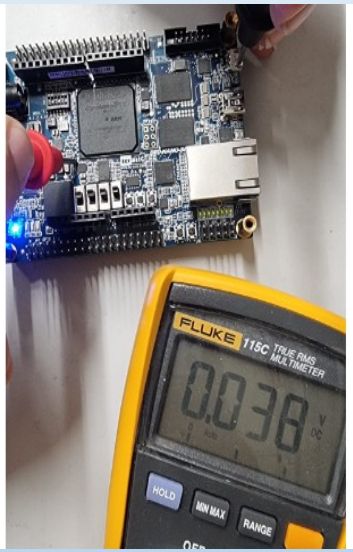


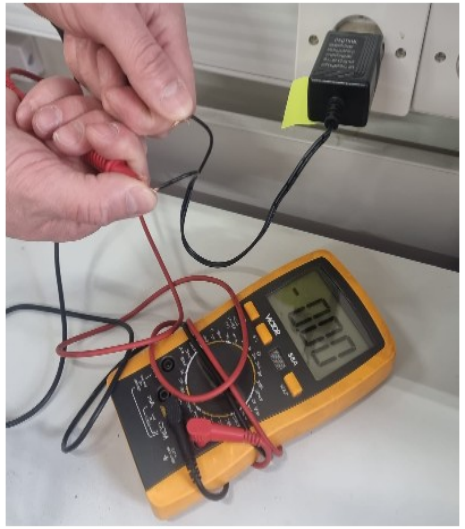
a) b) c)

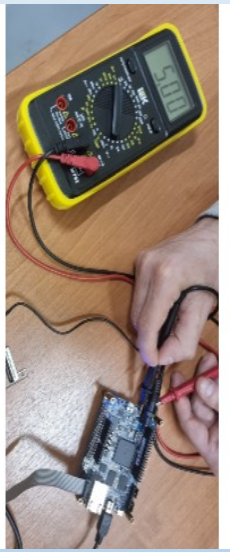
Radiation-induced disruptions affecting key components — (a) Ethernet port, (b) UART to USB interface, and (c) HPS_DDR3 memory.

Results from irradiating the Cyclone V FPGA on the DE0-Nano SoC Kit using the IREN accelerator.

- Radiation exposure can corrupt data transmission and disrupt communication with external devices by affecting the FPGA's +1.8 V power input (Figure a).
- This may result from interference with voltage regulation or transient faults.
- Additionally, the external 5V/2A household power supply is damaged (Figures b–c), further impacting system stability.







a) b) c)

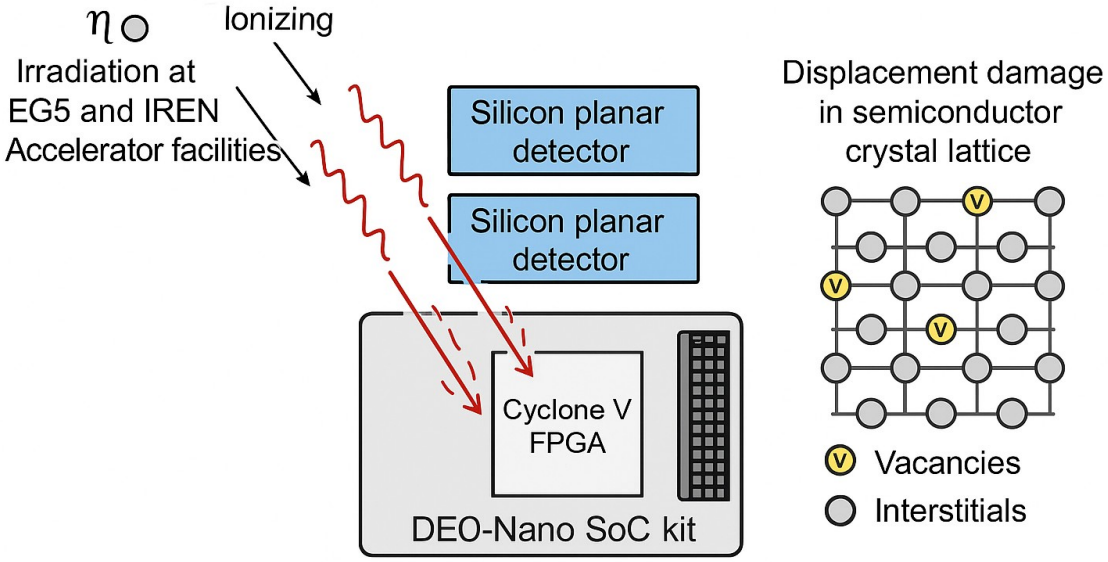
a) Radiation-induced disruption in power delivery to the FPGA: instability in the +1.2 V supply to the processor due to irradiation effects on voltage regulation, (b) damaged external 5V/2A power supply, and (c) its power input connection of 5V.

Determining Fast Neutron Fluence Using Planar Silicon Detectors

- Two silicon planar detectors were placed above the Cyclone V FPGA during irradiation at EG5 and IREN Accelerator facilities.

- Ionizing radiation (neutrons, gamma rays) causes displacement damage in the semiconductor crystal lattice.

- This damage creates vacancies and interstitials, reducing the performance of systems like the DE0-Nano SoC kit.



Two sillcon planar detectors were placed above the Cyclone V FPGA during irradiation at EG5 and IREN Accelerator facilities

Selection of a Silicon Planar Detector for Fast Neutron Fluence Measurement

Silicon detectors are sensitive to fast neutron irradiation.

- Radiation **damages silicon**, increasing its **reverse bulk (dark) current**.

- This **current increase** is proportional to:
  - **Neutron fluence (Φ)**
  - **Sensitive volume (V)** of the detector

Fluence Estimation Formula

$$\Delta I = \alpha \times \Phi \times V,$$

$$\Delta I = I - I_0 \,(\mathrm{A})$$

- **I**: Post-irradiation dark current
- **I_0**: Pre-irradiation dark current
- Both measured at full depletion voltage and normalized to **+20 °C**

Selection of a Silicon Planar Detector for Fast Neutron Fluence Measurement

Parameter Definitions

Φ (cm^{-2}): 1 MeV-equivalent fast neutron fluence

α_i = (5 ± 0.5) × 10^{-17} A/cm:

- Current-related damage constant
- For 1 MeV neutrons at +20 °C (excluding self-annealing)

V = d × S (cm^3):

- Sensitive volume
- **d** = detector thickness (cm)
- **S** = active area (cm^2)

Final Fluence Calculation

$$\Phi = \Delta I/(\alpha_i.V)\ ,$$

By measuring **ΔI** and knowing **α_i**, **d**, and **S**, the neutron fluence **Φ (n/cm^2)** can be accurately determined.

Selection of a Silicon Planar Detector for Fast Neutron Fluence Measurement

Table : Bulk Dark Current Measurements

- Shows results before and after fast neutron irradiation.
- Used in neutron monitor applications.

- Van de Graaff refers to a type of electrostatic accelerator.
- So together, it indicates that the irradiation was performed using both the Van de Graaff accelerator and the IREN neutron source.

№ Silicon Detector	d, mm	S, mm²	I, n A (V = 100 V) (before irradiation)	I, n A (V = 100 V) (after irradiation)	ΔI, nA (V = 100 V)	$\Phi_{n,\,eq}$ $_{<1MeV>}$ /см²
№16	0.266	13	0.6	4.21	3.56	2.06×10^{10} Van de Graaff
№17	0.251	13	0.7	105	104	6.36×10^{11} Van de

Impact of Radiation on I-V Characteristics

Normal Condition:

- I–V curve shows a **gradual increase in leakage current** with increasing reverse bias voltage.

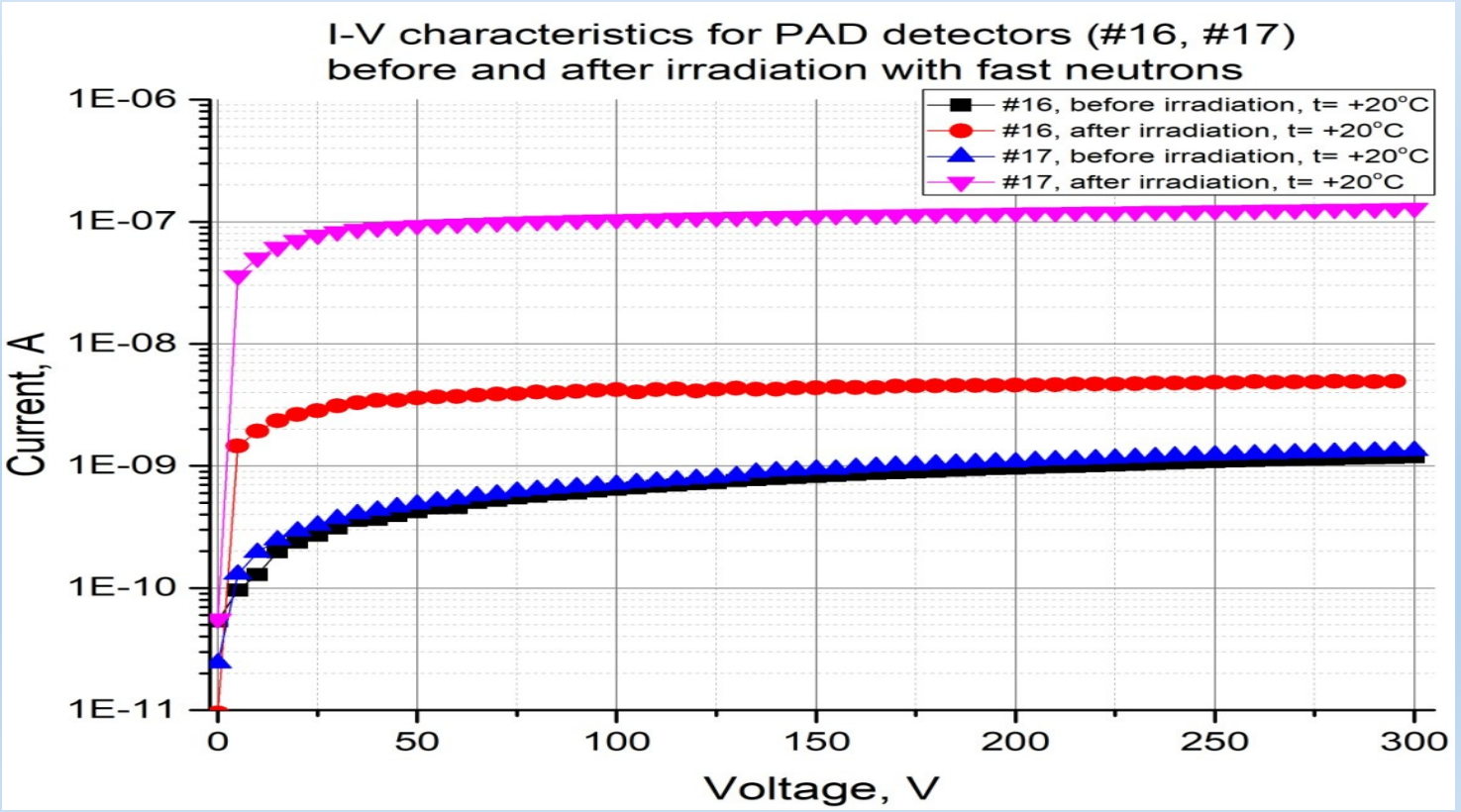
After Radiation Exposure:

- Entire curve **shifts upward**, indicating **higher leakage current** at all voltages.
- Curve often becomes **steeper**.

Leakage current increases more rapidly and breakdown voltage decreases in silicon detectors irradiated with the IREN accelerator.

Comparison: IREN vs. EG5 Irradiation

- Silicon detectors irradiated at IREN show:
- Greater increase in leakage current
- More severe radiation damage



Conclusion

- Radiation testing conducted on **DE0-Nano SoC** boards at EG-5 and IREN facilities.

- around **3 MeV neutron exposure** (Setup 1), the Cyclone V FPGA maintained operation for ~80 minutes before periodic shutdowns, followed by automatic 30-minute recoveries . The root cause of these shutdowns is still being investigated.

- Under **higher energy exposure (20–30 MeV)** in Setup 2, the DE0-Nano SoC's power system **completely failed after ~4 hours**.

- Results highlight the **vulnerability of power systems and interfaces** under increasing radiation levels, stressing the need for **radiation-hardened design and mitigation strategies**.

- Planned **repair and re-evaluation** include replacing faulty power regulators.

- Future work: Quantify radiation impact on **FPGA stability, data integrity, and reliability** over time.

Acknowledgement

We gratefully acknowledge Dr. Nicolay Zamyatin for his significant contributions to the investigation and experimental phases of this work. His expertise and support played a vital role in the development and completion of this study.

Thanks for your Attention

Full Name

Youmna
Ghoneim

Tel.: +7 (923) 40 80 895
E-mail: youmnasami24@gmail.com, Ghoneim@jinr.ru

Telegram Contact

15.05.2025